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IA59032
32-Bit High-Speed Microprocessor Slice
Data Sheet

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Features

- **Eight CMOS 2901 Type Devices in a Single Package**
- **32 x 32 Dual Port RAM**
- **High Speed Operation**
  - **23MHz Read-Modify-Write Cycle**
- **Fully Firmware Compatible with the 2901**

The IA59032 is a "plug-and-play" drop-in replacement for the original WSI™ WS59032. This replacement IC has been developed using innovASIC's MILES™, or Managed IC Lifetime Extension System, cloning technology. This technology produces replacement ICs far more complex than "emulation" while ensuring they are compatible with the original IC. MILES™ captures the design of a clone so it can be produced even as silicon technology advances. MILES™ also verifies the clone against the original IC so that even the "undocumented features" are duplicated. This data sheet documents all necessary engineering information about the IA59032 including functional and I/O descriptions, electrical characteristics, and applicable timing.
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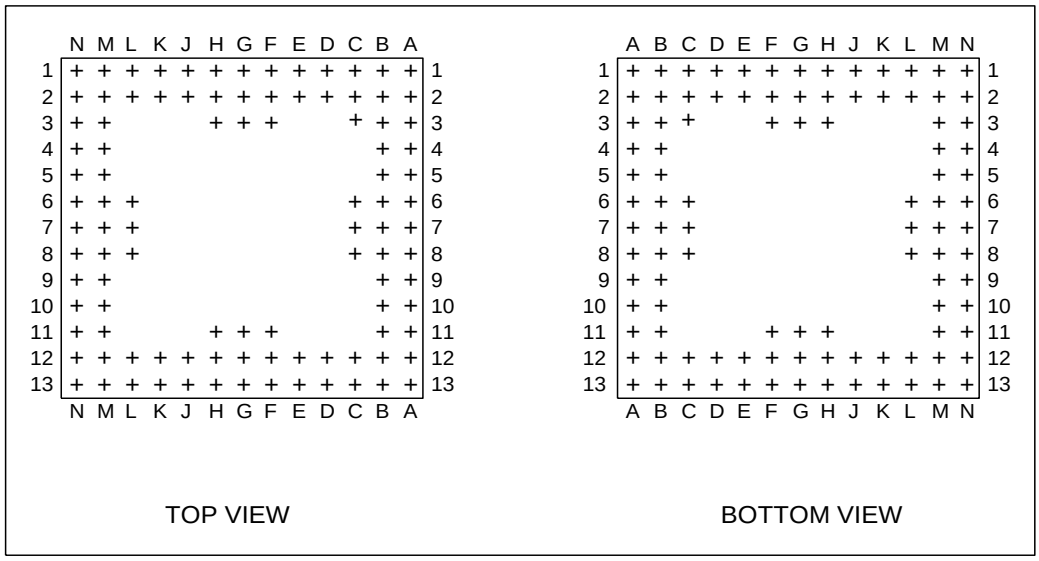
100 PIN PGA PACKAGE:



PIN DESIGNATOR:

PIN NAME	PGA GRID #	PIN NAME	PGA GRID #	PIN NAME	PGA GRID #	PIN NAME	PGA GRID #
VCC	N1	B3	N2	D23	B1	Y7	K12
VCC	A1	B4	M3	D24	B2	Y8	K13
GND	N7	D0	N6	D25	B3	Y9	J12
GND	G13	D1	M6	D26	A2	Y10	J13
GND	A12	D2	L6	D27	A3	Y11	H11
GND	C6	D3	N5	D28	B4	Y12	H12
RAM0	M7	D4	M5	D29	A4	Y13	H13
RAM31	B6	D5	N4	D30	B5	Y14	G12
Q0	L7	D6	M4	D31	A5	Y15	G11
Q31	A6	D7	N3	I0	N8	Y16	F13
CLK	A7	D8	H3	I1	M8	Y17	F12
CIN	N13	D9	H2	I2	L8	Y18	F11
CN-32	A9	D10	H1	I3	N9	Y19	E13
OVR	C8	D11	G1	I4	M9	Y20	E12
F-0	C13	D12	G3	I5	N10	Y21	D13
F31	B8	D13	G2	I6	A8	Y22	D12
OEN	M12	D14	F1	I7	B7	Y23	B13
A0	J1	D15	F2	I8	C7	Y24	C12
A1	J2	D16	F3	Y0	M10	Y25	A13
A2	K1	D17	E1	Y1	N11	Y26	B12
A3	K2	D18	E2	Y2	N12	Y27	B11
A4	L1	D19	D1	Y3	M11	Y28	A11
B0	M1	D20	D2	Y4	M13	Y29	B10
B1	L2	D21	C1	Y5	L12	Y30	A10
B2	M2	D22	C2	Y6	L13	Y31	B9

Description

The IA59032 is a 32-bit high-speed microprocessor that combines the functions of eight 2901 4-bit slice processors and distributed look-ahead carry generation on a single high performance CMOS device. The IA59032 dual port RAM is 32-bits wide and 32 words deep. This architecture provides grater flexibility and eases the task of generating new microcode while maintaining 100% compatibility with existing 2901 based microcode.

BLOCK DIAGRAM

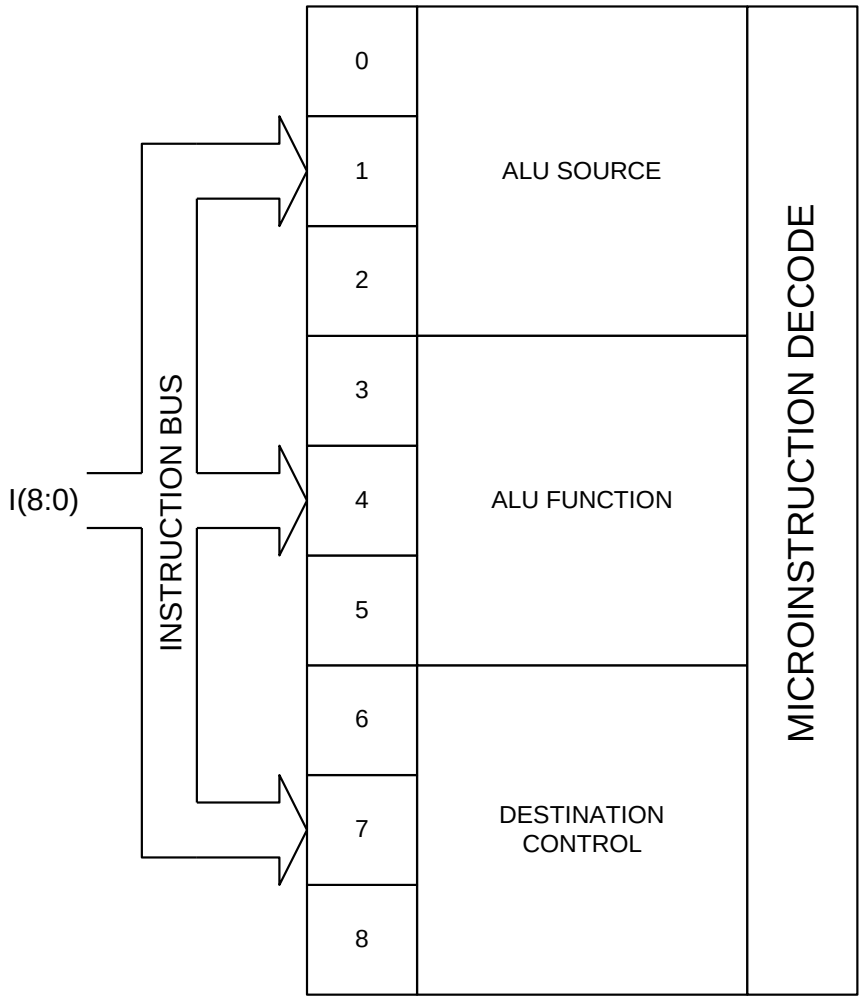
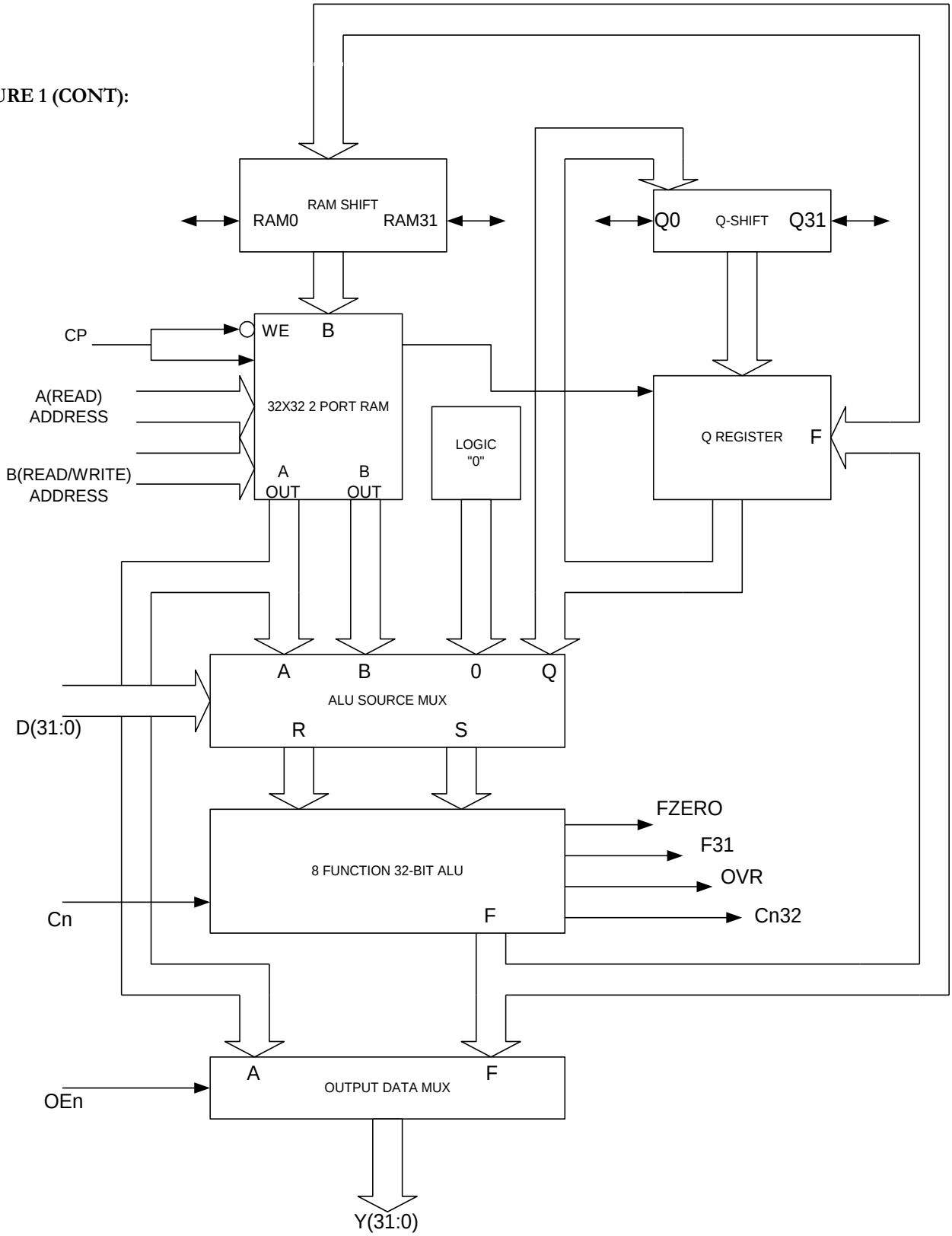


FIGURE 1 (CONT):



A detailed block diagram for the IA59032 is shown in **Error! Reference source not found.**. The two key elements in the block diagram are the 32 word by 32-bit 2-port RAM and the high-speed ALU.

Data in any of the 32 words of the RAM can be read from the A-port of the RAM as controlled by the 4-bit A address field input. Likewise, data in any of the 32 words of the RAM as defined by the B address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A select field and B select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (CP low), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input mux. This configuration is used to shift the ALU output data F if desired. This three-input mux scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The high speed ALU can perform three binary arithmetic and five logic operations on the two 32-bit input words R and S. The R input field is driven from a 2-input mux, while the S input field is driven by a 3-input mux. Both muxes also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to **Error! Reference source not found.**, the ALU R-input mux has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input mux has the RAM A-port, B-port, and the Q register connected as inputs.

This muxing scheme provides the capability of selecting various pairs of the A, B, D, Q, and zero inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. The I(2:0) inputs are the microinstruction inputs used to select the ALU source operands.

The two source operands not fully described as yet are the D input and the Q input. The D input is the 32-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 32-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is capable of performing three binary arithmetic and five logic functions. The I(5:3) inputs are used to select the ALU function.

The ALU has three status-oriented outputs. These are F31, FZERO, and OVR. The F31 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F31 is non-inverted with respect to the sign bit output Y(31). The FZERO output is used for zero detect. It is an open-collector output. FZERO is HIGH when all F outputs are LOW. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The OVR output is HIGH when overflow exists.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available, as defined by the I(8:6) inputs.

The 32-bit data output field (Y) features three-state outputs. An output control (OEn) is used to enable the three-state outputs. When OEn is HIGH, the Y outputs are in the high-impedance state.

A two input mux is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. I(8:6) inputs control this selection.

As was discussed previously, the RAM inputs are driven from a three-input mux. This allows the ALU outputs to be entered non-shifted, shifted up one position (X2) or shifted down one position (/2). The shifter has two ports; one is labeled RAM0 and the other is RAM31. Both of these ports consist of a buffer driver with a three-state output and an input to the mux. Thus, in the shift up mode, the RAM31 buffer is enabled and the RAM0 mux input is enabled. Likewise, is in the shift down mode, the RAM0 buffer and RAM31 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the mux inputs are not selected. The I(8:6) inputs control the shifter.

Similarly, the Q register is driven from a 3-input mux. In the no-shift mode, the mux enters the ALU data into the Q register. In either the shift-up or shift-down mode, the mux selects the Q register data appropriately shifted up or down. The Q shifter also has two ports; Q0 and Q31. The operations of these two ports are similar to the RAM shifter and are also controlled from the I(8:6) inputs.

The clock input controls the RAM, Q register, and the A and B data latches. When enabled, data is clocked into the Q register on the LOW to HIGH transition of the clock. When CP is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When CP is LOW, the latches are closed and will retain the last data entered. New data will be written into the RAM defined by the B address field when the clock input is LOW.

I/O Signal Description

The diagram below describes the I/O characteristics for each signal on the IC. The signal names correspond to the signal names on the pinout diagrams provide.

I/O CHARACTERISTICS:

SIGNAL NAME	I/O	DESCRIPTION
A(4:0)	I	The five address inputs to the on board RAM used to select word to be displayed throught the A-port
B(4:0)	I	Addresses which select the word of on board RAM which is to be diplayed through the B-port and into which data is written when the clock is low.
I(8:0)	I	The nine instruction control lines. Used to determine what data sources will be applied to the ALU(I(2:0)), what function the ALU will perform (I(5:3)), and what data is to be deposited in the Q-register or on board RAM (I(8:6)).
Q31 RAM31	I/O	Signal paths at the MSB of the on-board RAM and the Q-register which are used for shifting data. When the destination code on I(8:6) indicates an up shift(Octal 6 or 7) the three state outputs are enabled and the MSB of the Q-register is available on the Q31 pin. Otherwise the pins appear as inputs. When the destination code calls for a down shift the pins are used as the data inputs to the MSB of the Q-register (Octal 4) and RAM (Octal 4 and 5).
Q0 RAM0	I/O	Shift lines similar to the Q31 and RAM 31; however the decription is applied to the LSB of RAM and the Q-register.
D(31:0)	I	Direct data inputs which may be selected as one of the ALU data sources for entering data into the device. D0 is the LSB.
Y(31:0)	O	Tri-statable outputs which, when enabled, display either the data on the A-port of the register stack or the outputs of the ALU as determined by the destination code I(8:6).
OEn	I	Output enable. When HIGH, the Y outputs are in the high impedance state. When LOW, either the contents of the A-register or the outputs of the ALU are displayed on Y(31:0).
OVR	O	Overflow. This signal indicates that an overflow into the sign bit has occurred as a result of a two's complement operation.
FZERO	O	This output, when HIGH, indicates that the result of an ALU operation is zero.
F31	O	The most significnt ALU output bit.
Cn	I	The carry-in to the ALU.
Cn32	O	The carry-out of the ALU.
CP	I	The clock input. The clock low time is the write enable to the on-board dual port RAM, including set-up time fot the A and B - portregisters. The A and B- port outputs change while the clock is HIGH. The Q-register is latched on the clock LOW-to-HIGH transition.

FUNCTIONAL TABLES

ALU SOURCE OPERAND CONTROL

MNEMONIC	MICRO CODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	OCTAL CODE	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

ALU FUNCTION CONTROL

MNEMONIC	MICRO CODE				ALU FUNCTION	SYMBOL
	I_5	I_4	I_3	OCTAL CODE		
ADD	L	L	L	0	R PLUS S	R+S
SUBR	L	L	H	1	S MINUS R	S-R
SUBS	L	H	L	2	R MINUS S	R-S
OR	L	H	H	3	R OR S	R \/ S
AND	H	L	L	4	R AND S	R /\ S
NOTRS	H	L	H	5	Rn AND S	Rn /\ S
EXOR	H	H	L	6	R EX-OR S	R \-/ S
EXNOR	H	H	H	7	R EX-NOR S	(R \-/ S)n

ALU DESTINATION CONTROL

MNEMONIC	MICRO CODE				RAM FUNCT'N		Q REG FUNCT'N		Y OUTPUT	RAM SHIFT'R		Q SHIFT'R	
	I_8	I_7	I_6	OCTAL CODE	SHIFT	LOAD	SHIFT	LOAD		RAM_0	RAM_{15}	Q_0	Q_{15}
QREG	L	L	L	0	X	NONE	NONE	F→Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F→B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F→B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_{15}	Q_0	IN_{15}
RAMD	H	L	H	5	DOWN	F/2→B	X	NONE	F	F_0	IN_{15}	Q_0	X
RAMQU	H	H	L	6	UP	2F→B	UP	2Q→Q	F	IN_0	F_{15}	IN_0	Q_{15}
RAMU	H	H	H	7	UP	2F→B	X	NONE	F	IN_0	F_{15}	X	Q_{15}

*X Don't care
B=Register addressed by B inputs
DOWN is toward LSB, UP is toward MSB

SOURCE OPERAND AND ALU FUNCTION MATRIX

		I(2:0) OCTAL CODE							
		0	1	2	3	4	5	6	7
I(5:3) OCTAL CODE	ALU FUNCTION	ALU SOURCE (R,S)							
		A,Q	A,B	0,Q	0,B	0,A	D,A	D,Q	D,0
0	C_n=L R plus S C_n=H	A+Q A+Q+1	A+B A+B+1	Q Q+1	B B+1	A A+1	D+A D+A+1	D+Q D+Q+1	D D+1
1	C_n=L S minus R C_n=H	Q-A-1 Q-A	B-A-1 B-A	Q-1 Q	B-1 B	-A-1 -A	A-D-1 A-D	Q-D-1 Q-D	-D-1 -D
2	C_n=L R minus S C_n=H	A-Q-1 A-Q	A-B-1 A-B	-Q-1 -Q	-B-1 -B	A A+1	D-A-1 D-A	D-Q-1 D-Q	D-1 D
3	R OR S	A \/ Q	A \/ B	Q	B	A	D \/ A	D \/ Q	D
4	R AND S	A /\ Q	A /\ B	0	0	0	D /\ A	D /\ Q	0
5	Rn AND S	An /\ Q	An /\ B	Q	B	A	Dn /\ A	Dn /\ Q	0
6	R EXOR S	A \-/ Q	A \-/ B	Q	B	A	D \-/ A	D \-/ Q	D

* + = PLUS, - = Minus, \/ = OR, /\ = AND, \-/ = EX-OR

SOURCE OPERANDS AND ALU FUNCTIONS

Eight source operand pairs are available to the ALU as determined by the I0-I2 instruction inputs. The ALU performs eight functions; three of which are arithmetic and five of which are logic functions. This function selection is controlled by the I3-I5 instruction inputs. When in the arithmetic mode, the ALU results are also affected by the carry, Cn. In the logic mode, the Cn input has no effect.

The matrix of Table 4 results when Cn and I0 through I5 are viewed together. Table 5 defines the logic operation which the IA59032 has the capability to perform while Table 6 demonstrates the arithmetic operations of the device. Both carry-in HIGH (Cn = 1) and carry-in LOW (Cn = 0) are defined in these operations.

ALU LOGIC MODE FUNCTIONS

OCTAL I(5:3), I(2:0)	GROUP	FUNCTION
4,0	AND	A /\ Q
4,1		A /\ B
4,5		D /\ A
4,6		D /\ Q
3,0	OR	A \/ Q
3,1		A \/ B
3,5		D \/ A
3,6		D \/ Q
6,0	EXOR	A \-/ Q
6,1		A \-/ B
6,5		D \-/ A
6,6		D \-/ Q
7,0	EXNOR	(A \-/ Q)n
7,1		(A \-/ B)n
7,5		(D \-/ A)n
7,6		(D \-/ Q)n
7,2	INVERT	Qn
7,3		Bn
7,4		An
7,7		Dn
6,2	PASS	Qn
6,3		Bn
6,4		An
6,7		Dn
3,2	PASS	Q
3,3		B
3,4		A
3,7		D
4,2	ZERO	0
4,3		0
4,4		0
4,7		0
5,0	MASK	An /\ Q
5,1		An /\ B
5,5		Dn /\ A
5,6		Dn /\ Q

ALU ARITHMETIC MODE FUNCTIONS

OCTAL I(5:3), I(2,0)	C_n=0(LOW)		C_n=1(HIGH)	
	GROUP	FUNCTION	GROUP	FUNCTION
0,0 0,1 0,5 0,6	ADD	A+Q A+B D+A D+Q	ADD PLUS ONE	A+Q+1 A+B+1 D+A+1 D+Q+1
0,2 0,3 0,4 0,7	PASS	Q B A D	INCREMENT	Q+1 B+1 A+1 D+1
1,2 1,3 1,4 2,7	DECREMENT	Q-1 B-1 A-1 D-1	PASS	Q B A D
2,2 2,3 2,4 1,7	1'S COMPLEMENT	-Q-1 -B-1 -A-1 -D-1	2'S COMPLEMENT (NEGATE)	-Q -B -A -D
1,0 1,1 1,5 1,6 2,0 2,1 2,5 2,6	SUBTRACT 1'S COMPLEMENT	Q-A-1 B-A-1 A-D-1 Q-D-1 A-Q-1 A-B-1 D-A-1 D-Q-1	SUBTRACT 2'S COMPLEMENT	Q-A B-A A-D Q-D A-Q A-B D-A D-Q

AC/DC Parameters:

Absolute maximum ratings:
Operating Temp (Comm'l)…….....……...…..0°C to +70°C
(Mil)……...…-55°C to +125°C
Storage temperature.....…….....……...…- 55°C to 155°C
Voltage on any pin with
respect to GND…….....……..…...-0.6V to +7V
Latch Up Protection….....….....>200mA
ESD Protection…….……>± 2000V

DC Characteristics:

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNITS
V_{oh}	Output High Voltage	All outputs	I_{oh}=*	V_{DD}-1.0		V
V_{ol}	Output Low Voltage	Y(31:0)	Iol=*		V_{SS}+0.4	V
			Iol=*			
		All others	Iol=*			
V_{ih}	Input High Voltage	Guaranteed Input High Voltage		2		V
V_{il}	Input Low Voltage	Guaranteed Input Low Voltage			0.8	V
I_{ix}	Input Load Current	V_{CC}=Max, V_{in}=G_{nd} or V_{CC}		-10	10	uA
I_{oz}	High Impedance Output Current	B_{CC}=Max, V_O=G_{nd} or V_{CC}		-50	50	uA
I_{CC}	Power Supply Current	V_{CC}=Max	Comm'l (0C to 70C) Mil (-55C to 125C)		70 85	mA

***** As per specific buffer

CYCLE TIME AND CLOCK CHARACTERISTICS:

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	60ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I=432 or 632)	23.6 MHz
Minimum Clock Low Time	28ns
Minimum Clock High	30ns
Minimum Clock Period	60ns

OUTPUT ENABLE/DISABLE TIME:

From OEn LOW to Y output enable	36ns
From OEn HIGH to Y output enable	30ns

COMBINATIONAL PROPAGATION DELAYS (Cl = 50 pf):

To Output		**Y**	**F31**	**C_n+32**	**FZERO**	**OVR**	**RAM0, RAM31**	**Q0, Q31**	**UNITS**
From Input	A,B Address	66	68	58	66	62	75	--	ns
	D(31:0)	45	45	35	45	35	48	--	
	C_n	36	36	18	36	32	42	--	
	I(2:0)	46	46	35	46	41	58	--	
	I(5:3)	51	51	41	51	46	53	--	
	I(8:6)	22	--	--	--	--	22	20	
	A Bypass ALU (I=2XX)	48	--	--	--	--	--	--	
	Clock	51	51	42	51	48	59	22	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT:

CP		Set up before H to L	Hold after H to L	Set up before L to H	Hold after L to H	UNITS
Input	A,B Source Address	20	1 (note 3)	53 (note 4)	0	ns
	B Destination Address	10	Do not change (note 2)		0	
	D(31:0)	--	--	20	--	
	Cn	--	--	22	0	
	I(2:0)	--	--	28	0	
	I(5:3)	--	--	30	0	
	I(8:6)	7	Do not change (note 2)		0	
	RAM0,31 and Q0, 31	--	--	7	3	

*Notes :

1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.

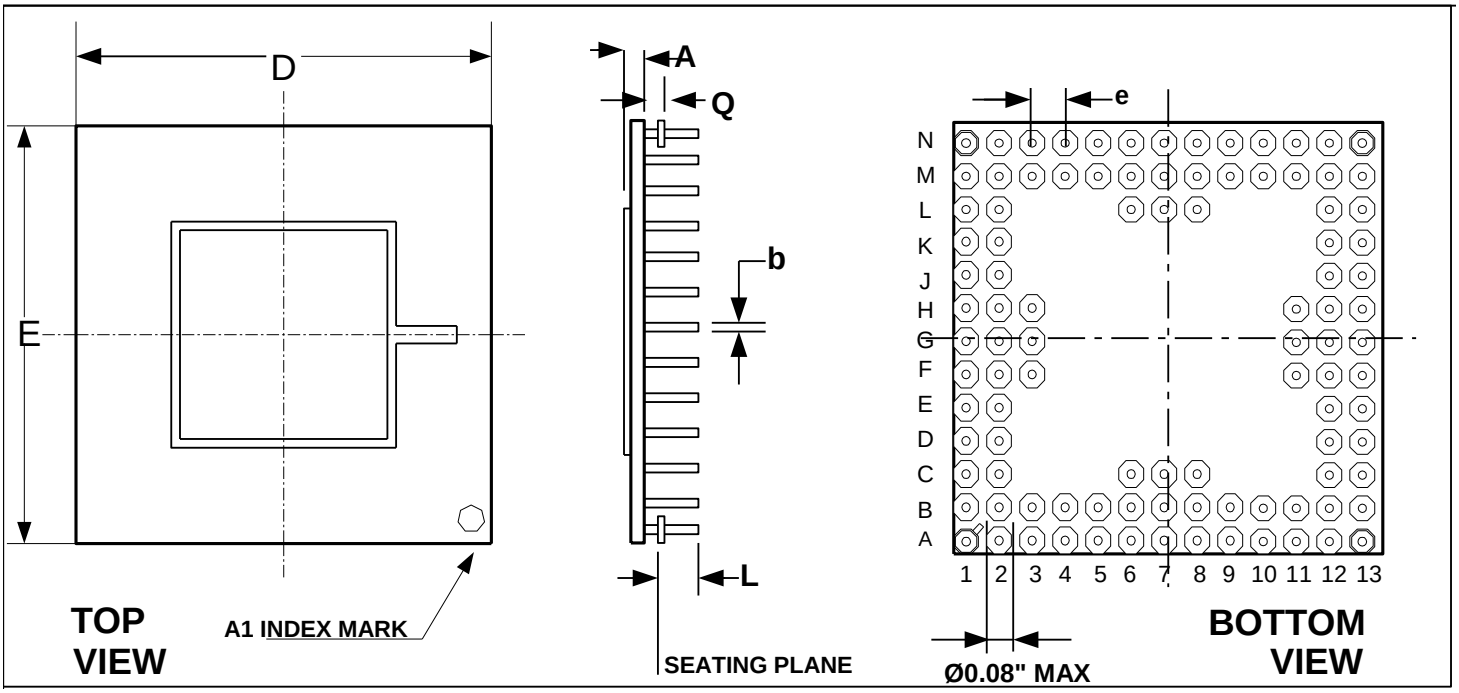
2) The phrase "Do Not Change" indicates that certain signals must remain LOW for the duration of the clock LOW time. Otherwise, erroneous operation may be the result.

3) Prior to clock HIGH to LOW transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the 'A' address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock LOW period.

4) Set-up time before HIGH to LOW included here.

Packaging Information

100 CPGA PACKAGE



100 CPGA, (13X13 pins)

Symbol	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.67	2.92	3.68	0.105	0.115	0.145
b	0.41	0.46	0.51	0.016	0.018	0
D	33.22	33.53	33.83	1.308	0	1.332
E	33.22	33.53	33.83	1.308	0	1.332
e		33.53			0	
L		33.53			0	
Q		33.53			0	

Ordering Information

Part Number	Environmental/ Qual Level
IA59032-CPGA100I	Industrial

Revision History

The table below presents the sequence of revisions to document IA211001108.

Date	Revision	Description	Page(s)
August 19, 2008	03	First edition released.	NA