TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

64MBIT (8M × 8 BITS/4M × 16 BITS) CMOS FLASH MEMORY

DESCRIPTION

The TC58FVM6T2A/B2A is a 67108864-bit, 3.0-V read-only electrically erasable and programmable flash memory organized as 8388608 × 8 bits or as 4194304 × 16 bits. The TC58FVM6T2A/B2A features commands for Read, Program and Erase operations to allow easy interfacing with microprocessors. The commands are based on the JEDEC standard. The Program and Erase operations are automatically executed in the chip. The TC58FVM6T2A/B2A also features a Simultaneous Read/Write operation so that data can be read during a Write or Erase operation.

FEATURES

- Power supply voltage
  V_{DD} = 2.3 V~3.6 V
- Operating temperature
  Ta = −40°C~85°C
- Organization
  8M × 8 bits/4M × 16 bits
- Functions
  Simultaneous Read/Write
  Page Read (8 word/16 byte)
  Auto Program, Auto Page Program
  Auto Block Erase, Auto Chip Erase
  Fast Program Mode/Acceleration Mode
  Program Suspend/Resume
  Erase Suspend/Resume
  data polling/Toggle bit
  block protection, boot block protection
  Automatic Sleep, support for hidden ROM area
  common flash memory interface (CFI)
  Byte/Word Modes
- Block erase architecture
  8 × 8 Kbytes/127 × 64 Kbytes
- Boot block architecture
  TC58FVM6T2A: top boot block
  TC58FVM6B2A: bottom boot block
- Mode control
  Compatible with JEDEC standard commands
- Erase/Program cycles
  10^5 cycles typ.
- Access Time (Random/Page)

V_{DD}	CL = 30 pF	CL = 100 pF
2.7~3.6 V	65 ns/25 ns	70 ns/30 ns
2.3~3.6 V	70 ns/30 ns	75 ns/35 ns

- Power consumption
  10 μA (Standby)
  15 mA (Program/Erase operation)
  55 mA (Random Read operation)
  11 mA (Address Increment Read operation)
  5 mA (Page Read operation)
- Package
  TC58FVM6**AFT:
  TSOPI48-P-1220-0.50 (weight: 0.51 g)
  TC58FVM6**AXB:
  P-TFBGA56-0710-0.80AZ (weight: 0.125 g)

Ordering information

TC58 F V M6 T2 A FT 65

- Speed version
  - 65 = 65 ns
- Package
  - FT = TSOP
  - XB = FBGA
- Design rule
  - A = 0.16 μm
- Function/Boot block architecture/Bank ratio
  - T2 = Page mode/Top boot block/1:3:3:1
  - B2 = Page mode/Bottom boot block/1:3:3:1
- Capacity
  - M6 = 64Mbits
- Supply Voltage
  - V = 3 V system
- Device type
  - F = NOR Flash memory
- Toshiba CMOS E^2PROM

<table>
<tr><th>Ordering type</th><th>Boot block</th><th>Bank ratio</th><th>Package</th></tr>
<tr><td>TC58FVM6T2AFT65</td><td>Top</td><td rowspan="4">1:3:3:1</td><td rowspan="2">TSOPI48-P-1220-0.50</td></tr>
<tr><td>TC58FVM6B2AFT65</td><td>Bottom</td></tr>
<tr><td>TC58FVM6T2AXB65</td><td>Top</td><td rowspan="2">P-TFBGA56-0710-0.80AZ</td></tr>
<tr><td>TC58FVM6B2AXB65</td><td>Bottom</td></tr>
</table>

PIN ASSIGNMENT (TOP VIEW)···TC58FVM6**AFT

A15	1	48	A16
A14	2	47	$\overline{\text{BYTE}}$
A13	3	46	V_{SS}
A12	4	45	DQ15/A-1
A11	5	44	DQ7
A10	6	43	DQ14
A9	7	42	DQ6
A8	8	41	DQ13
A19	9	40	DQ5
A20	10	39	DQ12
$\overline{\text{WE}}$	11	38	DQ4
$\overline{\text{RESET}}$	12	37	V_{DD}
A21	13	36	DQ11
$\overline{\text{WP}}$/ACC	14	35	DQ3
RY/$\overline{\text{BY}}$	15	34	DQ10
A18	16	33	DQ2
A17	17	32	DQ9
A7	18	31	DQ1
A6	19	30	DQ8
A5	20	29	DQ0
A4	21	28	$\overline{\text{OE}}$
A3	22	27	V_{SS}
A2	23	26	$\overline{\text{CE}}$
A1	24	25	A0

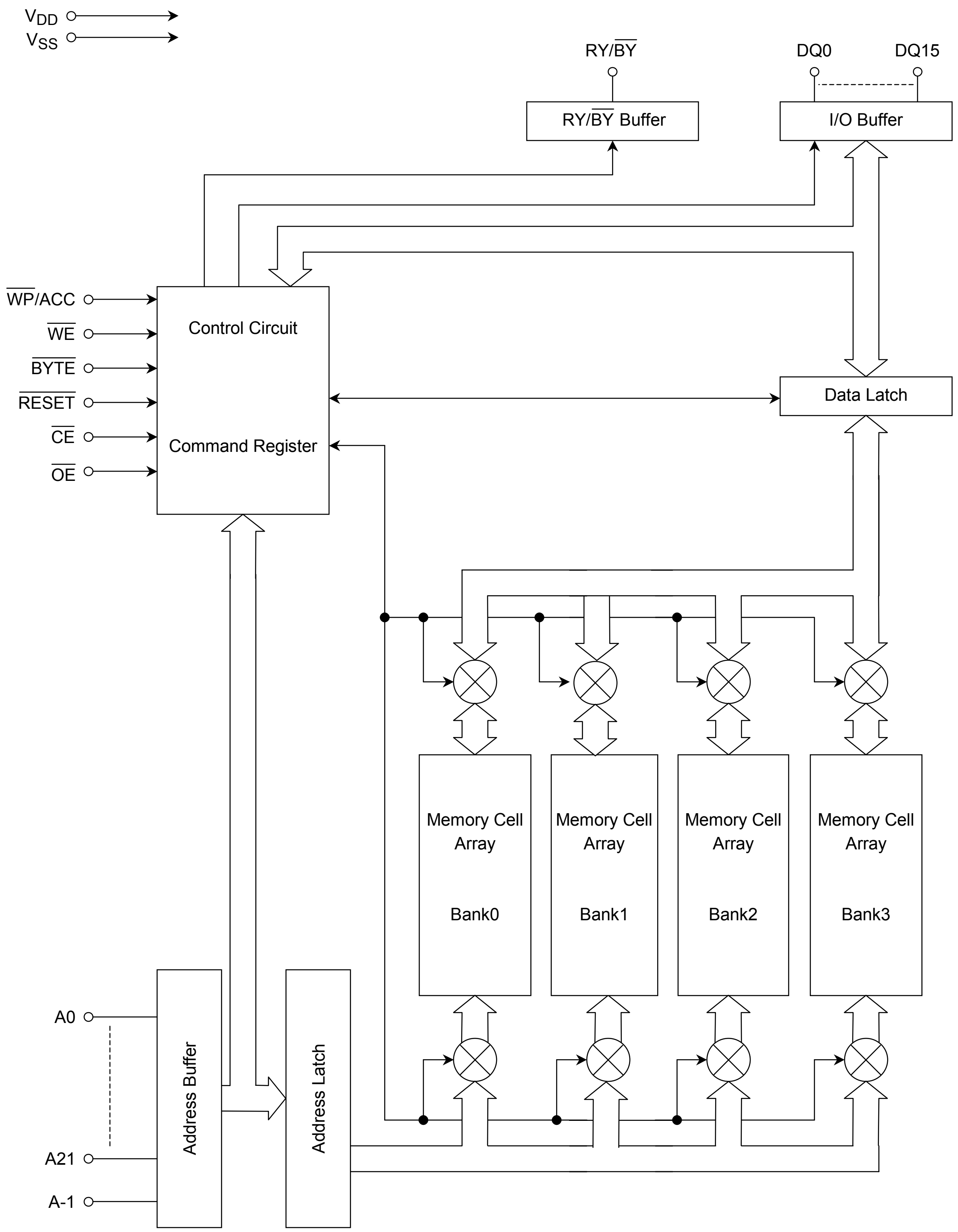
PIN NAMES

A-1, A0~A21	Address Input
DQ0~DQ15	Data Input/Output
$\overline{\text{CE}}$	Chip Enable Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{BYTE}}$	Word/Byte Select Input
$\overline{\text{WE}}$	Write Enable Input
RY/$\overline{\text{BY}}$	Ready/Busy Output
$\overline{\text{RESET}}$	Hardware Reset Input
$\overline{\text{WP}}$/ACC	Write Protect / Program Acceleration Input
V_{DD}	Power Supply
V_{SS}	Ground

PIN ASSIGNMENT (TOP VIEW)···TC58FVM6**AXB

	1	2	3	4	5	6	7	8
A	NC							NC
B	NC							NC
C		A3	A7	RY/$\overline{\text{BY}}$	$\overline{\text{WE}}$	A9	A13	
D		A4	A17	$\overline{\text{WP}}$/ACC	$\overline{\text{RESET}}$	A8	A12	
E		A2	A6	A18	A21	A10	A14	
F		A1	A5	A20	A19	A11	A15	
G		A0	DQ0	DQ2	DQ5	DQ7	A16	
H		$\overline{\text{CE}}$	DQ8	DQ10	DQ12	DQ14	$\overline{\text{BYTE}}$	
J		$\overline{\text{OE}}$	DQ9	DQ11	V_{DD}	DQ13	DQ15	
K		V_{SS}	DQ1	DQ3	DQ4	DQ6	V_{SS}	
L	NC							NC
M	NC							NC

BLOCK DIAGRAM



MODE SELECTION

										BYTE MODE	WORD MODE
MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A9	A6	A1	A0	$\overline{RESET}$	$\overline{WP}$/ACC	DQ0~DQ7[1]	DQ0~DQ15
Read/Page Read	L	L	H	A9	A6	A1	A0	H	*	D_{OUT}	D_{OUT}
ID Read (Manufacturer Code)	L	L	H	V_{ID}	L	L	L	H	*	Code	Code
ID Read (Device Code)	L	L	H	V_{ID}	L	L	H	H	*	Code	Code
Standby	H	*	*	*	*	*	*	H	*	High-Z	High-Z
Output Disable	*	H	H	*	*	*	*	*	*	High-Z	High-Z
Write	L	H	(2)	A9	A6	A1	A0	H	*	D_{IN}	D_{IN}
Block Protect 1	L	V_{ID}	(2)	V_{ID}	L	H	L	H	*	*	*
Block Protect 2	L	H	H	*	L	H	L	V_{ID}	*	*	*
Verify Block Protect	L	L	H	V_{ID}	L	H	L	H	*	Code	Code
Temporary Block Unprotect	*	*	*	*	*	*	*	V_{ID}	*	*	*
Hardware Reset/Standby	*	*	*	*	*	*	*	L	*	High-Z	High-Z
Boot Block Protect	*	*	*	*	*	*	*	*	L	*	*

Notes: * = V_{IH} or V_{IL}, L = V_{IL}, H = V_{IH}

(1) DQ8~DQ14 are High-Z and DQ15/A-1 is Address Input in Byte Mode.
Addresses are A21~A0 in Word Mode ($\overline{BYTE}$ = V_{IH}), A21~A-1 in Byte Mode ($\overline{BYTE}$ = V_{IL}).

(2) Pulse input

ID CODE TABLE

CODE TYPE		A21~A12	A6	A1	A0	CODE (HEX)[1]
Manufacturer Code		*	L	L	L	0098h
Device Code	TC58FVM6T2A	*	L	L	H	0057h
	TC58FVM6B2A	*	L	L	H	0058h
Verify Block Protect		BA[2]	L	H	L	Data[3]

Notes: * = V_{IH} or V_{IL}, L = V_{IL}, H = V_{IH}

(1) DQ8~DQ14 are High-Z and DQ15/A-1 is Address Input in Byte Mode.

(2) BA: Block Address

(3) 0001h - Protected Block
0000h - Unprotected Block

COMMAND SEQUENCES

COMMAND SEQUENCE		BUS WRITE CYCLES REQ'D	FIRST BUS WRITE CYCLE		SECOND BUS WRITE CYCLE		THIRD BUS WRITE CYCLE		FOURTH BUS WRITE CYCLE		FIFTH BUS WRITE CYCLE		SIXTH BUS WRITE CYCLE	
			Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset		1	XXXh	F0h										
Read/Reset	Word	3	555h	AAh	2AAh	55h	555h	F0h	RA[1]	RD[2]				
	Byte		AAAh		555h		AAAh							
ID Read	Word	3	555h	AAh	2AAh	55h	BK[3] + 555h	90h	IA[4]	ID[5]				
	Byte		AAAh		555h		BK[3] + AAAh							
Auto-Program	Word	4	555h	AAh	2AAh	55h	555h	A0h	PA[6]	PD[7]				
	Byte		AAAh		555h		AAAh							
Auto PageProgram	Word	11	555h	AAh	2AAh	55h	555h	E6h	PA[6]	PD[7]	PA[6]	PD[7]	PA[6]	PD[7]
	Byte	19	AAAh		555h		AAAh							
Program Suspend		1	BK[3]	B0h										
Program Resume		1	BK[3]	30h										
Auto Chip Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
	Byte		AAAh		555h		AAAh		AAAh		555h		AAAh	
Auto Block Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	BA[8]	30h
	Byte		AAAh		555h		AAAh		AAAh		555h			
Block Erase Suspend		1	BK[3]	B0h										
Block Erase Resume		1	BK[3]	30h										
Block Protect 2		4	XXXh	60h	BPA[9]	60h	XXXh	40h	BPA[9]	BPD[10]				
Verify Block Protect	Word	3	555h	AAh	2AAh	55h	BK[3] + 555h	90h	BPA[9]	BPD[10]				
	Byte		AAAh		555h		BK[3] + AAAh							
Fast Program Set	Word	3	555h	AAh	2AAh	55h	555h	20h						
	Byte		AAAh		555h		AAAh							
Fast Program		2	XXXh	A0h	PA[6]	PD[7]								
Fast Program Reset		2	XXXh	90h	XXXh	F0h[13]								
Hidden ROM Mode Entry	Word	3	555h	AAh	2AAh	55h	555h	88h						
	Byte		AAAh		555h		AAAh							
Hidden ROM Program	Word	4	555h	AAh	2AAh	55h	555h	A0h	PA[6]	PD[7]				
	Byte		AAAh		555h		AAAh							
Hidden ROM Erase	Word	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	BA[8]	30h
	Byte		AAAh		555h		AAAh		AAAh		555h			
Hidden ROM Mode Exit	Word	4	555h	AAh	2AAh	55h	555h	90h	XXXh	00h				
	Byte		AAAh		555h		AAAh							
Query Command	Word	2	BK[3] + 55h	98h	CA[11]	CD[12]								
	Byte		BK[3] +AAh											

Notes: The system should generate the following address patterns:

Word Mode: 555H or 2AAH on address pins A10~A0 DQ8~DQ15 are ignored in Word Mode.

Byte Mode: AAAH or 555H on address pins A10~A-1

(1) RA: Read Address
(2) RD: Read Data
(3) BK: Bank Address = A21~A15
(4) IA: Bank Address and ID Read Address (A6, A1, A0)
Bank Address = A21~A15
Manufacturer Code = (0, 0, 0)
Device Code = (0, 0, 1)
(5) ID: ID Data
(6) PA: Program Address
(Input continuous 8 address from (A0, A1, A2) = (0, 0, 0) to (A0, A1, A2) = (1, 1, 1) in Page program.)
(7) PD: Program Data
(8) BA: Block Address = A21~A12
(9) BPA: Block Address and ID Read Address (A6, A1, A0)
Block Address = A21~A12
ID Read Address = (0, 1, 0)
(10) BPD: Verify Data
(11) CA: CFI Address
(12) CD: CFI Data
(13) F0H: 00H is valid too

SIMULTANEOUS READ/WRITE OPERATION

The TC58FVM6T2A/B2A features a Simultaneous Read/Write operation. The Simultaneous Read/Write operation enables the device to simultaneously write data to or erase data from a bank while reading data from another bank.

The TC58FVM6T2A/B2A has a total of four banks (8Mbits: 24Mbits: 24Mbits: 8Mbits). Banks can be switched between using the bank addresses (A21~A19). For a description of bank blocks and addresses, please refer to the Block Address Table and Block Size Table.

The Simultaneous Read/Write operation cannot perform multiple operations within a single bank. The table below shows the operation modes in which simultaneous operation can be performed.

Note that during Auto-Program execution or Auto Block Erase operation, the Simultaneous Read/Write operation cannot read data from addresses in the same bank which have not been selected for operation. Data from these addresses can be read using the Program Suspend or Erase Suspend function, however.

SIMULTANEOUS READ/WRITE OPERATION

STATUS OF BANK ON WHICH OPERATION IS BEING PERFORMED	STATUS OF OTHER BANKS
Read Mode	Read Mode
ID Read Mode(1)	
Auto-Program Mode	
Auto-Page Program Mode	
Fast Program Mode(2)	
Program Suspend Mode	
Auto Block Erase Mode	
Auto Multiple Block Erase Mode(3)	
Erase Suspend Mode	
Program during Erase Suspend	
Program Suspend during Erase Suspend	
CFI Mode	

(1) Only Command Mode is valid.
(2) Including times when Acceleration Mode is in use.
(3) If the selected blocks are spread across all nine banks, simultaneous operation cannot be carried out.

OPERATION MODES

In addition to the Read, Write and Erase Modes, the TC58FVM6T2A/B2A features many functions including block protection and data polling. When incorporating the device into a deign, please refer to the timing charts and flowcharts in combination with the description below.

READ MODE (PAGE READ)

To read data from the memory cell array, set the device to Read Mode. In the Read Mode, the device can perform high-speed random access and Page Read as an asynchronous ROM. The page size of the device is 8 word or 16 byte, with the appropriate page address being selected by address of A0-A2 (and A-1 in byte mode).

The device is automatically set to Read Mode immediately after power-on or on completion of automatic operation. A software reset releases ID Read Mode and the lock state which the device enters if an automatic operation ends abnormally, and sets the device to Read Mode. A hardware reset terminates operation of the device and resets it to Read Mode. When reading data without changing the address immediately after power-on, either input a hardware Reset or change $\overline{CE}$ from H to L.

ID Read Mode

ID Read Mode is used to read the device maker code and device code. The mode is useful in that it allows EPROM programmers to identify the device type automatically.

ID read can be executed in two ways, as follows:

(1) Applying V_{ID} to A9

This method is used mainly by EPROM programmers. Applying V_{ID} to A9 sets the device to ID Read Mode, outputting the maker code from address 00h and the device code from address 01h. Releasing V_{ID} from A9 returns the device to Read Mode. With this method all banks are set to ID Read Mode; thus, simultaneous operation cannot be performed.

(2) Input command sequence

With this method simultaneous operation can be performed. Inputting an ID Read command sets the specified bank to ID Read Mode. Banks are specified by inputting the bank address (BK) in the third Bus Write cycle of the Command cycle. To read an ID code, the bank address as well as the ID read address must be specified (with $\overline{\text{WP}}$/ACC $= V_{IH}$ or V_{IL}). The maker code is output from address BK + 00; the device code is output from address BK + 01. From other banks data are output from the memory cells. Inputting a Reset command releases ID Read Mode and returns the device to Read Mode.

Access time in ID Read Mode is the same as that in Read Mode. For a list of the codes, please refer to the ID Code Table.

Standby Mode

There are two ways to put the device into Standby Mode.

(1) Control using $\overline{\text{CE}}$ and $\overline{\text{RESET}}$

With the device in Read Mode, input $V_{DD} \pm 0.3$ V to $\overline{\text{CE}}$ and $\overline{\text{RESET}}$. The device will enter Standby Mode and the current will be reduced to the standby current (I_{DDS1}). However, if the device is in the process of performing simultaneous operation, the device will not enter Standby Mode but will instead cause the operating current to flow.

(2) Control using $\overline{\text{RESET}}$ only

With the device in Read Mode, input $V_{SS} \pm 0.3$ V to $\overline{\text{RESET}}$. The device will enter Standby Mode and the current will be reduced to the standby current (I_{DDS1}). Even if the device is in the process of performing simultaneous operation, this method will terminate the current operation and set the device to Standby Mode. This is a hardware reset and is described later.

In Standby Mode DQ is put in High-Impedance state.

Auto-Sleep Mode

This function suppresses power dissipation during reading. If the address input does not change for 150 ns, the device will automatically enter Sleep Mode and the current will be reduced to the standby current (I_{DDS2}). However, if the device is in the process of performing simultaneous operation, the device will not enter Standby Mode but will instead cause the operating current to flow. Because the output data is latched, data is output in Sleep Mode. When the address is changed, Sleep Mode is automatically released, and data from the new address is output.

Output Disable Mode

Inputting V_{IH} to $\overline{\text{OE}}$ disables output from the device and sets DQ to High-Impedance.

Command Write

The TC58FVM6T2A/B2A uses the standard JEDEC control commands for a single-power supply E^2PROM. A Command Write is executed by inputting the address and data into the Command Register. The command is written by inputting a pulse to $\overline{WE}$ with $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ ($\overline{WE}$ control). The command can also be written by inputting a pulse to $\overline{CE}$ with $\overline{WE} = V_{IL}$ ($\overline{CE}$ control). The address is latched on the falling edge of either $\overline{WE}$ or $\overline{CE}$. The data is latched on the rising edge of either $\overline{WE}$ or $\overline{CE}$. DQ0~DQ7 are valid for data input and DQ8~DQ15 are ignored.

To abort input of the command sequence use the Reset command. The device will reset the Command Register and enter Read Mode. If an undefined command is input, the Command Register will be reset and the device will enter Read Mode.

Software Reset

Apply a software reset by inputting a Read/Reset command. A software reset returns the device from ID Read Mode or CFI Mode to Read Mode, releases the lock state if automatic operation has ended abnormally, and clears the Command Register.

Hardware Reset

A hardware reset initializes the device and sets it to Read Mode. When a pulse is input to $\overline{RESET}$ for t_{RP}, the device abandons the operation which is in progress and enters Read Mode after t_{READY}. Note that if a hardware reset is applied during data overwriting, such as a Write or Erase operation, data at the address or block being written to at the time of the reset will become undefined.

After a hardware reset the device enters Read Mode if $\overline{RESET} = V_{IH}$ or Standby Mode if $\overline{RESET} = V_{IL}$. The DQ pins are High-Impedance when $\overline{RESET} = V_{IL}$. After the device has entered Read Mode, Read operations and input of any command are allowed.

Comparison between Software Reset and Hardware Reset

ACTION	SOFTWARE RESET	HARDWARE RESET
Releases ID Read Mode or CFI Mode.	True	True
Clears the Command Register.	True	True
Releases the lock state if automatic operation has ended abnormally.	True	True
Stops any automatic operation which is in progress.	False	True
Stops any operation other than the above and returns the device to Read Mode.	False	True

$\overline{BYTE}$/Word Mode

$\overline{BYTE}$ is used select Word Mode (16 bits) or Byte Mode (8 bits) for the TC58FVM6T2A/B2A. If V_{IH} is input to $\overline{BYTE}$, the device will operate in Word Mode. Read data or write commands using DQ0~DQ15. When V_{IL} is input to $\overline{BYTE}$, read data or write commands using DQ0~DQ7. DQ15/A-1 is used as the lowest address. DQ8~DQ14 will become High-Impedance.

Auto-Program Mode

The TC58FVM6T2A/B2A can be programmed in either byte or word units. Auto-Program Mode is set using the Program command. The program address is latched on the falling edge of the $\overline{WE}$ signal and data is latched on the rising edge of the fourth Bus Write cycle (with $\overline{WE}$ control). Auto programming starts on the rising edge of the $\overline{WE}$ signal in the fourth Bus Write cycle. The Program and Program Verify commands are automatically executed by the chip. The device status during programming is indicated by the Hardware Sequence flag. To read the Hardware Sequence flag, specify the address to which the Write is being performed.

During Auto Program execution, a command sequence for the bank on which execution is being performed cannot be accepted. To terminate execution, use a hardware reset. Note that if the Auto-Program operation is terminated in this manner, the data written so far is invalid.

Any attempt to program a protected block is ignored. In this case the device enters Read Mode 3 μs after the rising edge of the $\overline{WE}$ signal in the fourth Bus Write cycle.

If an Auto-Program operation fails, the device remains in the programming state and does not automatically return to Read Mode. The device status is indicated by the Hardware Sequence flag. Either a Reset command or a hardware reset is required to return the device to Read Mode after a failure. If a programming operation fails, the block which contains the address to which data could not be programmed should not be used. To build a more reliable system, the host processor should take measures to prevent subsequent use of failed blocks.

The device allows 0s to be programmed into memory cells which contain a 1. 1s cannot be programmed into cells which contain 0s. If this is attempted, execution of Auto Program will fail. This is a user error, not a device error. A cell containing 0 must be erased in order to set it to 1.

Auto-Page Program Mode

Auto-Page Program is a function which enables to simultaneously program 8words or 16bytes data.

In this mode Program time for 64M bit is less than 60% compare with Auto program mode. In word mode, input page program command during first bus write cycle to third bus write cycle. Input program data and address of (A0, A1, A2) = (0, 0, 0) in forth bus write cycle. Input increment address and program data during fifth bus write cycle to eleventh bus write cycle. After input eleventh bus write cycle , page program operation start. In byte mode, input increment address and program data of (A-1, A0, A1, A2) = (0, 0, 0, 0) --- (A-1, A0, A1, A2) = (1, 1, 1, 1) during fifth bus write cycle to nineteenth bus write cycle.

Fast Program Mode

Fast Program is a function which enables execution of the command sequence for the Auto Program to be completed in two cycles. In this mode the first two cycles of the command sequence, which normally requires four cycles, are omitted. Writing is performed in the remaining two cycles. To execute Fast Program, input the Fast Program command. Write in this mode uses the Fast Program command but operation is the same at that for ordinary Auto-Program. The status of the device is indicated by the Hardware Sequence flag and read operations can be performed as usual. To exit this mode, the Fast Program Reset command must be input. When the command is input, the device will return to Read Mode.

Acceleration Mode

The TC58FVM6T2A/B2A features Acceleration Mode which allows write time to be reduced. Applying V_{ACC} to $\overline{WP}$ or ACC automatically sets the device to Acceleration Mode. In Acceleration Mode, Block Protect Mode changes to Temporary Block Unprotect Mode. Write Mode changes to Fast Program Mode. Modes are switched by the $\overline{WP}$/ACC signal; thus, there is no need for a Temporary Block Unprotect operation or to set or reset Fast Program Mode. Operation of Write is the same as in Auto-Program Mode. Removing V_{ACC} from $\overline{WP}$/ACC terminates Acceleration Mode.

Program Suspend/Resume Mode

Program Suspend is used to enable Data Read by suspending the Write operation. The device accepts a Program Suspend command in Write Mode (including Write operations performed during Erase Suspend) but ignores the command in other modes. When the command is input, the address of the bank on which Write is being performed must be specified. After input of the command, the device will enter Program Suspend Read Mode after t_{SUSP}.

During Program Suspend, Cell Data Read, ID Read and CFI Data Read can be performed. When Data Write is suspended, the address to which Write was being performed becomes undefined. ID Read and CFI Data Read are the same as usual.

After completion of Program Suspend input a Program Resume command to return to Write Mode. When inputting the command, specify the address of the bank on which Write is being performed. If the ID Read or CFI Data Read functions is being used, abort the function before inputting the Resume command. On receiving the Resume command, the device returns to Write Mode and resumes outputting the Hardware Sequence flag for the bank to which data is being written.

Program Suspend can be run in Fast Program Mode or Acceleration Mode. However, note that when running Program Suspend in Acceleration Mode, V_{ACC} must not be released.

Auto Chip Erase Mode

The Auto Chip Erase Mode is set using the Chip Erase command. An Auto Chip Erase operation starts on the rising edge of $\overline{WE}$ in the sixth bus cycle. All memory cells are automatically preprogrammed to 0, erased and verified as erased by the chip. The device status is indicated by the Hardware Sequence flag.

Command input is ignored during an Auto Chip Erase. A hardware reset can interrupt an Auto Chip Erase operation. If an Auto Chip Erase operation is interrupted, it cannot be completed correctly. Hence an additional Erase operation must be performed.

Any attempt to erase a protected block is ignored. If all blocks are protected, the Auto Erase operation will not be executed and the device will enter Read mode 250 μs after the rising edge of the $\overline{WE}$ signal in the sixth bus cycle.

If an Auto Chip Erase operation fails, the device will remain in the erasing state and will not return to Read Mode. The device status is indicated by the Hardware Sequence flag. Either a Reset command or a hardware reset is required to return the device to Read Mode after a failure.

In this case it cannot be ascertained which block the failure occurred in. Either abandon use of the device altogether, or perform a Block Erase on each block, identify the failed blocks, and stop using them. To build a more reliable system, the host processor should take measures to prevent subsequent use of failed blocks.

Auto Block Erase/Auto Multi-Block Erase Modes

The Auto Block Erase Mode and Auto Multi-Block Erase Mode are set using the Block Erase command. The block address is latched on the falling edge of the $\overline{WE}$ signal in the sixth bus cycle. The block erase starts as soon as the Erase Hold Time (t_{BEH}) has elapsed after the rising edge of the $\overline{WE}$ signal. When multiple blocks are erased, the sixth Bus Write cycle is repeated with each block address and Auto Block Erase command being input within the Erase Hold Time (this constitutes an Auto Multi-Block Erase operation). If a command other than an Auto Block Erase command or Erase Suspend command is input during the Erase Hold Time, the device will reset the Command Register and enter Read Mode. The Erase Hold Time restarts on each successive rising edge of $\overline{WE}$. Once operation starts, all memory cells in the selected block are automatically preprogrammed to 0, erased and verified as erased by the chip. The device status is indicated by the setting of the Hardware Sequence flag. When the Hardware Sequence flag is read, the addresses of the blocks on which auto-erase operation is being performed must be specified. If the selected blocks are spread across all nine banks, simultaneous operation cannot be carried out.

All commands (except Erase Suspend) are ignored during an Auto Block Erase or Auto Multi-Block Erase operation. Either operation can be aborted using a Hardware Reset. If an auto-erase operation is interrupted, it cannot be completed correctly; therefore, a further erase operation is necessary to complete the erasing.

Any attempt to erase a protected block is ignored. If all the selected blocks are protected, the auto-erase operation is not executed and the device returns to Read Mode 250 μs after the rising edge of the $\overline{WE}$ signal in the last bus cycle.

If an auto-erase operation fails, the device remains in Erasing state and does not return to Read Mode. The device status is indicated by the Hardware Sequence flag. After a failure either a Reset command or a Hardware Reset is required to return the device to Read Mode. If multiple blocks are selected, it will not be possible to ascertain the block in which the failure occurred. In this case either abandon use of the device altogether, or perform a Block Erase on each block, identify the failed blocks, and stop using them. To build a more reliable system, the host processor should take measures to prevent subsequent use of failed blocks.

Erase Suspend/Erase Resume Modes

Erase Suspend Mode suspends Auto Block Erase and reads data from or writes data to an unselected block. The Erase Suspend command is allowed during an auto block erase operation but is ignored in all other operation modes. When the command is input, the address of the bank on which Erase is being performed must be specified.

In Erase Suspend Mode only a Read, Program or Resume command can be accepted. If an Erase Suspend command is input during an Auto Block Erase, the device will enter Erase Suspend Read Mode after t_{SUSE}. The device status (Erase Suspend Read Mode) can be verified by checking the Hardware Sequence flag. If data is read consecutively from the block selected for Auto Block Erase, the DQ2 output will toggle and the DQ6 output will stop toggling and RY/$\overline{BY}$ will be set to High-Impedance.

Inputting a Write command during an Erase Suspend enables a Write to be performed to a block which has not been selected for the Auto Block Erase. Data is written in the usual manner.

To resume the Auto Block Erase, input an Erase Resume command. On input of the command, the address of the bank on which the Write was being performed must be specified. On receiving an Erase Resume command, the device returns to the state it was in when the Erase Suspend command was input. If an Erase Suspend command is input during the Erase Hold Time, the device will return to the state it was in at the start of the Erase Hold Time. At this time more blocks can be specified for erasing. If an Erase Resume command is input during an Auto Block Erase, Erase resumes. At this time toggle output of DQ6 resumes and 0 is output on RY/$\overline{BY}$.

BLOCK PROTECTION

Block Protection is a function for disabling writing and erasing specific blocks. Block protection can be carried out in two ways: by supplying a high voltage (V_{ID}) to the device (see Block protection 1) or by supplying a high voltage and a command sequence (see Block protection 2).

(1) Block protection 1

Specify a device block address and make the following signal settings A9 = $\overline{OE}$ = V_{ID}, A1 = V_{IH} and $\overline{CE}$ = A0 = A6 = V_{IL}. Now when a pulse is input to $\overline{WE}$ for t_{PPLH}, the device will start to write to the block protection circuit. Block protection can be verified using the Verify Block Protect command. Inputting V_{IL} on $\overline{OE}$ sets the device to Verify Mode. 01h is output if the block is protected and 00h is output if the block is unprotected. If block protection was unsuccessful, the operation must be repeated. Releasing V_{ID} from A9 and $\overline{OE}$ terminates this mode.

(2) Block protection 2

Applying V_{ID} to $\overline{RESET}$ and inputting the Block Protect 2 command also performs block protection. The first cycle of the command sequence is the Set-up command. In the second cycle, the Block Protect command is input, in which a block address and A1 = V_{IH} and A0 = A6 = V_{IL} are input. Now the device writes to the block protection circuit. There is a wait of t_{PPLH} until this write is completed; however, no intervention is necessary during this time. In the third cycle the Verify Block Protect command is input. This command verifies the write to the block protection circuit. Read is performed in the fourth cycle. If the protection operation is complete, 01h is output. If a value other than 01h is output, block protection is not complete and the Block Protect command must be input again. Removing the V_{ID} input from $\overline{RESET}$ exits this mode.

Temporary Block Unprotection

The TC58FVM6T2A/B2A has a temporary block unprotection feature which disables block protection for all protected blocks. Unprotection is enabled by applying V_{ID} to the $\overline{RESET}$ pin. Now Write and Erase operations can be performed on all blocks except the boot blocks which have been protected by the Boot Block Protect operation. The device returns to its previous state when V_{ID} is removed from the $\overline{RESET}$ pin. That is, previously protected blocks will be protected again.

Verify Block Protect

The Verify Block Protect command is used to ascertain whether a block is protected or unprotected. Verification is performed either by inputting the Verify Block Protect command or by applying V_{ID} to the A9 pin. The Verify Block Protect command, which can be performed simultaneously with operations in another bank, is performed by setting the block address with A0 = A6 = V_{IL} and A1 = V_{IH}. If the block is protected, 01h is output. If the block is unprotected, 00h is output.

Inputting the verify block protect command sequence sets the specified bank to the Verify Block Protect mode. Inputting a Reset command releases this mode and returns the device to Read Mode. When verifying block protect across a bank boundary, a Reset command is needed at the time of the change of a bank.

Boot Block Protection

Boot block protection temporarily protects certain boot blocks using a method different from ordinary block protection. Neither V_{ID} nor a command sequence is required. Protection is performed simply by inputting V_{IL} on $\overline{WP}$/ACC . The target blocks are the two pairs of boot blocks. The top boot blocks are BA133 and BA134; the bottom boot blocks are BA0 and BA1. Inputting V_{IH} on $\overline{WP}$/ACC releases the mode. From now on, if it is necessary to protect these blocks, the ordinary Block Protection Mode must be used.

Hidden ROM Area

The TC58FVM6T2A/B2A features a 64-Kbyte hidden ROM area which is separate from the memory cells. The area consists of one block. Data Read, Write and Protect can be performed on this block. Because Protect cannot be released, once the block is protected, data in the block cannot be overwritten.

The hidden ROM area is located in the address space indicated in the HIDDEN ROM AREA ADDRESS TABLE. To access the Hidden ROM area, input a Hidden ROM Mode Entry command. The device now enters Hidden ROM Mode, allowing Read, Write, Erase and Block Protect to be executed. Write and Erase operations are the same as auto operations except that the device is in Hidden ROM Mode. To protect the hidden ROM area, use the block protection function. The operation of Block Protect here is the same as a normal Block Protect except that V_{IH} rather than V_{ID} is input to $\overline{RESET}$. Once the block has been protected, protection cannot be released, even using the temporary block unprotection function. Use Block Protect carefully. Note that in Hidden ROM Mode, simultaneous operation cannot be performed for BANK3 in top boot type and for BANK0 in bottom boot type.

To exit Hidden ROM Mode, use the Hidden ROM Mode Exit command. This will return the device to Read Mode.

HIDDEN ROM AREA ADDRESS TABLE

TYPE	BOOT BLOCK ARCHITECTURE	BYTE MODE		WORD MODE	
		ADDRESS RANGE	SIZE	ADDRESS RANGE	SIZE
TC58FVM6T2A	TOP BOOT BLOCK	7F0000h~7FFFFFh	64 Kbytes	3F8000h~3FFFFFh	32 Kwords
TC58FVM6B2A	BOTTOM BOOT BLOCK	000000h~00FFFFh	64 Kbytes	000000h~007FFFh	32 Kwords

COMMON FLASH MEMORY INTERFACE (CFI)

The TC58FVM6T2A/B2A conforms to the CFI specifications. To read information from the device, input the Query command followed by the address. In Word Mode DQ8~DQ15 all output 0s. To exit this mode, input the Reset command.

CFI CODE TABLE

ADDRESS A6~A0	DATA DQ15~DQ0	DESCRIPTION
10h 11h 12h	0051h 0052h 0059h	ASCII string "QRY"
13h 14h	0002h 0000h	Primary OEM command set 2: AMD/FJ standard type
15h 16h	0040h 0000h	Address for primary extended table
17h 18h	0000h 0000h	Alternate OEM command set 0: none exists
19h 1Ah	0000h 0000h	Address for alternate OEM extended table
1Bh	0023h	V_{DD} (min) (Write/Erase) DQ7~DQ4: 1 V DQ3~DQ0: 100 mV
1Ch	0036h	V_{DD} (max) (Write/Erase) DQ7~DQ4: 1 V DQ3~DQ0: 100 mV
1Dh	0000h	V_{PP} (min) voltage
1Eh	0000h	V_{PP} (max) voltage
1Fh	0004h	Typical time-out per single byte/word write (2^N μs)
20h	0000h	Typical time-out for minimum size buffer write (2^N μs)
21h	000Ah	Typical time-out per individual block erase (2^N ms)
22h	0000h	Typical time-out for full chip erase (2^N ms)
23h	0005h	Maximum time-out for byte/word write (2^N times typical)
24h	0000h	Maximum time-out for buffer write (2^N times typical)
25h	0004h	Maximum time-out per individual block erase (2^N times typical)
26h	0000h	Maximum time-out for full chip erase (2^N times typical)
27h	0017h	Device Size (2^N byte)
28h 29h	0002h 0000h	Flash device interface description 2: ×8/×16
2Ah 2Bh	0004h 0000h	Maximum number of bytes in multi-byte write (2^N)

ADDRESS A6~A0	DATA DQ15~DQ0	DESCRIPTION
2Ch	0002h	Number of erase block regions within device
2Dh 2Eh 2Fh 30h	0007h 0000h 0020h 0000h	Erase Block Region 1 information Bits 0~15: y = block number Bits 16~31: z = block size (z × 256 bytes)
31h 32h 33h 34h	007Eh 0000h 0000h 0001h	Erase Block Region 2 information
40h 41h 42h	0050h 0052h 0049h	ASCII string "PRI"
43h	0031h	Major version number, ASCII
44h	0031h	Minor version number, ASCII
45h	0000h	Address-Sensitive Unlock 0: Required 1: Not required
46h	0002h	Erase Suspend 0: Not supported 1: For Read-only 2: For Read & Write
47h	0001h	Block Protect 0: Not supported X: Number of blocks per group
48h	0001h	Block Temporary Unprotect 0: Not supported 1: Supported
49h	0004h	Block Protect/Unprotect scheme
4Ah	0001h	Simultaneous operation 0: Not supported 1: Supported
4Bh	0000h	Burst Mode 0: Not supported
4Ch	0001h	Page Mode 0: Not supported 1: Supported
4Dh	0085h	V_{ACC} (min) voltage DQ7~DQ4: 1 V DQ3~DQ0: 100 mV
4Eh	0095h	V_{ACC} (max) voltage DQ7~DQ4: 1 V DQ3~DQ0: 100 mV
4Fh	000Xh	Top/Bottom Boot Block Flag 2: TC58FVM6B2A 3: TC58FVM6T2A
50h	0001h	Program Suspend 0: Not supported 1: Supported

ADDRESS A6~A0	DATA DQ15~DQ0	DESCRIPTION
57h	0004h	Bank Organization 00h: Data at 4Ah is zero X: Number of Banks
58h	00XXh	Bank0 Region information X = Number of blocks in Bank0 TOP: 10h BOTTOM: 17h
59h	00XXh	Bank1 Region information X = Number of blocks in Bank1 TOP: 30h BOTTOM: 30h
5Ah	00XXh	Bank2 Region information X = Number of blocks in Bank2 TOP: 30h BOTTOM: 30h
5Bh	00XXh	Bank3 Region information X = Number of blocks in Bank3 TOP: 17h BOTTOM: 10h

HARDWARE SEQUENCE FLAGS

The TC58FVM6T2A/B2A has a Hardware Sequence flag which allows the device status to be determined during an auto mode operation. The output data is read out using the same timing as that used when $\overline{CE}$ = $\overline{OE}$ = V_{IL} in Read Mode. The RY/$\overline{BY}$ output can be either High or Low.

The device re-enters Read Mode automatically after an auto mode operation has been completed successfully. The Hardware Sequence flag is read to determine the device status and the result of the operation is verified by comparing the read-out data with the original data.

STATUS				DQ7	DQ6	DQ5	DQ3	DQ2	RY/$\overline{BY}$
In Progress	Auto Programming/Auto Page Programming			$\overline{DQ7}$ (4)	Toggle	0	0	1	0
	Read in Program Suspend(1)			Data	Data	Data	Data	Data	High-Z
	In Auto Erase	Erase Hold Time	Selected(2)	0	Toggle	0	0	Toggle	0
			Not-selected(3)	0	Toggle	0	0	1	0
		Auto Erase	Selected	0	Toggle	0	1	Toggle	0
			Not-selected	0	Toggle	0	1	1	0
	In Erase Suspend	Read	Selected	1	1	0	0	Toggle	High-Z
			Not-selected	Data	Data	Data	Data	Data	High-Z
		Programming	Selected	$\overline{DQ7}$ (4)	Toggle	0	0	Toggle	0
			Not-selected	$\overline{DQ7}$ (4)	Toggle	0	0	1	0
Time Limit Exceeded	Auto Programming/Auto Page Programming			$\overline{DQ7}$ (4)	Toggle	1	0	1	0
	Auto Erase			0	Toggle	1	1	NA	0
	Programming in Erase Suspend			$\overline{DQ7}$ (4)	Toggle	1	0	NA	0

Notes: DQ outputs cell data and RY/$\overline{BY}$ goes High-Impedence when the operation has been completed.
DQ0 and DQ1 pins are reserved for future use.
0 is output on DQ0, DQ1 and DQ4.
(1) Data output from an address to which Write is being performed is undefined.
(2) Output when the block address selected for Auto Block Erase is specified and data is read from there. During Auto Chip Erase, all blocks are selected.
(3) Output when a block address not selected for Auto Block Erase of same bank as selected block is specified and data is read from there.
(4) In case of Page program operation is program data of (A0, A1, A2) = (1, 1, 1) in eleventh bus write cycle in word mode. Program data of (A-1, A0, A1, A2) = (1, 1, 1, 1) in nineteenth bus write cycle in byte mode.

DQ7 ($\overline{DATA}$ polling)

During an Auto-Program or auto-erase operation, the device status can be determined using the data polling function. $\overline{DATA}$ polling begins on the rising edge of $\overline{WE}$ in the last bus cycle. In an Auto-Program operation, DQ7 outputs inverted data during the programming operation and outputs actual data after programming has finished. In an auto-erase operation, DQ7 outputs 0 during the Erase operation and outputs 1 when the Erase operation has finished. If an Auto-Program or auto-erase operation fails, DQ7 simply outputs the data.

When the operation has finished, the address latch is reset. Data polling is asynchronous with the $\overline{OE}$ signal.

DQ6 (Toggle bit 1)

The device status can be determined by the Toggle Bit function during an Auto-Program or auto-erase operation. The Toggle bit begins toggling on the rising edge of $\overline{WE}$ in the last bus cycle. DQ6 alternately outputs a 0 or a 1 for each $\overline{OE}$ access while $\overline{CE}$ = V_{IL} while the device is busy. When the internal operation has been completed, toggling stops and valid memory cell data can be read by subsequent reading. If the operation fails, the DQ6 output toggles.

If an attempt is made to execute an Auto Program operation on a protected block, DQ6 will toggle for around 3 µs. It will then stop toggling. If an attempt is made to execute an auto erase operation on a protected block, DQ6 will toggle for around 250 µs. It will then stop toggling. After toggling has stopped the device will return to Read Mode.

DQ5 (internal time-out)

If the internal timer times out during a Program or Erase operation, DQ5 outputs a 1. This indicates that the operation has not been completed within the allotted time.

Any attempt to program a 1 into a cell containing a 0 will fail (see Auto-Program Mode). In this case DQ5 outputs a 1. Either a hardware reset or a software Reset command is required to return the device to Read Mode.

DQ3 (Block Erase timer)

The Block Erase operation starts 50 µs (the Erase Hold Time) after the rising edge of $\overline{WE}$ in the last command cycle. DQ3 outputs a 0 for the duration of the Block Erase Hold Time and a 1 when the Block Erase operation starts. Additional Block Erase commands can only be accepted during the Block Erase Hold Time. Each Block Erase command input within the hold time resets the timer, allowing additional blocks to be marked for erasing. DQ3 outputs a 1 if the Program or Erase operation fails.

DQ2 (Toggle bit 2)

DQ2 is used to indicate which blocks have been selected for Auto Block Erase or to indicate whether the device is in Erase Suspend Mode.

If data is read continuously from the selected block during an Auto Block Erase, the DQ2 output will toggle. Now 1 will be output from non-selected blocks; thus, the selected block can be ascertained. If data is read continuously from the block selected for Auto Block Erase while the device is in Erase Suspend Mode, the DQ2 output will toggle. Because the DQ6 output is not toggling, it can be determined that the device is in Erase Suspend Mode. If data is read from the address to which data is being written during Erase Suspend in Programming Mode, DQ2 will output a 1.

RY/$\overline{BY}$ (READY/$\overline{BUSY}$)

TC58FVM6T2A/B2A has a RY/$\overline{BY}$ signal to indicate the device status to the host processor. A 0 (Busy state) indicates that an Auto-Program or auto-erase operation is in progress. A 1 (Ready state) indicates that the operation has finished and that the device can now accept a new command. RY/$\overline{BY}$ outputs a 0 when an operation has failed.

RY/$\overline{BY}$ outputs a 0 after the rising edge of $\overline{WE}$ in the last command cycle.

During an Auto Block Erase operation, commands other than Erase Suspend are ignored. RY/$\overline{BY}$ outputs a 1 during an Erase Suspend operation. The output buffer for the RY/$\overline{BY}$ pin is an open-drain type circuit, allowing a wired-OR connection. A pull-up resistor must be inserted between V_{DD} and the RY/$\overline{BY}$ pin.

DATA PROTECTION

The TC58FVM6T2A/B2A includes a function which guards against malfunction or data corruption.

Protection against Program/Erase Caused by Low Supply Voltage

To prevent malfunction at power-on or power-down, the device will not accept commands while V_{DD} is below V_{LKO}. In this state, command input is ignored.

If V_{DD} drops below V_{LKO} during an Auto Operation, the device will terminate Auto-Program execution. In this case, Auto operation is not executed again when V_{DD} return to recommended V_{DD} voltage Therefore, command need to be input to execute Auto operation again.

When $V_{DD} > V_{LKO}$, make up countermeasure to be input accurately command in system side please.

Protection against Malfunction Caused by Glitches

To prevent malfunction during operation caused by noise from the system, the device will not accept pulses shorter than 3 ns (Typ.) input on $\overline{WE}$, $\overline{CE}$ or $\overline{OE}$. However, if a glitch exceeding 3 ns (Typ.) occurs and the glitch is input to the device malfunction may occur.

The device uses standard JEDEC commands. It is conceivable that, in extreme cases, system noise may be misinterpreted as part of a command sequence input and that the device will acknowledge it. Then, even if a proper command is input, the device may not operate. To avoid this possibility, clear the Command Register before command input. In an environment prone to system noise, Toshiba recommend input of a software or hardware reset before command input.

Protection against Malfunction at Power-on

To prevent damage to data caused by sudden noise at power-on, when power is turned on with $\overline{WE} = \overline{CE} = V_{IL}$ the device does not latch the command on the first rising edge of $\overline{WE}$ or $\overline{CE}$. Instead, the device automatically Resets the Command Register and enters Read Mode.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RANGE	UNIT
V_{DD}	V_{DD} Supply Voltage	−0.6~4.6	V
V_{IN}	Input Voltage	-0.6~$V_{DD} + 0.5$ ($\leq$ 4.6)(1)	V
V_{DQ}	Input/Output Voltage	-0.6~$V_{DD} + 0.5$ ($\leq$ 4.6)(1)	V
V_{IDH}	Maximum Input Voltage for A9, $\overline{OE}$ and $\overline{RESET}$ (2)	13.0	V
V_{ACCH}	Maximum Input Voltage for $\overline{WP}$/ACC (2)	10.5	V
P_D	Power Dissipation	600	mW
T_{solder}	Soldering Temperature (10s)	260	°C
T_{stg}	Storage Temperature	−55~150	°C
T_{opr}	Operating Temperature	−40~85	°C
I_{OSHORT}	Output Short-Circuit Current(3)	100	mA

(1) This level may undershoot to −2.0 V for periods < 20 ns, and may overshoot to +2.0 V for periods < 20 ns.
(2) Do not apply VID/VACC when the supply voltage is not within the device's recommended operating voltage range.
(3) Outputs should be shorted for no more than one second.
No more than one output should be shorted at a time.

CAPACITANCE (Ta = 25°C, f = 1 MHz)

TSOPI

SYMBOL	PARAMETER	CONDITION	MAX	UNIT
C_{IN}	Input Pin Capacitance	V_{IN} = 0 V	4	pF
C_{OUT}	Output Pin Capacitance	V_{OUT} = 0 V	8	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0 V	8	pF

This parameter is periodically sampled and is not tested for every device.

TFBGA

SYMBOL	PARAMETER	CONDITION	MAX	UNIT
C_{IN}	Input Pin Capacitance	V_{IN} = 0 V	4	pF
C_{OUT}	Output Pin Capacitance	V_{OUT} = 0 V	8	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0 V	9	pF

This parameter is periodically sampled and is not tested for every device.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD}	V_{DD} Supply Voltage	2.3	3.6	V
V_{IH}	Input High-Level Voltage	$0.7 \times V_{DD}$	$V_{DD} + 0.3$	V
V_{IL}	Input Low-Level Voltage	−0.3	$0.2 \times V_{DD}$	V
V_{ID}	High-Level Voltage for A9, $\overline{OE}$ and $\overline{RESET}$	11.4	12.6	V
V_{ACC}	High-Level Voltage for $\overline{WP}$/ACC	8.5	9.5	V
Ta	Operating Temperature	−40	85	°C

DC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_{LI}	Input Leakage Current	$0\ V \le V_{IN} \le V_{DD}$	—	—	±1	µA
I_{LO}	Output Leakage Current	$0\ V \le V_{OUT} \le V_{DD}$	—	—	±1	µA
V_{OH}	Output High Voltage	$I_{OH} = -0.1$ mA	$V_{DD} - 0.4$	—	—	V
		$I_{OH} = -2.5$ mA	$0.85 \times V_{DD}$	—	—	V
V_{OL}	Output Low Voltage	$I_{OL} = 4.0$ mA	—	—	0.4	V
I_{DDO1}	V_{DD} Average Random Read Current	$V_{IN} = V_{IH}/V_{IL}$, $I_{OUT} = 0$ mA $t_{RC} = 100$ ns (MIN)	—	35	55	mA
I_{DDO2}	V_{DD} Average Program Current	$V_{IN} = V_{IH}/V_{IL}$, $I_{OUT} = 0$ mA	—	8	15	mA
I_{DDO3}	V_{DD} Average Erase Current	$V_{IN} = V_{IH}/V_{IL}$, $I_{OUT} = 0$ mA	—	8	15	mA
I_{DDO4}	V_{DD} Average Read-While-Program Current	$V_{IN} = V_{IH}/V_{IL}$, $I_{OUT} = 0$ mA $t_{RC} = 100$ ns (MIN)	—	43	70	mA
I_{DDO5}	V_{DD} Average Read-while-Erase Current	$V_{IN} = V_{IH}/V_{IL}$, $I_{OUT} = 0$ mA $t_{RC} = 100$ ns (MIN)	—	43	70	mA
I_{DDO6}	V_{DD} Average Program-while-Erase-Suspend Current	$V_{IN} = V_{IH}/V_{IL}$, $I_{OUT} = 0$ mA	—	8	15	mA
I_{DDO7}	V_{DD} Average Page Read Current	$V_{IN} = V_{IH}/V_{IL}$, $I_{OUT} = 0$ mA $t_{PRC} = 25$ ns (MIN)	—	1	5	mA
I_{DDO8}	V_{DD} Average Address Increment Read Current(2)	$V_{IN} = V_{IH}/V_{IL}$, $I_{OUT} = 0$ mA $t_{RC} = 100$ ns (MIN) $t_{PRC} = 25$ns (MIN)	—	5	11	mA
I_{DDS1}	V_{DD} Standby Current	$\overline{CE} = \overline{RESET} = V_{DD}$ or $\overline{RESET} = V_{SS}$	—	2	10	µA
I_{DDS2}	V_{DD} Standby Current (Automatic Sleep Mode(1))	$V_{IH} = V_{DD}$ $V_{IL} = V_{SS}$	—	2	10	µA
I_{ID}	High-Voltage Input Current for A9, $\overline{OE}$ and $\overline{RESET}$	$11.4\ V \le V_{ID} \le 12.6\ V$	—	—	35	µA
I_{ACC}	High-Voltage Input Current for $\overline{WP}$/ACC	$8.5\ V \le V_{ACC} \le 9.5\ V$	—	—	20	mA
V_{LKO}	Low-V_{DD} Lock-out Voltage	—	1.5	—	2.0	V

(1) The device enters Automatic Sleep Mode in which the address remains fixed for during 150 ns.

(2) $(I_{DDO1} + I_{DDO7} \times 7)/8$words

AC TEST CONDITIONS

PARAMETER	CONDITION
Input Pulse Level	V_{DD}, 0.0 V
Input Pulse Rise and Fall Time (10%~90%)	5 ns
Timing Measurement Reference Level (input)	VDD/2, VDD/2
Timing Measurement Reference Level (output)	VDD/2, VDD/2
Output Load	C_L (100 pF) + 1 TTL Gate/C_L (30 pF) + 1 TTL Gate

AC CHARACTERISTICS AND OPERATING CONDITIONS

READ CYCLE

	Product name	TC58FVM6T2A/B2A								
	VDD voltage (V)	VDD = 2.7-3.6 V				VDD = 2.3-3.6V				UNIT
	Output load capacitance (CL)	30 pF		100 pF		30 pF		100 pF		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	65	—	70	—	70	—	75	—	ns
t_{PRC}	Page Read Cycle Time	25	—	30	—	30	—	35	—	ns
t_{ACC}	Address Access Time	—	65	—	70	—	70	—	75	ns
t_{CE}	$\overline{CE}$ Access Time	—	65	—	70	—	70	—	75	ns
t_{OE}	$\overline{OE}$ Access Time	—	25	—	30	—	30	—	35	ns
t_{PACC}	Page Access Time	—	25	—	30	—	30	—	35	ns
t_{OEH}	$\overline{OE}$ High-Level Hold Time (read)	0	—	0	—	0	—	0	—	ns
t_{CEE}	$\overline{CE}$ to Output Low-Z	0	—	0	—	0	—	0	—	ns
t_{OEE}	$\overline{OE}$ to Output Low-Z	0	—	0	—	0	—	0	—	ns
t_{OH}	Output Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{DF1}	$\overline{CE}$ to Output High-Z	—	25	—	25	—	25	—	25	ns
t_{DF2}	$\overline{OE}$ to Output High-Z	—	25	—	25	—	25	—	25	ns

BLOCK PROTECT

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{VPT}	V_{ID} Transition Time	4	—	μs
t_{VPS}	V_{ID} Set-up Time	4	—	μs
t_{CESP}	$\overline{CE}$ Set-up Time	4	—	μs
t_{VPH}	$\overline{OE}$ Hold Time	4	—	μs
t_{PPLH}	$\overline{WE}$ Low-Level Hold Time	100	—	μs

PROGRAM AND ERASE CHARACTERISTICS

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
t_{PPW}	Auto-Program Time (Byte Mode)	—	8	300	μs
	Auto-Program Time (Word Mode)	—	11	300	μs
t_{PPAW}	Auto-Page program time	—	45	2400	μs
t_{PCEW}	Auto Chip Erase Time(1)	—	95	1350	s
t_{PBEW}	Auto Block Erase Time(1)	—	0.7	10(2)	s
t_{EW}	Erase/Program Cycle	10^5	—	—	Cycles

(1) Auto Chip Erase Time and Auto Block Erase Time include internal pre program time.

(2) Minimum interval between resume and the following suspend command is 8 ms. If it's shorter than 8 ms, auto block erase time is expand more than maximum (10 s).

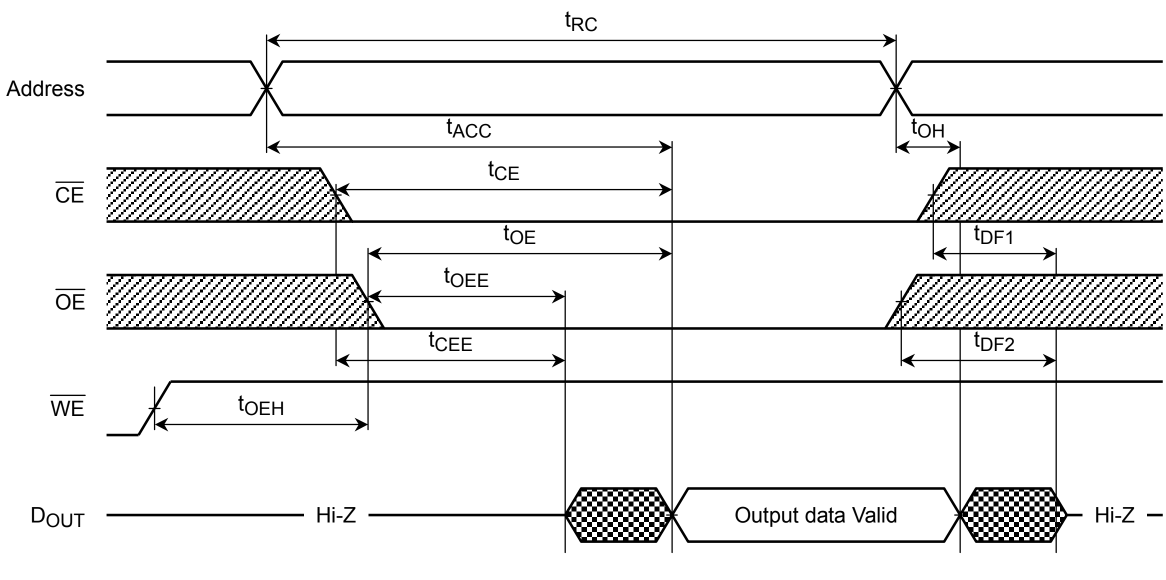
COMMAND WRITE/PROGRAM/ERASE CYCLE

SYMBOL	PARAMETER			UNIT
		MIN	MAX	
t_{CMD}	Command Write Cycle Time	60	—	ns
t_{AS}	Address Set-up Time/ $\overline{BYTE}$ Set-up Time	0	—	ns
t_{AH}	Address Hold Time/ $\overline{BYTE}$ Hold Time	30	—	ns
t_{DS}	Data Set-up Time	30	—	ns
t_{DH}	Data Hold Time	0	—	ns
t_{WELH}	$\overline{WE}$ Low-Level Hold Time ($\overline{WE}$ Control)	30	—	ns
t_{WEHH}	$\overline{WE}$ High-Level Hold Time ($\overline{WE}$ Control)	20	—	ns
t_{CES}	$\overline{CE}$ Set-up Time to $\overline{WE}$ Active ($\overline{WE}$ Control)	0	—	ns
t_{CEH}	$\overline{CE}$ Hold Time from $\overline{WE}$ High Level ($\overline{WE}$ Control)	0	—	ns
t_{CELH}	$\overline{CE}$ Low-Level Hold Time ($\overline{CE}$ Control)	30	—	ns
t_{CEHH}	$\overline{CE}$ High-Level Hold Time ($\overline{CE}$ Control)	20	—	ns
t_{WES}	$\overline{WE}$ Set-up time to $\overline{CE}$ Active ($\overline{CE}$ Control)	0	—	ns
t_{WEH}	$\overline{WE}$ Hold Time from $\overline{CE}$ High Level ($\overline{CE}$ Control)	0	—	ns
t_{OES}	$\overline{OE}$ Set-up Time	0	—	ns
t_{OEHP}	$\overline{OE}$ Hold Time (Toggle, Data Polling)	10	—	ns
t_{OEHT}	$\overline{OE}$ High-Level Hold Time (Toggle)	20	—	ns
t_{CEHT}	$\overline{CE}$ High-Level Hold Time (Toggle)	20	—	ns
t_{AHT}	Address Hold Time (Toggle)	0	—	ns
t_{AST}	Address Set-up Time (Toggle)	0	—	ns
t_{BEH}	Erase Hold Time	50	—	μs
t_{VDS}	V_{DD} Set-up Time	500	—	μs
t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay	—	90	ns
	Program/Erase Valid to RY/$\overline{BY}$ Delay during Suspend Mode	—	300	ns
t_{RP}	$\overline{RESET}$ Low-Level Hold Time	500	—	ns
t_{READY}	$\overline{RESET}$ Low-Level to Read Mode	—	20	μs
t_{RB}	RY/$\overline{BY}$ Recovery Time	0	—	ns
t_{RH}	$\overline{RESET}$ Recovery Time	50	—	ns
t_{CEBTS}	$\overline{CE}$ Set-up time $\overline{BYTE}$ Transition	5	—	ns
t_{BTD}	$\overline{BYTE}$ to Output High-Z	—	30	ns
t_{SUSP}	Program Suspend Command to Suspend Mode	—	1.6	μs
t_{SUSPA}	Page Program Suspend Command to Suspend Mode	—	2.0	μs
t_{RESP}	Program Resume Command to Program Mode	—	1	μs
t_{SUSE}	Erase Suspend Command to Suspend Mode	—	15	μs
t_{RESE}	Erase Resume Command to Erase Mode	—	1	μs

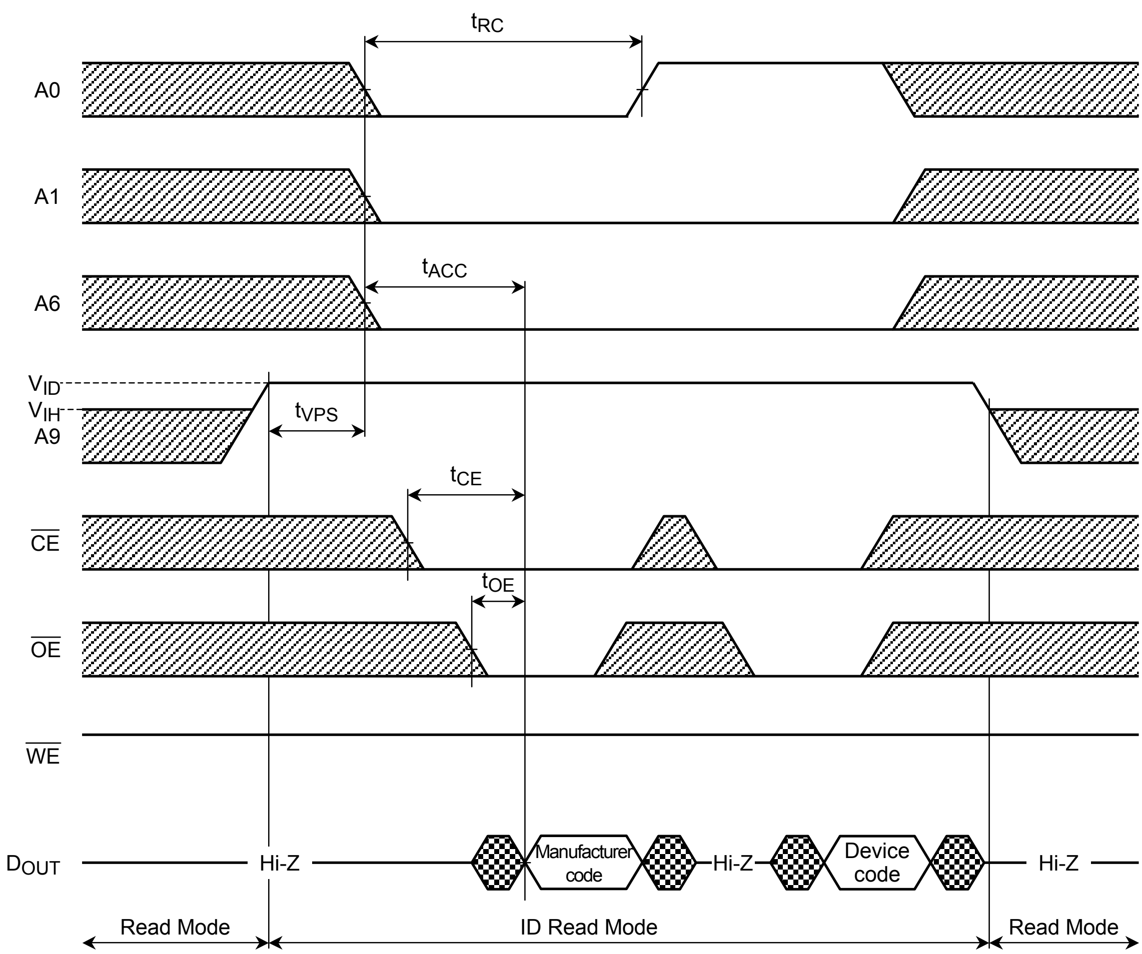
TIMING DIAGRAMS

V_{IH} or V_{IL} Data invalid

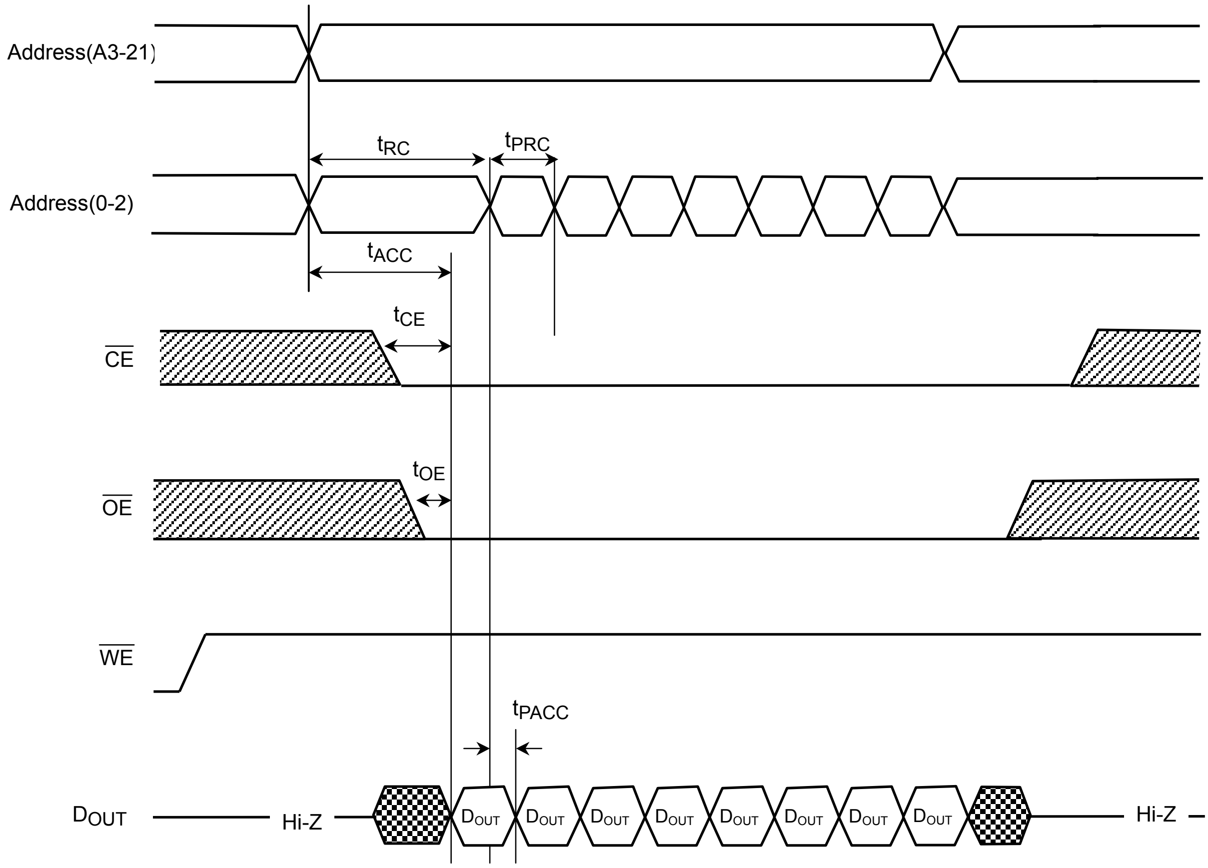
Read/ID Read Operation



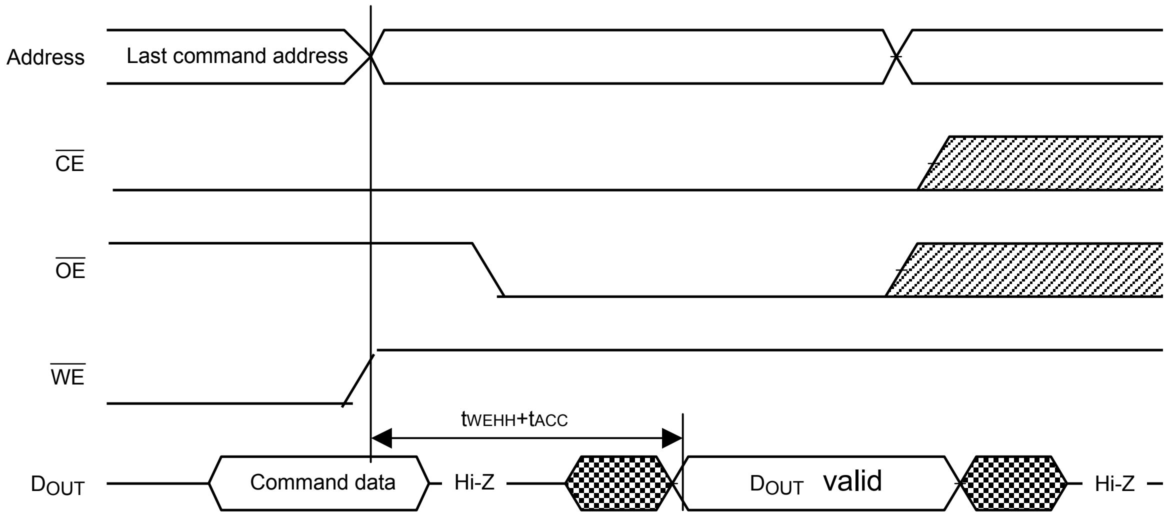
ID Read Operation (apply V_{ID} to A9)



Page Read Operation



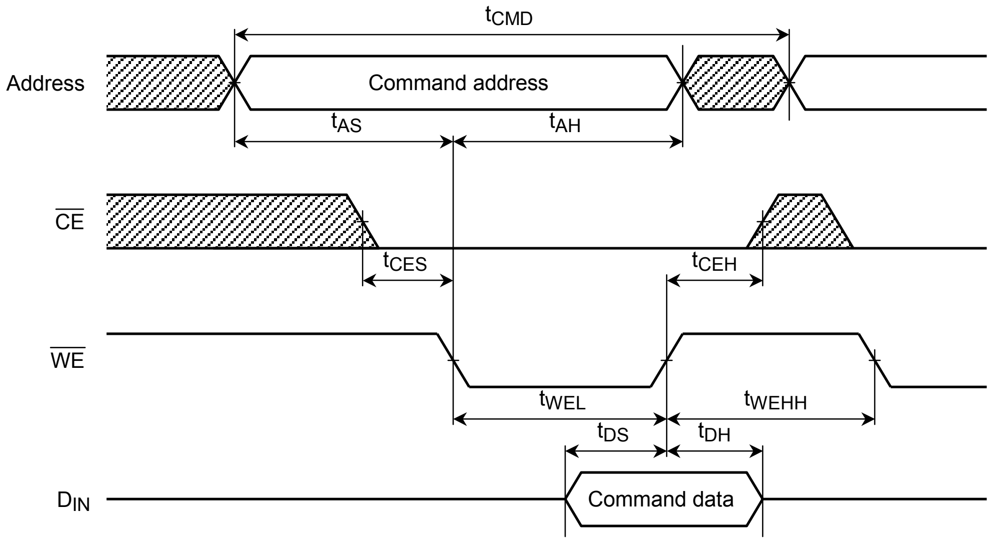
Read after command input (Only Hidden Rom/CFI Read)



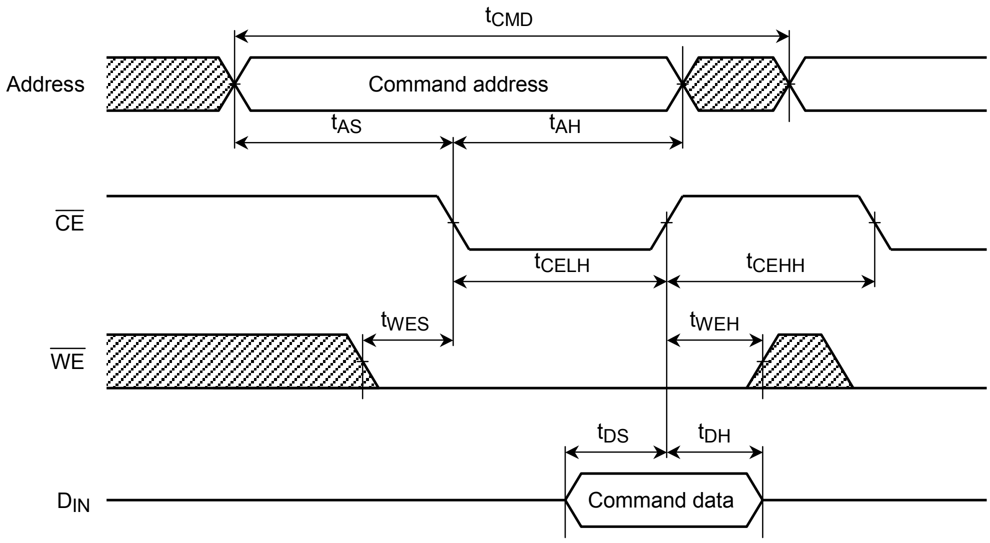
Command Write Operation

This is the timing of the Command Write Operation. The timing which is described in the following pages is essentially the same as the timing shown on this page.

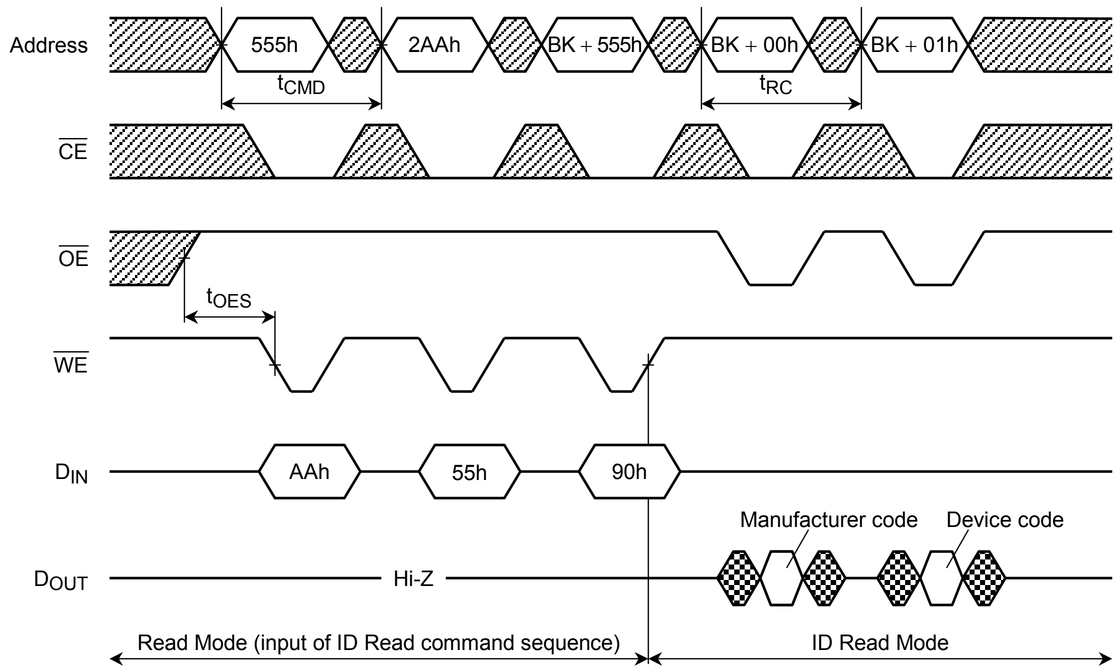
- $\overline{\mathrm{WE}}$ Control



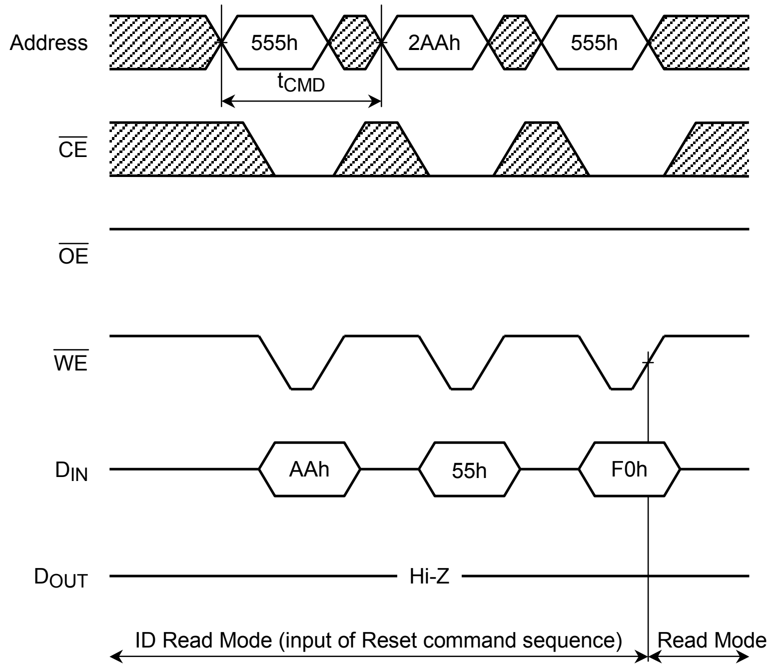
- $\overline{\mathrm{CE}}$ Control



ID Read Operation (input command sequence)

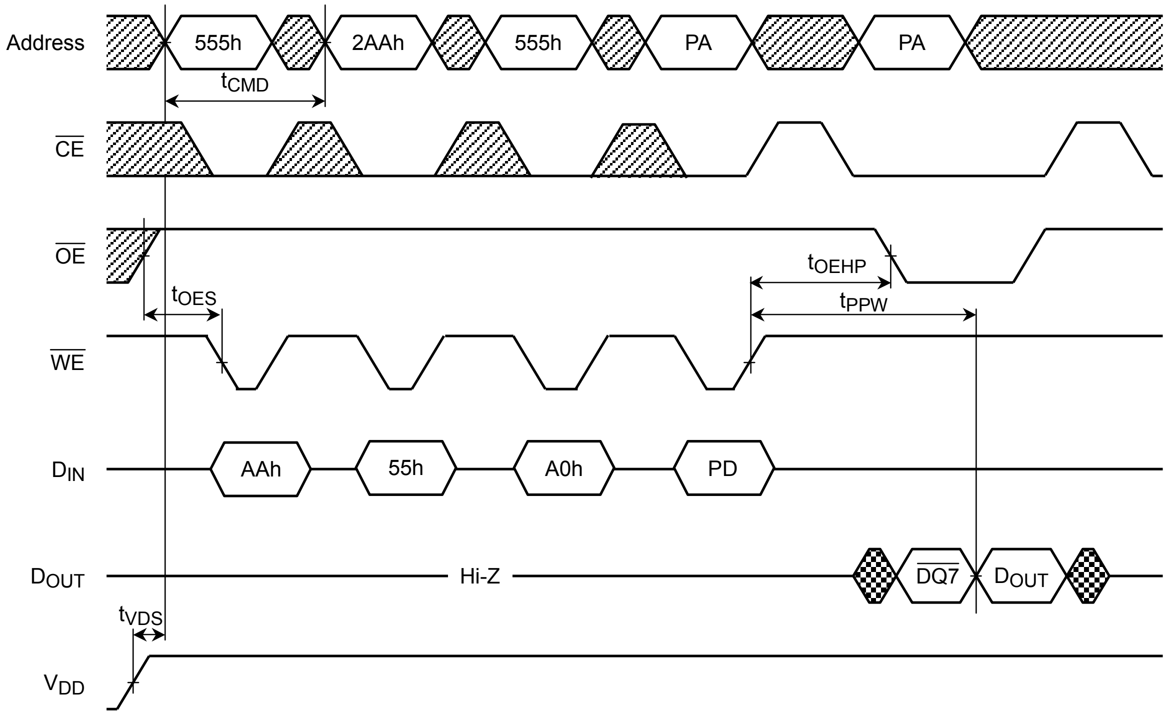


(Continued)



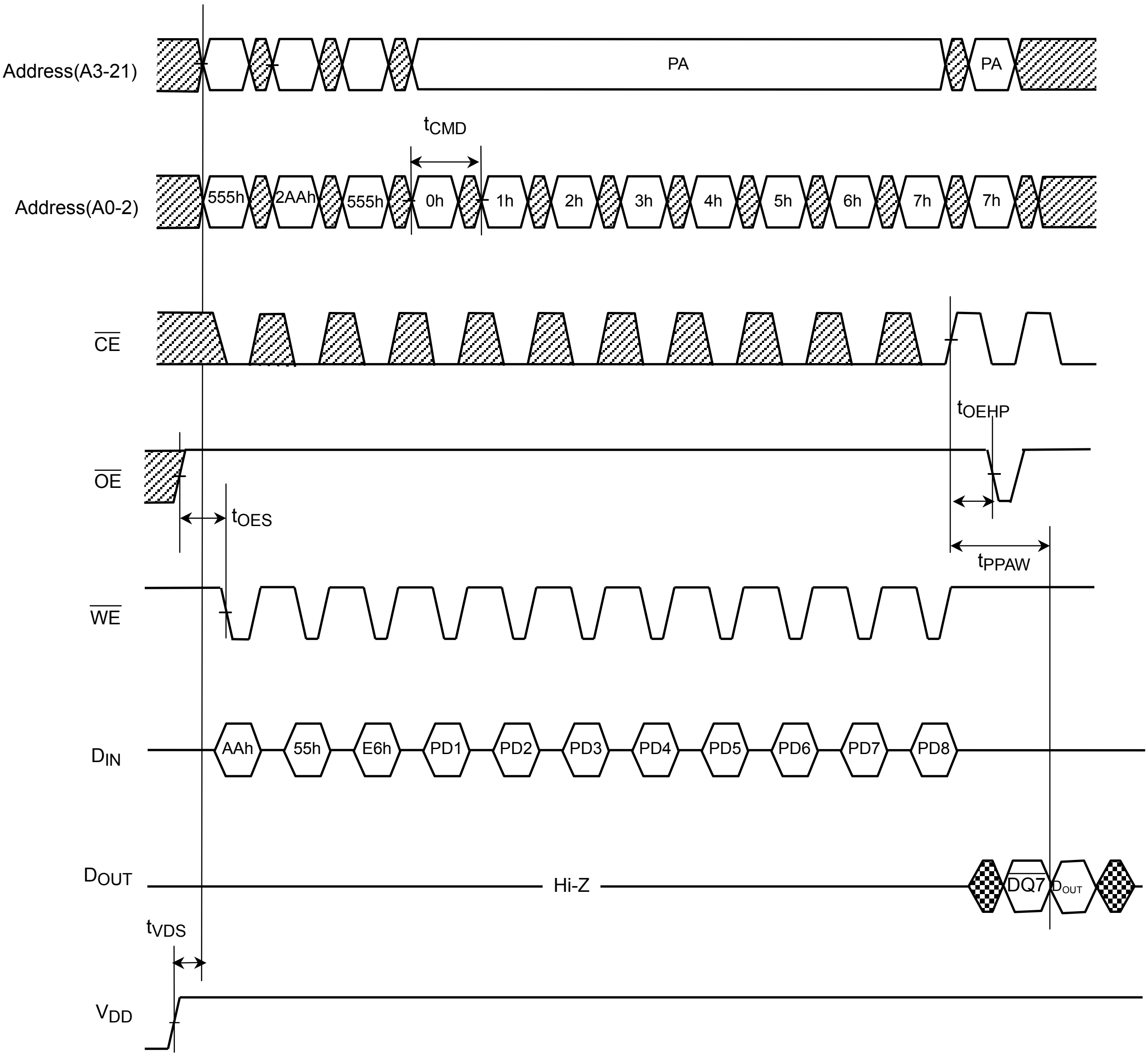
Note: Word Mode address shown.
BK: Bank address

Auto-Program Operation ($\overline{WE}$ Control)



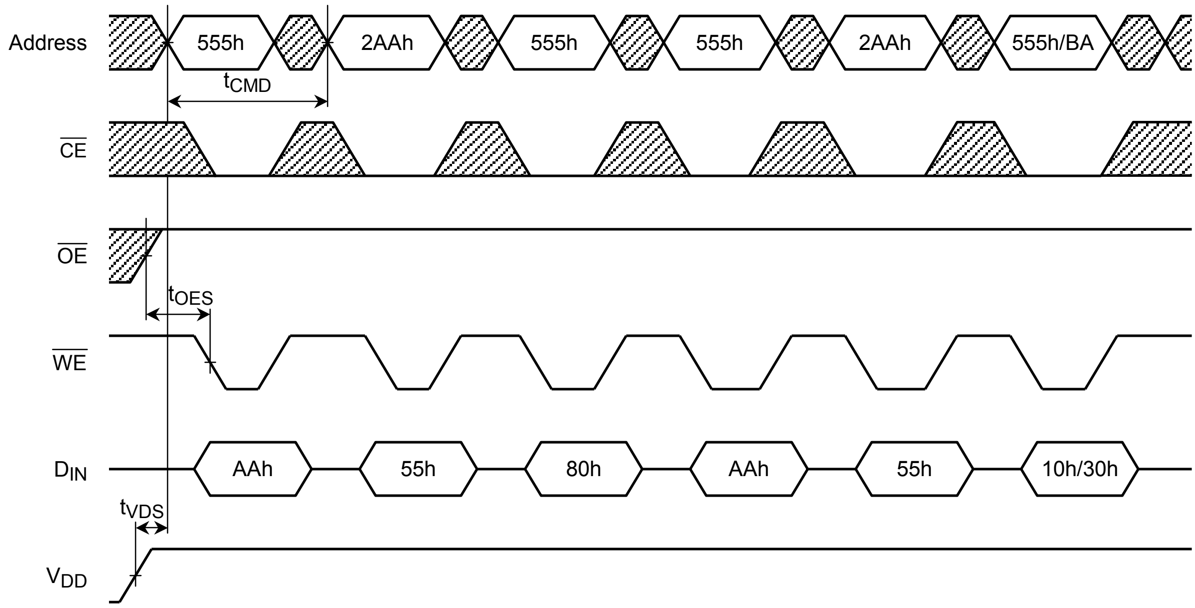
Note: Word Mode address shown.
PA: Program address
PD: Program data

Auto Page Program Operation ($\overline{WE}$ Control)



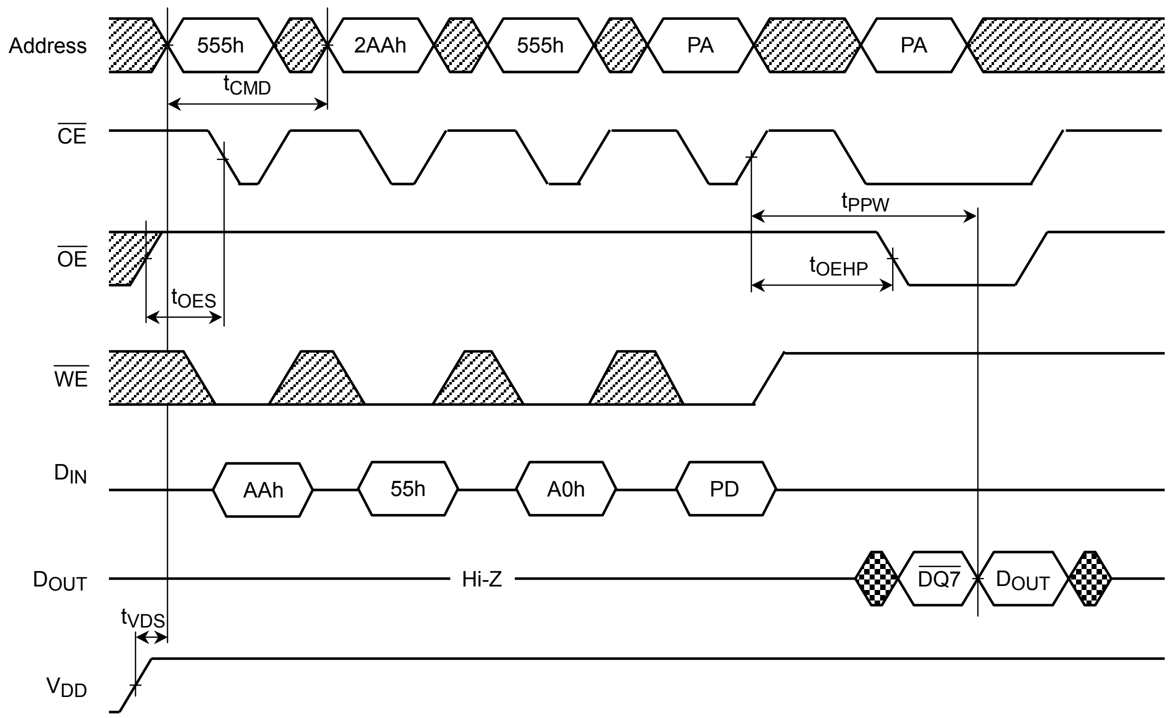
Note: Word Mode address shown.
PA: Program address
PD: Program Data

Auto Chip Erase/Auto Block Erase Operation ($\overline{WE}$ Control)



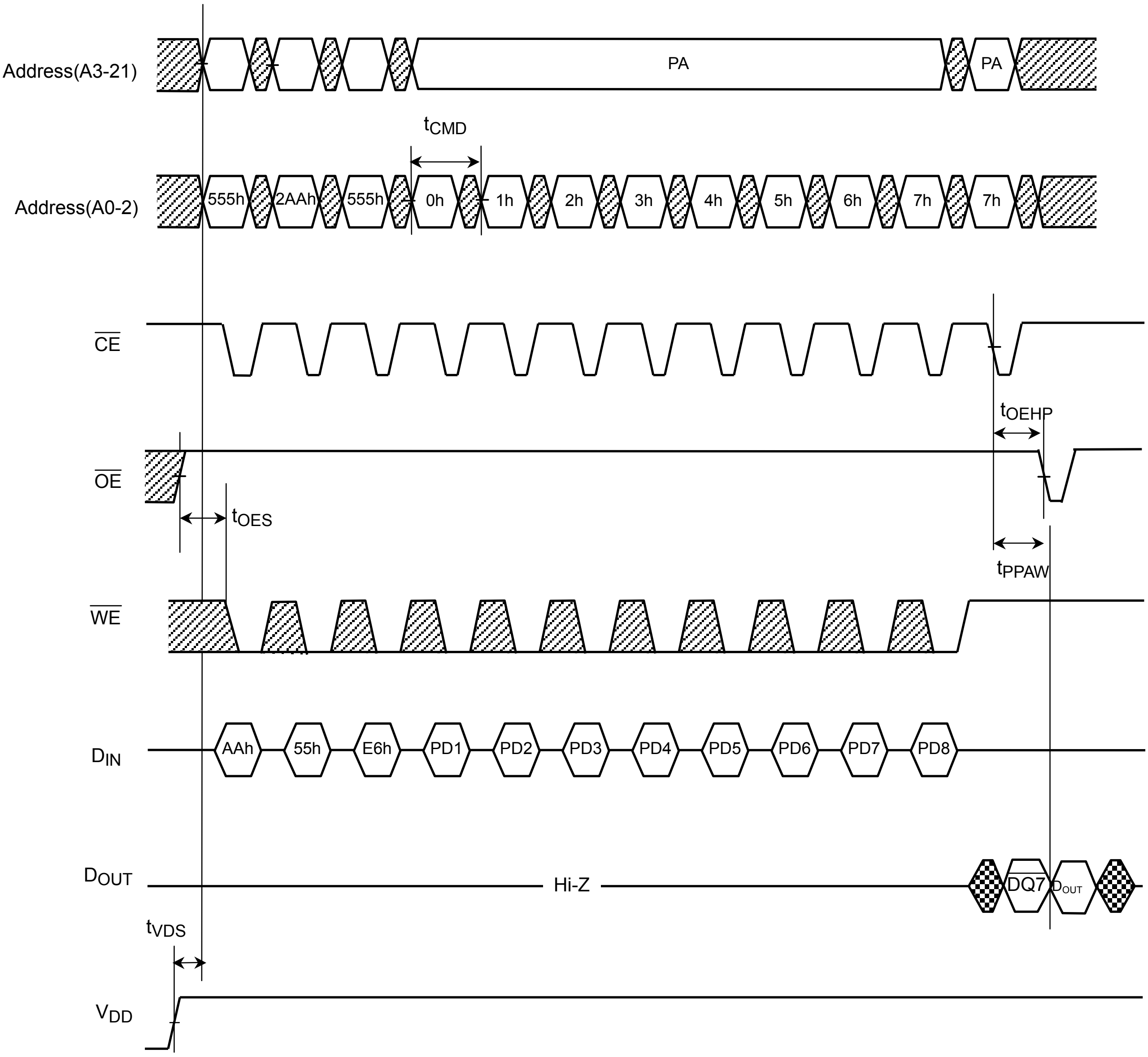
Note: Word Mode address shown.
BA: Block address for Auto Block Erase operation

Auto-Program Operation ($\overline{CE}$ Control)



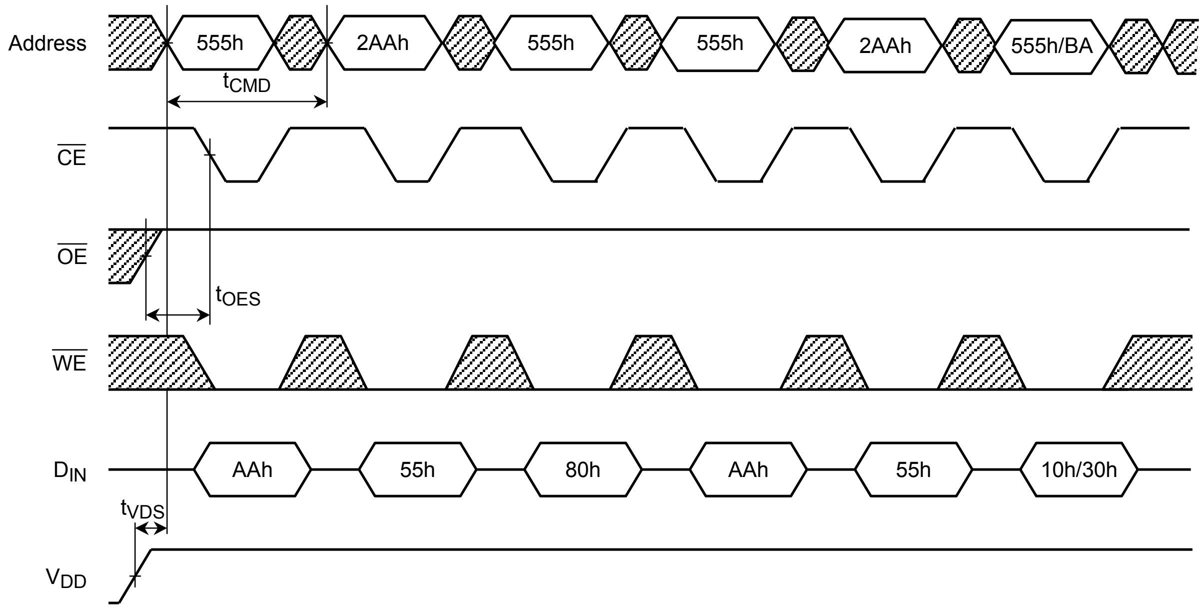
Note: Word Mode address shown.
PA: Program address
PD: Program data

Auto Page Program Operation ($\overline{CE}$ Control)



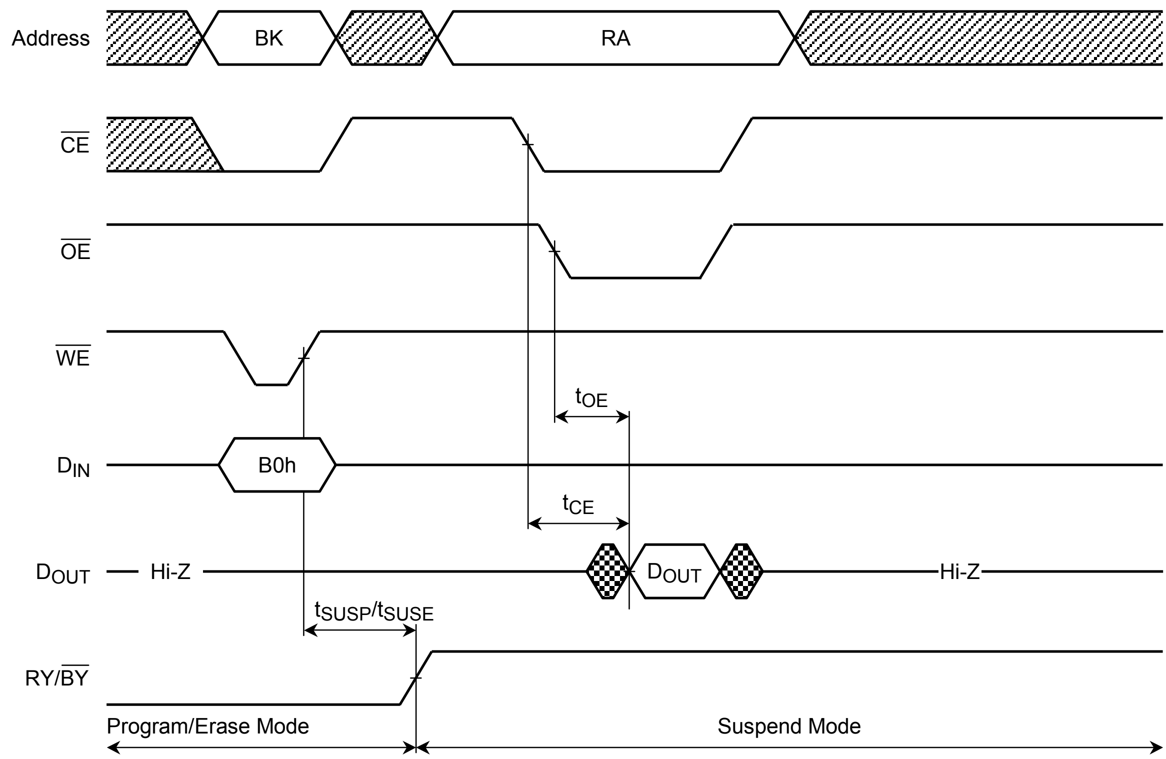
Note: Word Mode address shown.
PA: Program address
PD: Program data

Auto Chip Erase/Auto Block Erase Operation ($\overline{CE}$ Control)



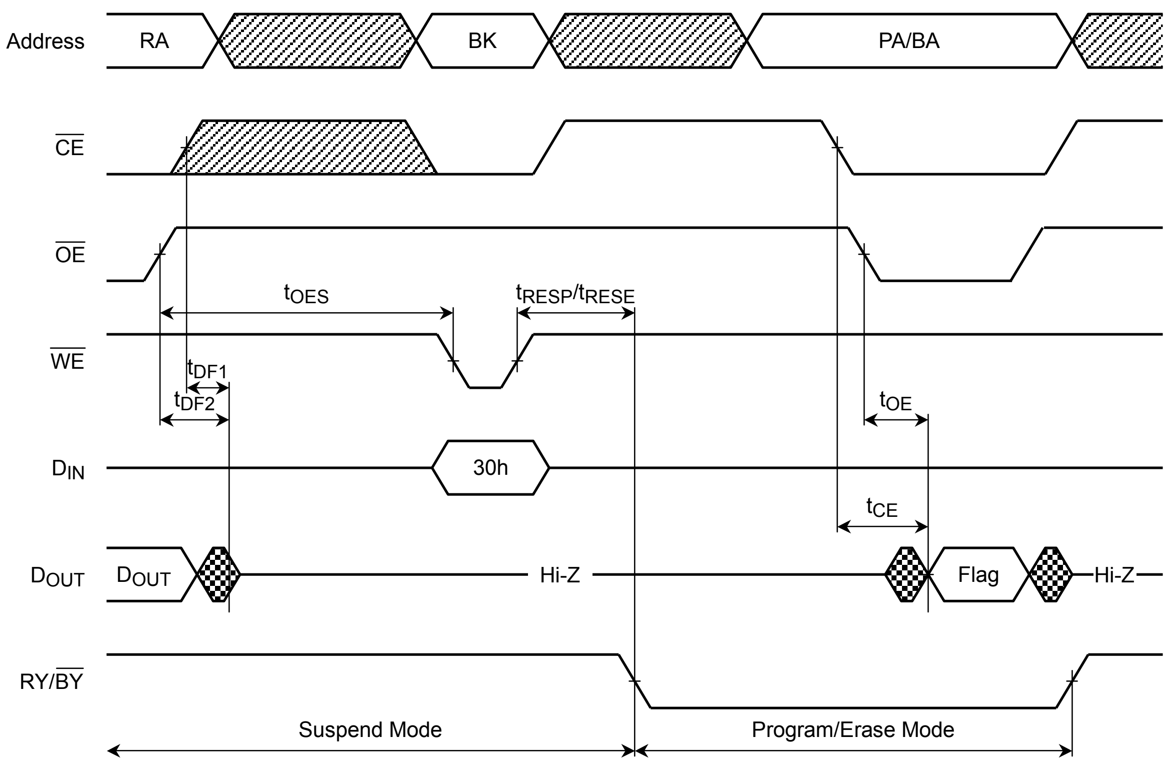
Note: Word Mode address shown.
BA: Block address for Auto Block Erase operation

Program/Erase Suspend Operation



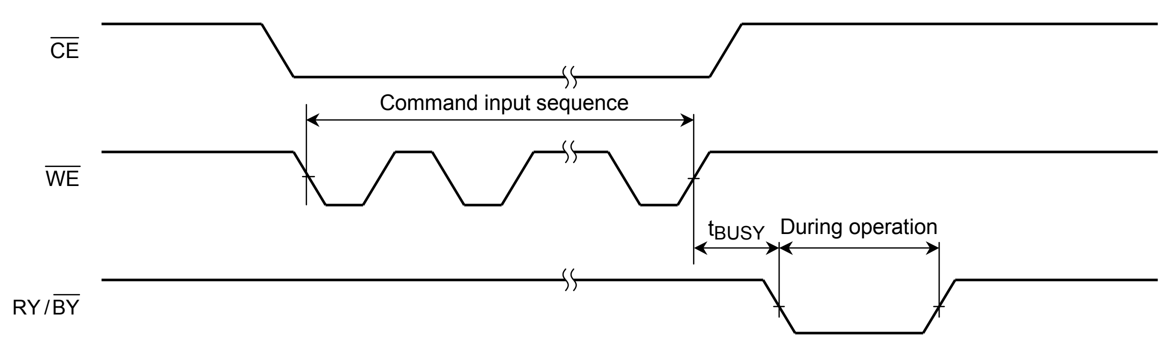
RA: Read address

Program/Erase Resume Operation

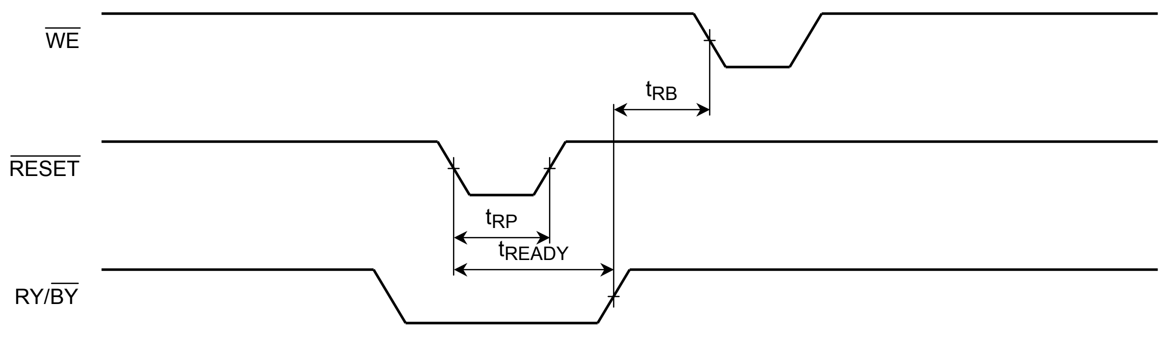


PA: Program address
BK: Bank address
BA: Block address
RA: Read address
Flag: Hardware Sequence flag

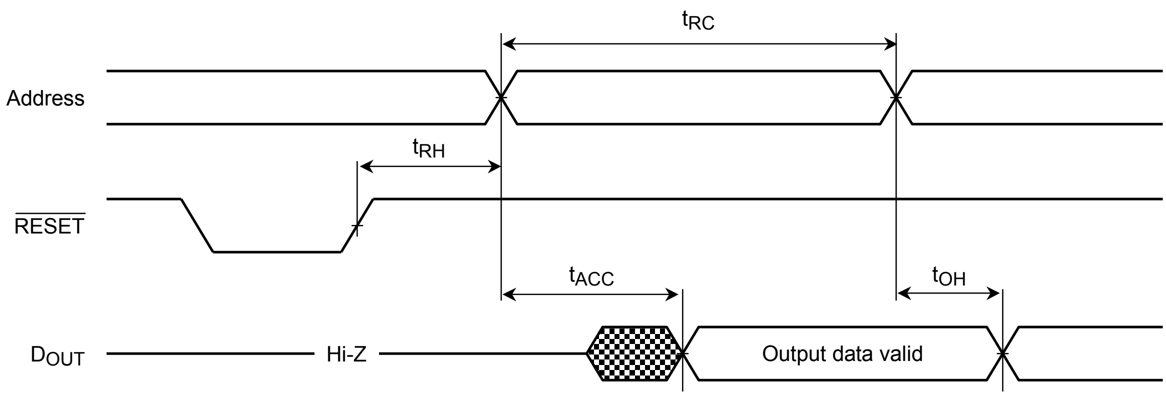
RY/$\overline{BY}$ during Auto Program/Erase Operation



Hardware Reset Operation

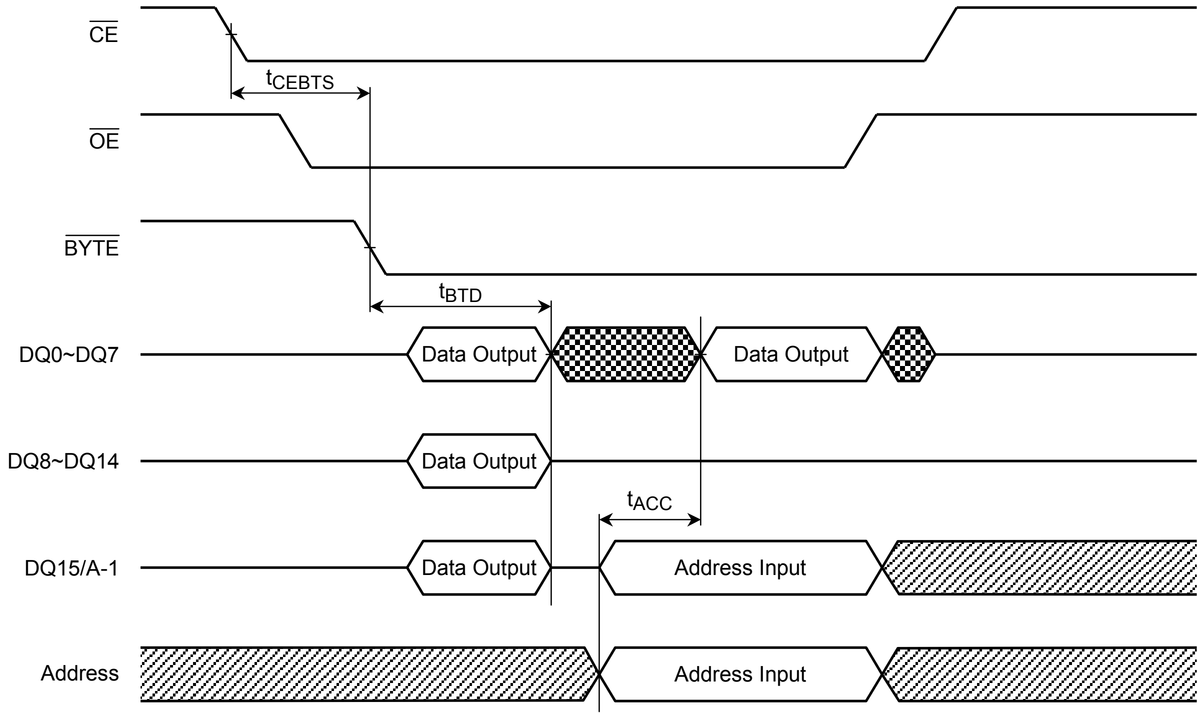


Read after $\overline{RESET}$

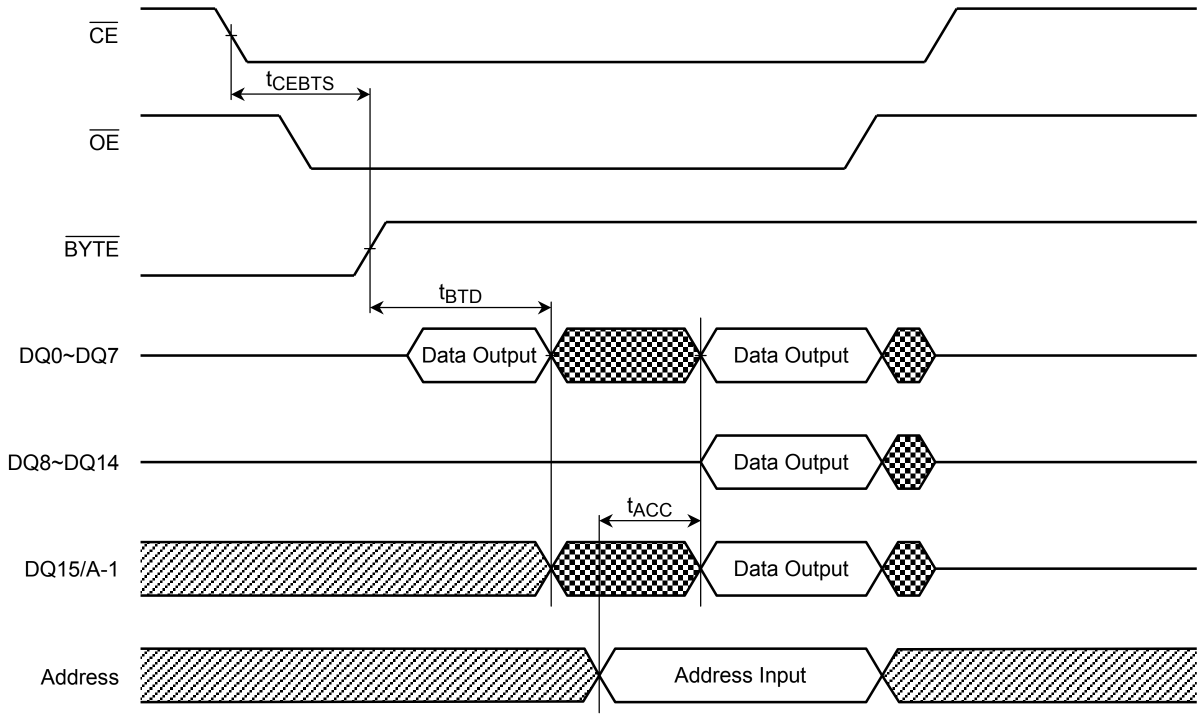


$\overline{\text{BYTE}}$ during Read Operation

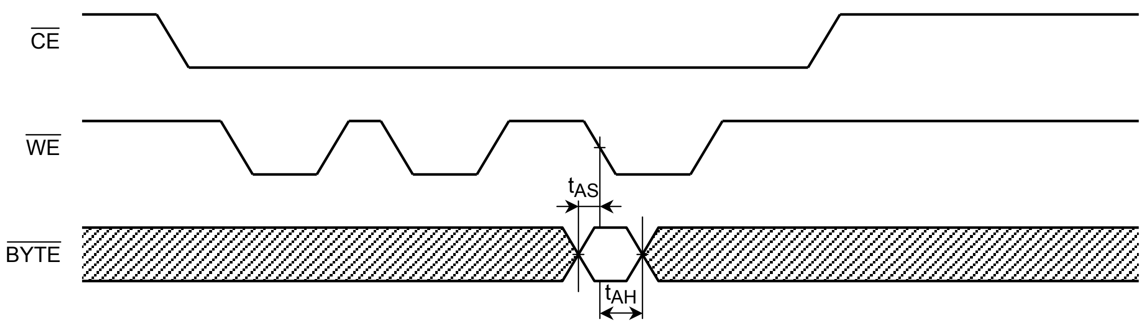
- Word → Byte



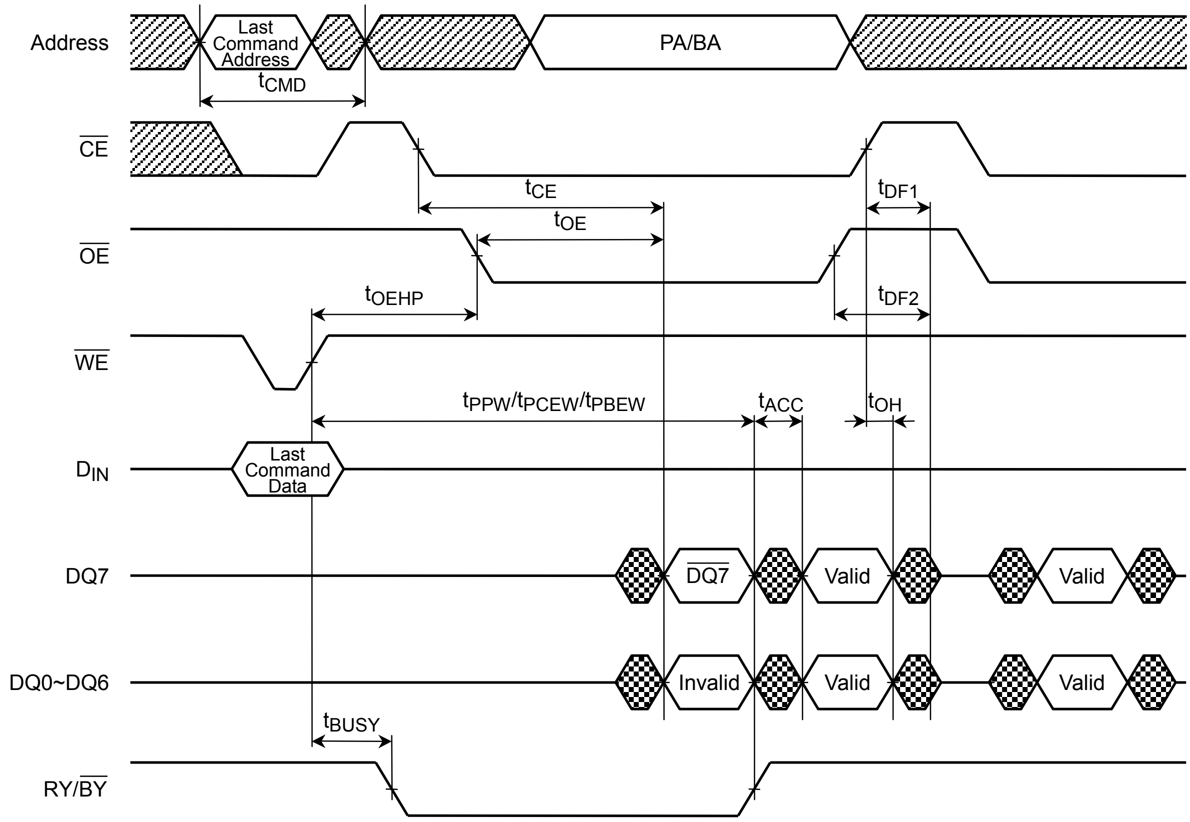
- Byte → Word



$\overline{\text{BYTE}}$ during Write Operation

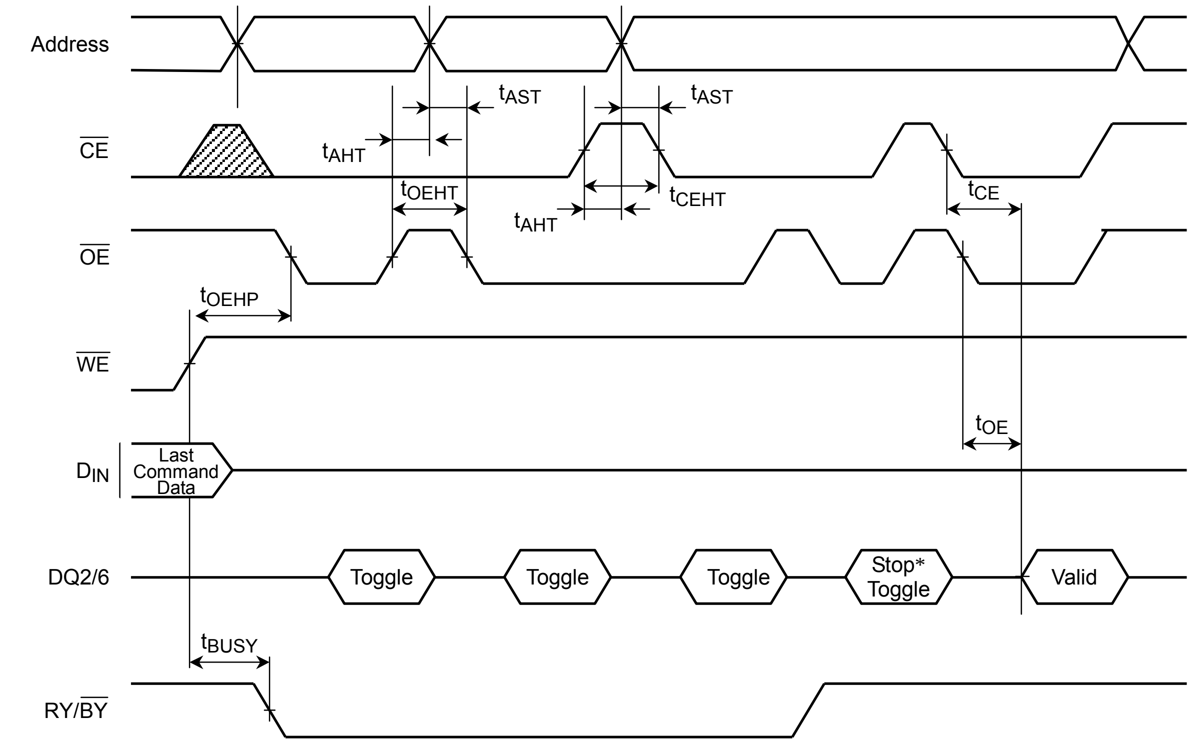


Hardware Sequence Flag ($\overline{DATA}$ Polling)



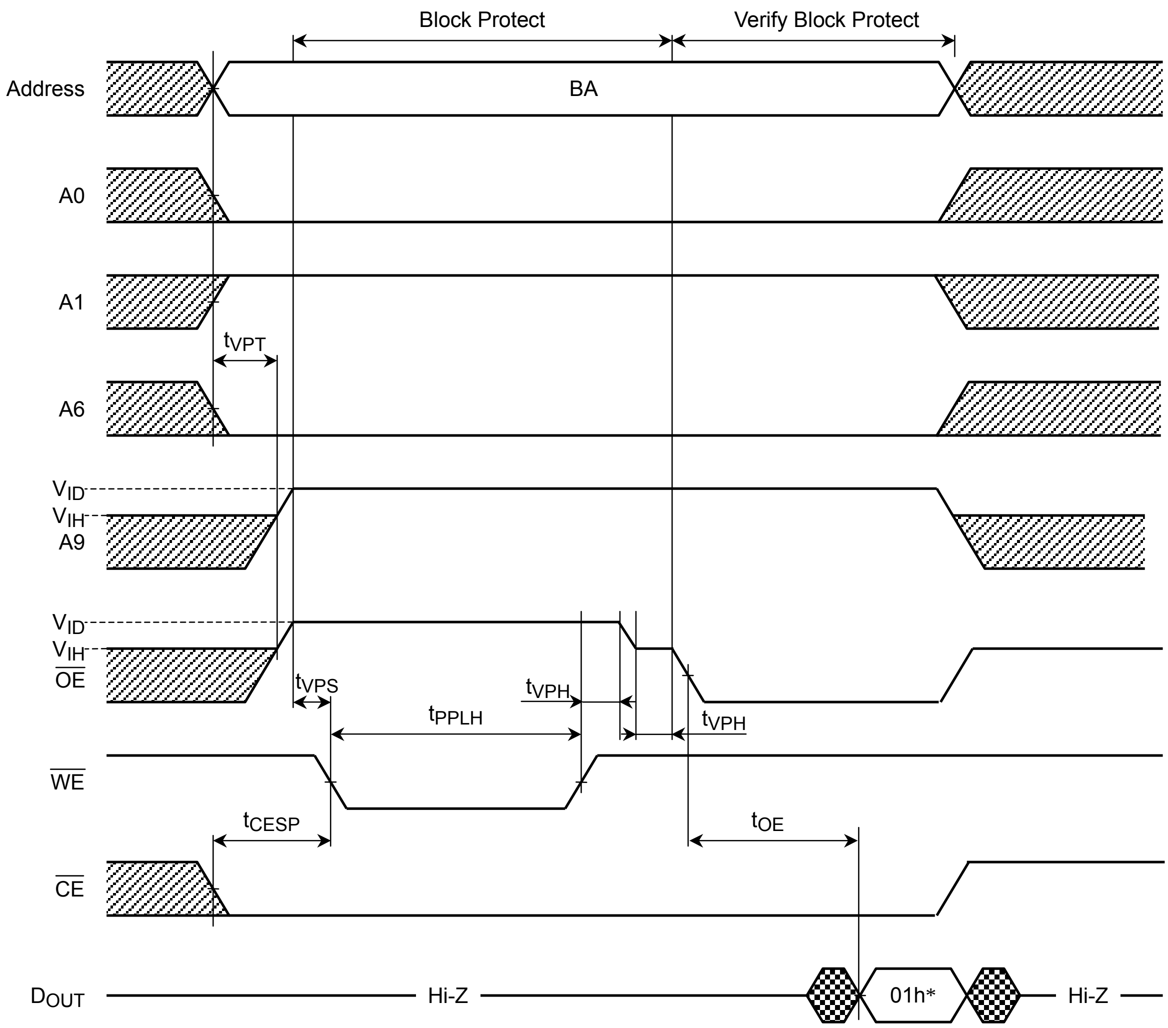
PA: Program address
BA: Block address

Hardware Sequence Flag (Toggle bit)



*DQ2/DQ6 stops toggling when auto operation has been completed.

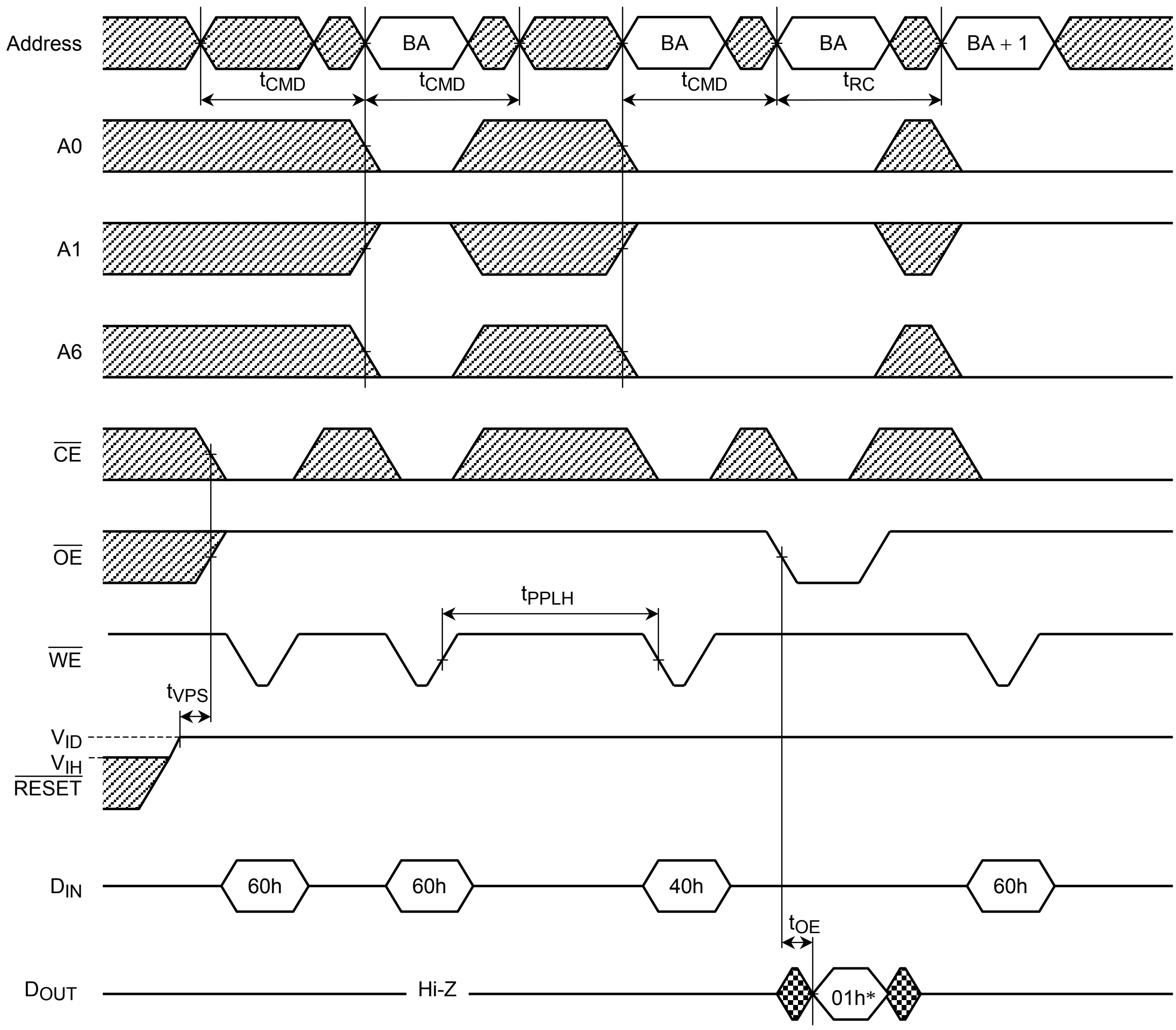
Block Protect 1 Operation



BA: Block address

*: 01H indicates that block is protected.

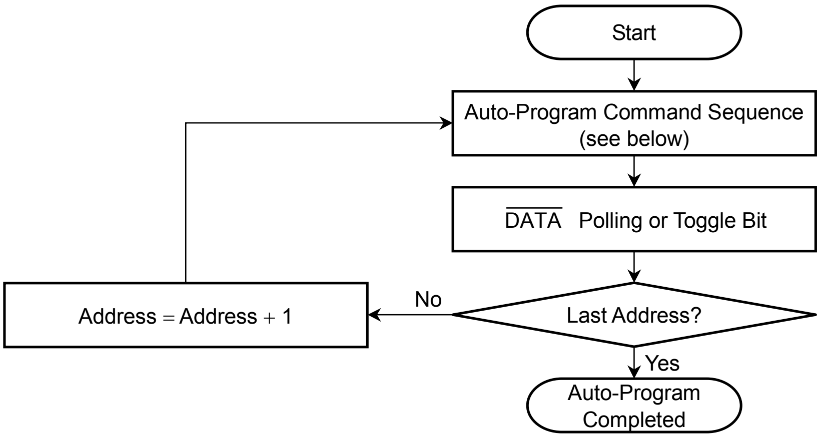
Block Protect 2 Operation



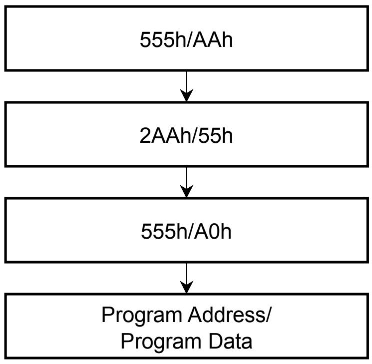
BA: Block address
BA + 1: Address of next block
*: 01h indicates that block is protected.

FLOWCHARTS

Auto-Program

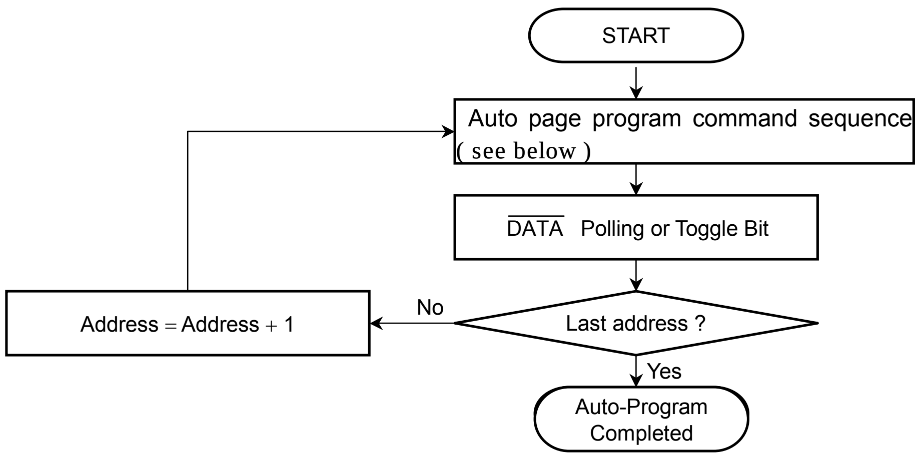


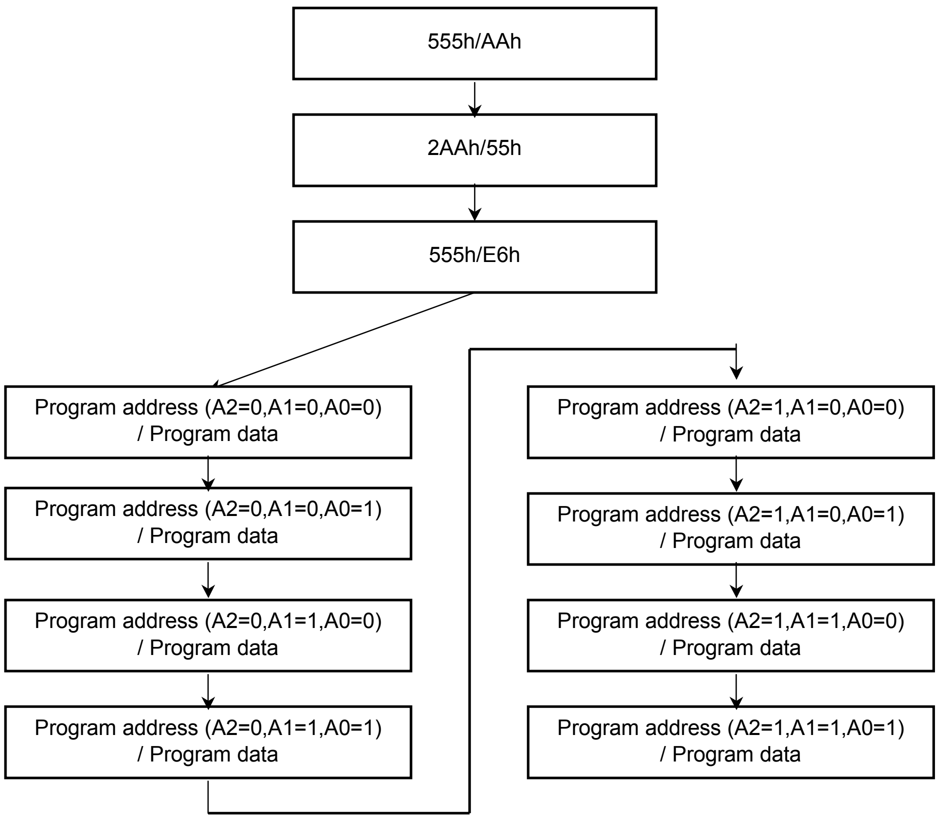
Auto-Program Command Sequence (address/data)



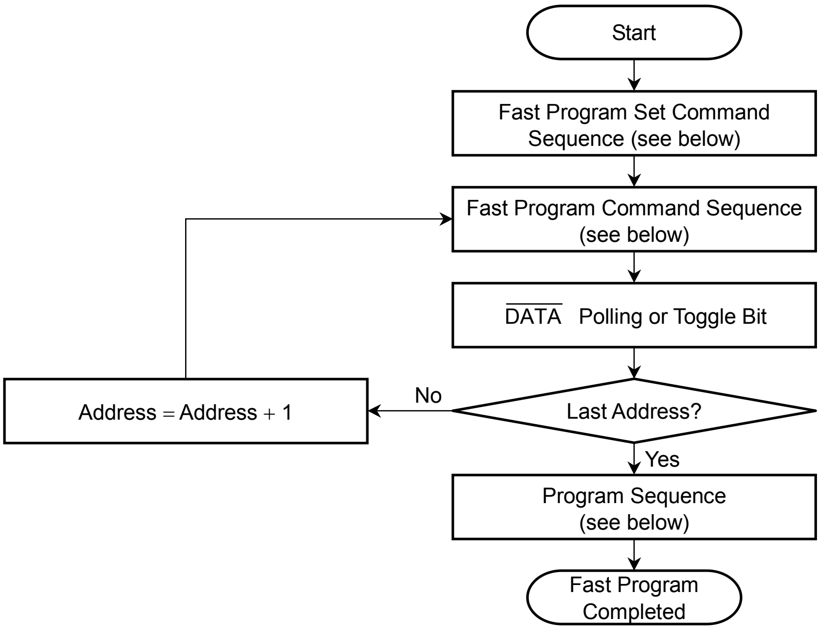
Note: The above command sequence takes place in Word Mode.

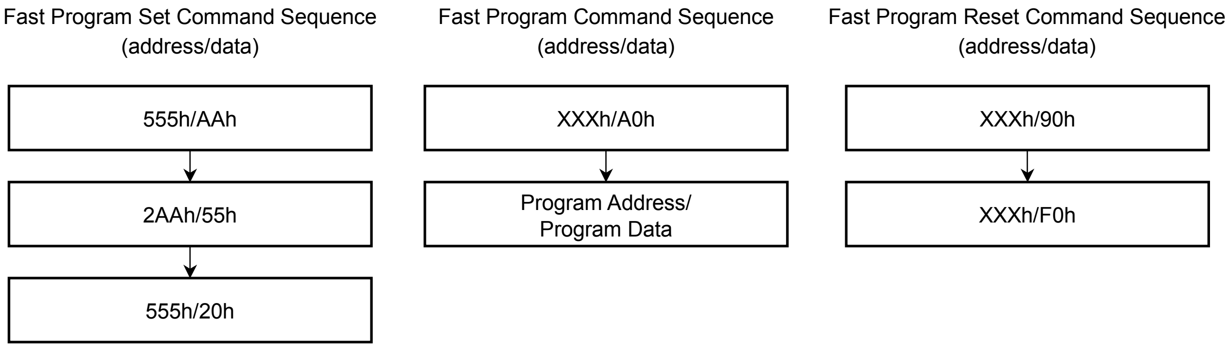
Auto-Page Program



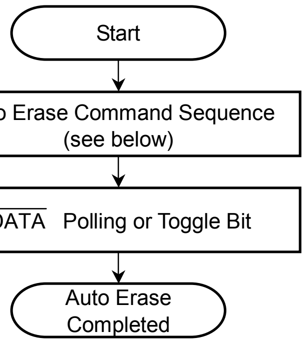


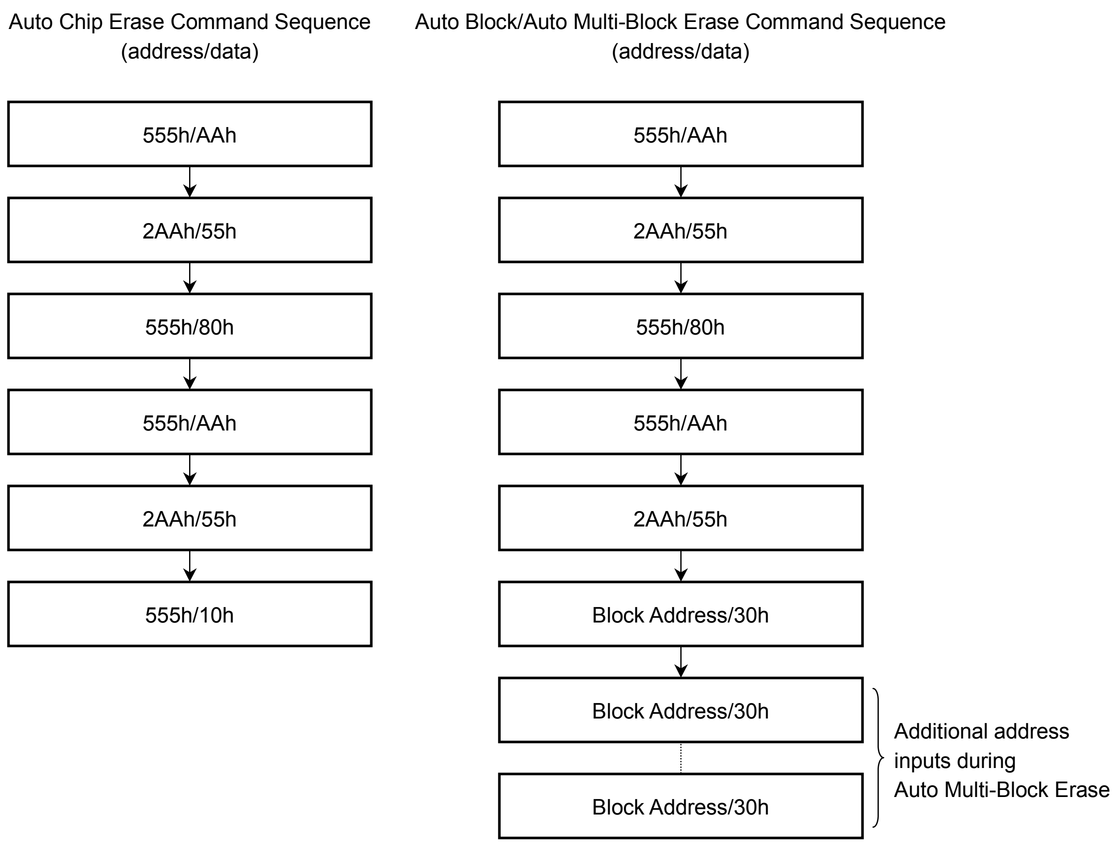
Fast Program





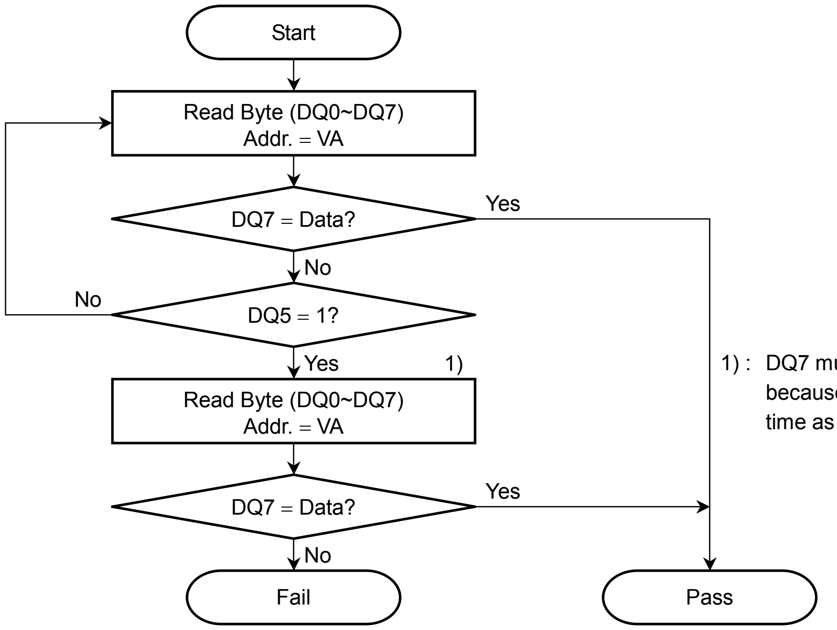
Auto Erase





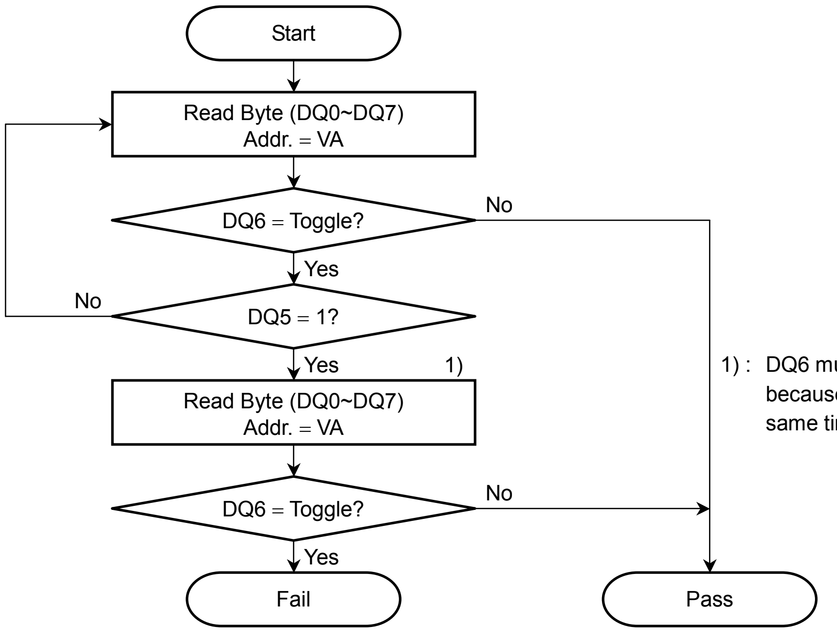
Note: The above command sequence takes place in Word Mode.

DQ7 $\overline{\text{DATA}}$ Polling



1) : DQ7 must be rechecked even if DQ5 = 1 because DQ7 may change at the same time as DQ5.

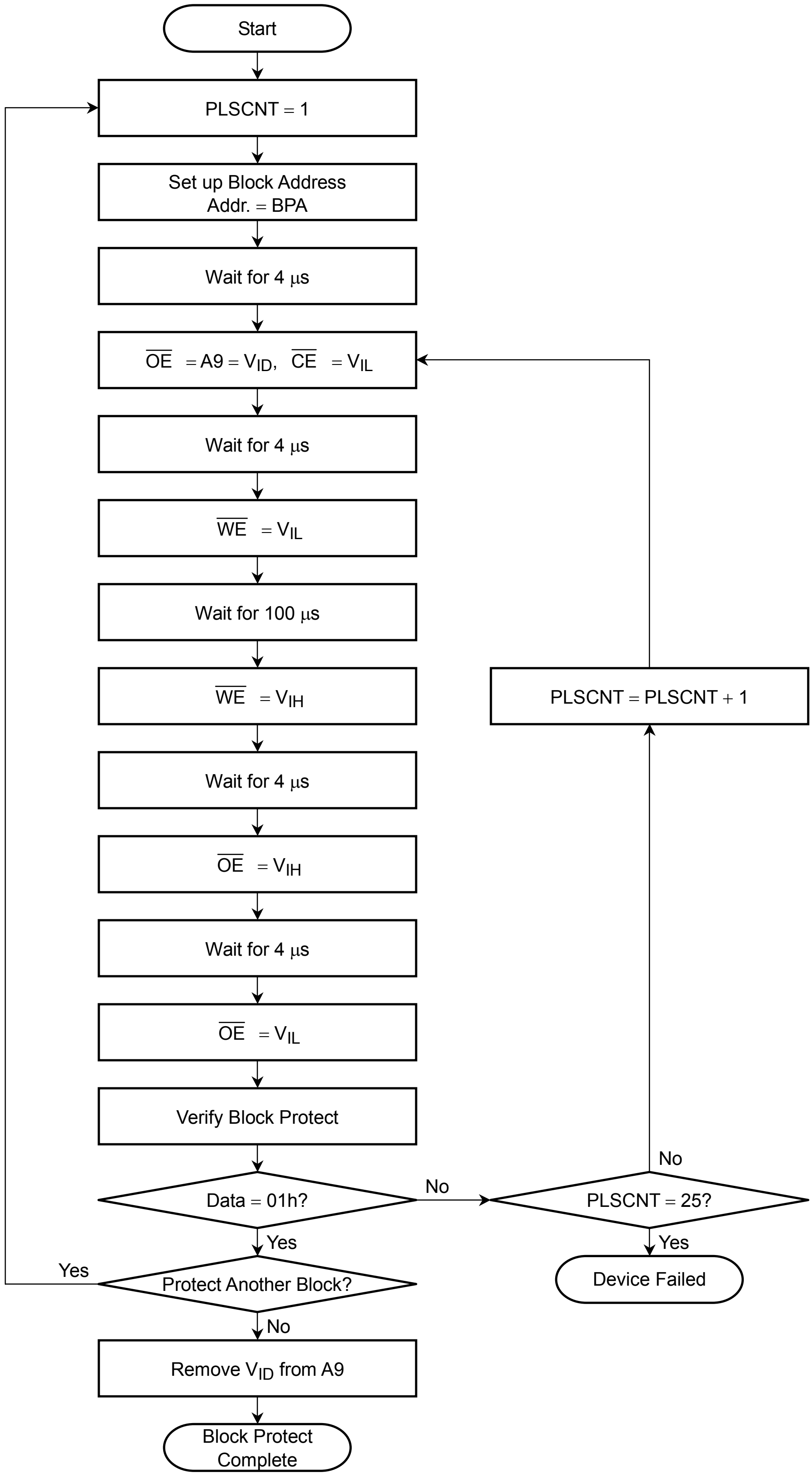
DQ6 Toggle Bit



1) : DQ6 must be rechecked even if DQ5 = 1 because DQ6 may stop toggling at the same time that DQ5 changes to 1.

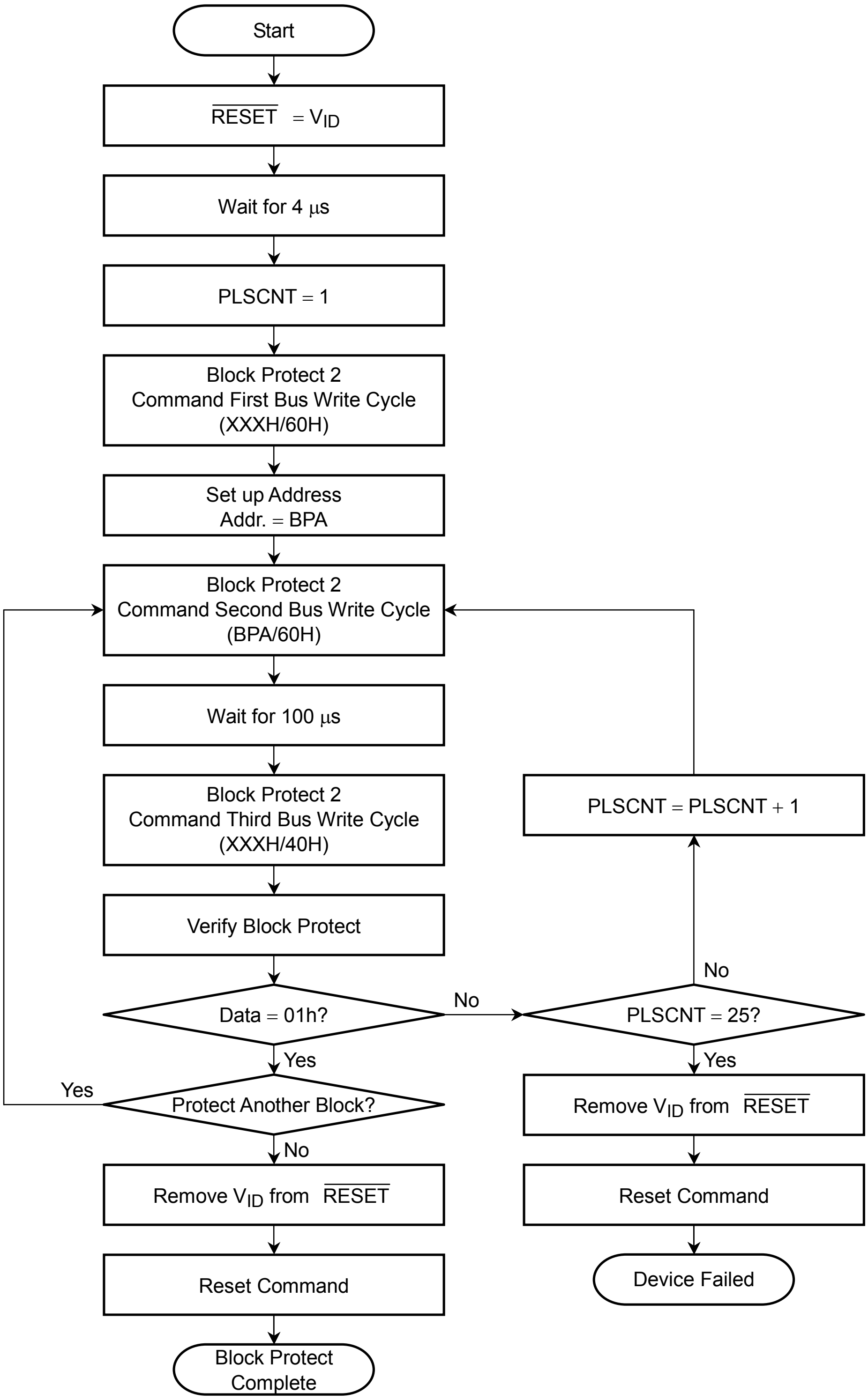
VA: Valid address for programming
Any of the addresses within the block being erased during a Block Erase operation
“Don’t care” during a Chip Erase operation

Block Protect 1



BPA: Block Address and ID Read Address (A6, A1, A0)
ID Read Address = (0, 1, 0)

Block Protect 2



BPA: Block Address and ID Read Address (A6, A1, A0)
ID Read Address = (0, 1, 0)

BLOCK ADDRESS TABLES

(1) TC58FVM6T2A (top boot block)

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE	
		BANK ADDRESS											
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	BYTE MODE	WORD MODE
BK0	BA0	L	L	L	L	L	L	L	*	*	*	000000h~00FFFFh	000000h~007FFFh
	BA1	L	L	L	L	L	L	H	*	*	*	010000h~01FFFFh	008000h~00FFFFh
	BA2	L	L	L	L	L	H	L	*	*	*	020000h~02FFFFh	010000h~017FFFh
	BA3	L	L	L	L	L	H	H	*	*	*	030000h~03FFFFh	018000h~01FFFFh
	BA4	L	L	L	L	H	L	L	*	*	*	040000h~04FFFFh	020000h~027FFFh
	BA5	L	L	L	L	H	L	H	*	*	*	050000h~05FFFFh	028000h~02FFFFh
	BA6	L	L	L	L	H	H	L	*	*	*	060000h~06FFFFh	030000h~037FFFh
	BA7	L	L	L	L	H	H	H	*	*	*	070000h~07FFFFh	038000h~03FFFFh
	BA8	L	L	L	H	L	L	L	*	*	*	080000h~08FFFFh	040000h~047FFFh
	BA9	L	L	L	H	L	L	H	*	*	*	090000h~09FFFFh	048000h~04FFFFh
	BA10	L	L	L	H	L	H	L	*	*	*	0A0000h~0AFFFFh	050000h~057FFFh
	BA11	L	L	L	H	L	H	H	*	*	*	0B0000h~0BFFFFh	058000h~05FFFFh
	BA12	L	L	L	H	H	L	L	*	*	*	0C0000h~0CFFFFh	060000h~067FFFh
	BA13	L	L	L	H	H	L	H	*	*	*	0D0000h~0DFFFFh	068000h~06FFFFh
	BA14	L	L	L	H	H	H	L	*	*	*	0E0000h~0EFFFFh	070000h~077FFFh
	BA15	L	L	L	H	H	H	H	*	*	*	0F0000h~0FFFFFh	078000h~07FFFFh
BK1	BA16	L	L	H	L	L	L	L	*	*	*	100000h~10FFFFh	080000h~087FFFh
	BA17	L	L	H	L	L	L	H	*	*	*	110000h~11FFFFh	088000h~08FFFFh
	BA18	L	L	H	L	L	H	L	*	*	*	120000h~12FFFFh	090000h~097FFFh
	BA19	L	L	H	L	L	H	H	*	*	*	130000h~13FFFFh	098000h~09FFFFh
	BA20	L	L	H	L	H	L	L	*	*	*	140000h~14FFFFh	0A0000h~0A7FFFh
	BA21	L	L	H	L	H	L	H	*	*	*	150000h~15FFFFh	0A8000h~0AFFFFh
	BA22	L	L	H	L	H	H	L	*	*	*	160000h~16FFFFh	0B0000h~0B7FFFh
	BA23	L	L	H	L	H	H	H	*	*	*	170000h~17FFFFh	0B8000h~0BFFFFh
	BA24	L	L	H	H	L	L	L	*	*	*	180000h~18FFFFh	0C0000h~0C7FFFh
	BA25	L	L	H	H	L	L	H	*	*	*	190000h~19FFFFh	0C8000h~0CFFFFh
	BA26	L	L	H	H	L	H	L	*	*	*	1A0000h~1AFFFFh	0D0000h~0D7FFFh
	BA27	L	L	H	H	L	H	H	*	*	*	1B0000h~1BFFFFh	0D8000h~0DFFFFh
	BA28	L	L	H	H	H	L	L	*	*	*	1C0000h~1CFFFFh	0E0000h~0E7FFFh
	BA29	L	L	H	H	H	L	H	*	*	*	1D0000h~1DFFFFh	0E8000h~0EFFFFh
	BA30	L	L	H	H	H	H	L	*	*	*	1E0000h~1EFFFFh	0F0000h~0F7FFFh
	BA31	L	L	H	H	H	H	H	*	*	*	1F0000h~1FFFFFh	0F8000h~0FFFFFh

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE	
		BANK ADDRESS											
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	BYTE MODE	WORD MODE
BK1	BA32	L	H	L	L	L	L	L	*	*	*	200000h~20FFFFh	100000h~107FFFh
	BA33	L	H	L	L	L	L	H	*	*	*	210000h~21FFFFh	108000h~10FFFFh
	BA34	L	H	L	L	L	H	L	*	*	*	220000h~22FFFFh	110000h~117FFFh
	BA35	L	H	L	L	L	H	H	*	*	*	230000h~23FFFFh	118000h~11FFFFh
	BA36	L	H	L	L	H	L	L	*	*	*	240000h~24FFFFh	120000h~127FFFh
	BA37	L	H	L	L	H	L	H	*	*	*	250000h~25FFFFh	128000h~12FFFFh
	BA38	L	H	L	L	H	H	L	*	*	*	260000h~26FFFFh	130000h~137FFFh
	BA39	L	H	L	L	H	H	H	*	*	*	270000h~27FFFFh	138000h~13FFFFh
	BA40	L	H	L	H	L	L	L	*	*	*	280000h~28FFFFh	140000h~147FFFh
	BA41	L	H	L	H	L	L	H	*	*	*	290000h~29FFFFh	148000h~14FFFFh
	BA42	L	H	L	H	L	H	L	*	*	*	2A0000h~2AFFFFh	150000h~157FFFh
	BA43	L	H	L	H	L	H	H	*	*	*	2B0000h~2BFFFFh	158000h~15FFFFh
	BA44	L	H	L	H	H	L	L	*	*	*	2C0000h~2CFFFFh	160000h~167FFFh
	BA45	L	H	L	H	H	L	H	*	*	*	2D0000h~2DFFFFh	168000h~16FFFFh
	BA46	L	H	L	H	H	H	L	*	*	*	2E0000h~2EFFFFh	170000h~177FFFh
	BA47	L	H	L	H	H	H	H	*	*	*	2F0000h~2FFFFFh	178000h~17FFFFh
	BA48	L	H	H	L	L	L	L	*	*	*	300000h~30FFFFh	180000h~187FFFh
	BA49	L	H	H	L	L	L	H	*	*	*	310000h~31FFFFh	188000h~18FFFFh
	BA50	L	H	H	L	L	H	L	*	*	*	320000h~32FFFFh	190000h~197FFFh
	BA51	L	H	H	L	L	H	H	*	*	*	330000h~33FFFFh	198000h~19FFFFh
	BA52	L	H	H	L	H	L	L	*	*	*	340000h~34FFFFh	1A0000h~1A7FFFh
	BA53	L	H	H	L	H	L	H	*	*	*	350000h~35FFFFh	1A8000h~1AFFFFh
	BA54	L	H	H	L	H	H	L	*	*	*	360000h~36FFFFh	1B0000h~1B7FFFh
	BA55	L	H	H	L	H	H	H	*	*	*	370000h~37FFFFh	1B8000h~1BFFFFh
	BA56	L	H	H	H	L	L	L	*	*	*	380000h~38FFFFh	1C0000h~1C7FFFh
	BA57	L	H	H	H	L	L	H	*	*	*	390000h~39FFFFh	1C8000h~1CFFFFh
	BA58	L	H	H	H	L	H	L	*	*	*	3A0000h~3AFFFFh	1D0000h~1D7FFFh
	BA59	L	H	H	H	L	H	H	*	*	*	3B0000h~3BFFFFh	1D8000h~1DFFFFh
	BA60	L	H	H	H	H	L	L	*	*	*	3C0000h~3CFFFFh	1E0000h~1E7FFFh
	BA61	L	H	H	H	H	L	H	*	*	*	3D0000h~3DFFFFh	1E8000h~1EFFFFh
	BA62	L	H	H	H	H	H	L	*	*	*	3E0000h~3EFFFFh	1F0000h~1F7FFFh
	BA63	L	H	H	H	H	H	H	*	*	*	3F0000h~3FFFFFh	1F8000h~1FFFFFh

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE	
		BANK ADDRESS											
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	BYTE MODE	WORD MODE
BK2	BA64	H	L	L	L	L	L	L	*	*	*	400000h~40FFFFh	200000h~207FFFh
	BA65	H	L	L	L	L	L	H	*	*	*	410000h~41FFFFh	208000h~20FFFFh
	BA66	H	L	L	L	L	H	L	*	*	*	420000h~42FFFFh	210000h~217FFFh
	BA67	H	L	L	L	L	H	H	*	*	*	430000h~43FFFFh	218000h~21FFFFh
	BA68	H	L	L	L	H	L	L	*	*	*	440000h~44FFFFh	220000h~227FFFh
	BA69	H	L	L	L	H	L	H	*	*	*	450000h~45FFFFh	228000h~22FFFFh
	BA70	H	L	L	L	H	H	L	*	*	*	460000h~46FFFFh	230000h~237FFFh
	BA71	H	L	L	L	H	H	H	*	*	*	470000h~47FFFFh	238000h~23FFFFh
	BA72	H	L	L	H	L	L	L	*	*	*	480000h~48FFFFh	240000h~247FFFh
	BA73	H	L	L	H	L	L	H	*	*	*	490000h~49FFFFh	248000h~24FFFFh
	BA74	H	L	L	H	L	H	L	*	*	*	4A0000h~4AFFFFh	250000h~257FFFh
	BA75	H	L	L	H	L	H	H	*	*	*	4B0000h~4BFFFFh	258000h~25FFFFh
	BA76	H	L	L	H	H	L	L	*	*	*	4C0000h~4CFFFFh	260000h~267FFFh
	BA77	H	L	L	H	H	L	H	*	*	*	4D0000h~4DFFFFh	268000h~26FFFFh
	BA78	H	L	L	H	H	H	L	*	*	*	4E0000h~4EFFFFh	270000h~277FFFh
	BA79	H	L	L	H	H	H	H	*	*	*	4F0000h~4FFFFFh	278000h~27FFFFh
	BA80	H	L	H	L	L	L	L	*	*	*	500000h~50FFFFh	280000h~287FFFh
	BA81	H	L	H	L	L	L	H	*	*	*	510000h~51FFFFh	288000h~28FFFFh
	BA82	H	L	H	L	L	H	L	*	*	*	520000h~52FFFFh	290000h~297FFFh
	BA83	H	L	H	L	L	H	H	*	*	*	530000h~53FFFFh	298000h~29FFFFh
	BA84	H	L	H	L	H	L	L	*	*	*	540000h~54FFFFh	2A0000h~2A7FFFh
	BA85	H	L	H	L	H	L	H	*	*	*	550000h~55FFFFh	2A8000h~2AFFFFh
	BA86	H	L	H	L	H	H	L	*	*	*	560000h~56FFFFh	2B0000h~2B7FFFh
	BA87	H	L	H	L	H	H	H	*	*	*	570000h~57FFFFh	2B8000h~2BFFFFh
	BA88	H	L	H	H	L	L	L	*	*	*	580000h~58FFFFh	2C0000h~2C7FFFh
	BA89	H	L	H	H	L	L	H	*	*	*	590000h~59FFFFh	2C8000h~2CFFFFh
	BA90	H	L	H	H	L	H	L	*	*	*	5A0000h~5AFFFFh	2D0000h~2D7FFFh
	BA91	H	L	H	H	L	H	H	*	*	*	5B0000h~5BFFFFh	2D8000h~2DFFFFh
	BA92	H	L	H	H	H	L	L	*	*	*	5C0000h~5CFFFFh	2E0000h~2E7FFFh
	BA93	H	L	H	H	H	L	H	*	*	*	5D0000h~5DFFFFh	2E8000h~2EFFFFh
	BA94	H	L	H	H	H	H	L	*	*	*	5E0000h~5EFFFFh	2F0000h~2F7FFFh
	BA95	H	L	H	H	H	H	H	*	*	*	5F0000h~5FFFFFh	2F8000h~2FFFFFh

BANK #	BLOCK #	BLOCK ADDRESS (BANK ADDRESS: A21–A19)										ADDRESS RANGE	
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	BYTE MODE	WORD MODE
BK2	BA96	H	H	L	L	L	L	L	*	*	*	600000h~60FFFFh	300000h~307FFFh
	BA97	H	H	L	L	L	L	H	*	*	*	610000h~61FFFFh	308000h~30FFFFh
	BA98	H	H	L	L	L	H	L	*	*	*	620000h~62FFFFh	310000h~317FFFh
	BA99	H	H	L	L	L	H	H	*	*	*	630000h~63FFFFh	318000h~31FFFFh
	BA100	H	H	L	L	H	L	L	*	*	*	640000h~64FFFFh	320000h~327FFFh
	BA101	H	H	L	L	H	L	H	*	*	*	650000h~65FFFFh	328000h~32FFFFh
	BA102	H	H	L	L	H	H	L	*	*	*	660000h~66FFFFh	330000h~337FFFh
	BA103	H	H	L	L	H	H	H	*	*	*	670000h~67FFFFh	338000h~33FFFFh
	BA104	H	H	L	H	L	L	L	*	*	*	680000h~68FFFFh	340000h~347FFFh
	BA105	H	H	L	H	L	L	H	*	*	*	690000h~69FFFFh	348000h~34FFFFh
	BA106	H	H	L	H	L	H	L	*	*	*	6A0000h~6AFFFFh	350000h~357FFFh
	BA107	H	H	L	H	L	H	H	*	*	*	6B0000h~6BFFFFh	358000h~35FFFFh
	BA108	H	H	L	H	H	L	L	*	*	*	6C0000h~6CFFFFh	360000h~367FFFh
	BA109	H	H	L	H	H	L	H	*	*	*	6D0000h~6DFFFFh	368000h~36FFFFh
	BA110	H	H	L	H	H	H	L	*	*	*	6E0000h~6EFFFFh	370000h~377FFFh
	BA111	H	H	L	H	H	H	H	*	*	*	6F0000h~6FFFFFh	378000h~37FFFFh
BK3	BA112	H	H	H	L	L	L	L	*	*	*	700000h~70FFFFh	380000h~387FFFh
	BA113	H	H	H	L	L	L	H	*	*	*	710000h~71FFFFh	388000h~38FFFFh
	BA114	H	H	H	L	L	H	L	*	*	*	720000h~72FFFFh	390000h~397FFFh
	BA115	H	H	H	L	L	H	H	*	*	*	730000h~73FFFFh	398000h~39FFFFh
	BA116	H	H	H	L	H	L	L	*	*	*	740000h~74FFFFh	3A0000h~3A7FFFh
	BA117	H	H	H	L	H	L	H	*	*	*	770000h~75FFFFh	3A8000h~3AFFFFh
	BA118	H	H	H	L	H	H	L	*	*	*	760000h~76FFFFh	3B0000h~3B7FFFh
	BA119	H	H	H	L	H	H	H	*	*	*	770000h~77FFFFh	3B8000h~3BFFFFh
	BA120	H	H	H	H	L	L	L	*	*	*	780000h~78FFFFh	3C0000h~3C7FFFh
	BA121	H	H	H	H	L	L	H	*	*	*	790000h~79FFFFh	3C8000h~3CFFFFh
	BA122	H	H	H	H	L	H	L	*	*	*	7A0000h~7AFFFFh	3D0000h~3D7FFFh
	BA123	H	H	H	H	L	H	H	*	*	*	7B0000h~7BFFFFh	3D8000h~3DFFFFh
	BA124	H	H	H	H	H	L	L	*	*	*	7C0000h~7CFFFFh	3E0000h~3E7FFFh
	BA125	H	H	H	H	H	L	H	*	*	*	7D0000h~7DFFFFh	3E8000h~3EFFFFh
	BA126	H	H	H	H	H	H	L	*	*	*	7E0000h~7EFFFFh	3F0000h~3F7FFFh

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE	
		BANK ADDRESS											
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	BYTE MODE	WORD MODE
BK3	BA127	H	H	H	H	**H**	H	**H**	L	L	L	7F0000h~7F1FFFh	3F8000h~3F8FFFh
	BA128	H	H	H	H	**H**	H	**H**	L	L	**H**	7F2000h~7F3FFFh	3F9000h~3F9FFFh
	BA129	H	H	H	H	H	H	H	L	H	L	7F4000h~7F5FFFh	3FA000h~3FAFFFh
	BA130	H	H	H	H	H	H	H	L	H	H	7F6000h~7F7FFFh	3FB000h~3FBFFFh
	BA131	H	H	H	H	H	H	H	H	L	L	7F8000h~7F9FFFh	3FC000h~3FCFFFh
	BA132	H	H	H	H	H	H	H	H	L	H	7FA000h~7FBFFFh	3FD000h~3FDFFFh
	BA133	H	H	H	H	H	H	H	H	H	L	7FC000h~7FDFFFh	3FE000h~3FEFFFh
	BA134	H	H	H	H	H	H	H	H	H	H	7FE000h~7FFFFFh	3FF000h~3FFFFFh

(2) TC58FVM6B2A (bottom boot block)

BANK #	BLOCK #	BLOCK ADDRESS (BANK ADDRESS: A21–A19)										ADDRESS RANGE	
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	BYTE MODE	WORD MODE
BK0	BA0	L	L	L	L	L	L	L	L	L	L	000000h~001FFFh	000000h~000FFFh
	BA1	L	L	L	L	L	L	L	L	L	H	002000h~003FFFh	001000h~001FFFh
	BA2	L	L	L	L	L	L	L	L	H	L	004000h~005FFFh	002000h~002FFFh
	BA3	L	L	L	L	L	L	L	L	H	H	006000h~007FFFh	003000h~003FFFh
	BA4	L	L	L	L	L	L	L	H	L	L	008000h~009FFFh	004000h~004FFFh
	BA5	L	L	L	L	L	L	L	H	L	H	00A000h~00BFFFh	005000h~005FFFh
	BA6	L	L	L	L	L	L	L	H	H	L	00C000h~00DFFFh	006000h~006FFFh
	BA7	L	L	L	L	L	L	L	H	H	H	00E000h~00FFFFh	007000h~007FFFh
	BA8	L	L	L	L	L	L	H	*	*	*	010000h~01FFFFh	008000h~00FFFFh
	BA9	L	L	L	L	L	H	L	*	*	*	020000h~02FFFFh	010000h~017FFFh
	BA10	L	L	L	L	L	H	H	*	*	*	030000h~03FFFFh	018000h~01FFFFh
	BA11	L	L	L	L	H	L	L	*	*	*	040000h~04FFFFh	020000h~027FFFh
	BA12	L	L	L	L	H	L	H	*	*	*	050000h~05FFFFh	028000h~02FFFFh
	BA13	L	L	L	L	H	H	L	*	*	*	060000h~06FFFFh	030000h~037FFFh
	BA14	L	L	L	L	H	H	H	*	*	*	070000h~07FFFFh	038000h~03FFFFh
	BA15	L	L	L	H	L	L	L	*	*	*	080000h~08FFFFh	040000h~047FFFh
	BA16	L	L	L	H	L	L	H	*	*	*	090000h~09FFFFh	048000h~04FFFFh
	BA17	L	L	L	H	L	H	L	*	*	*	0A0000h~0AFFFFh	050000h~057FFFh
	BA18	L	L	L	H	L	H	H	*	*	*	0B0000h~0BFFFFh	058000h~05FFFFh
	BA19	L	L	L	H	H	L	L	*	*	*	0C0000h~0CFFFFh	060000h~067FFFh
	BA20	L	L	L	H	H	L	H	*	*	*	0D0000h~0DFFFFh	068000h~06FFFFh
	BA21	L	L	L	H	H	H	L	*	*	*	0E0000h~0EFFFFh	070000h~077FFFh
	BA22	L	L	L	H	H	H	H	*	*	*	0F0000h~0FFFFFh	078000h~07FFFFh
BK1	BA23	L	L	H	L	L	L	L	*	*	*	100000h~10FFFFh	080000h~087FFFh
	BA24	L	L	H	L	L	L	H	*	*	*	110000h~11FFFFh	088000h~08FFFFh
	BA25	L	L	H	L	L	H	L	*	*	*	120000h~12FFFFh	090000h~097FFFh
	BA26	L	L	H	L	L	H	H	*	*	*	130000h~13FFFFh	098000h~09FFFFh
	BA27	L	L	H	L	H	L	L	*	*	*	140000h~14FFFFh	0A0000h~0A7FFFh
	BA28	L	L	H	L	H	L	H	*	*	*	150000h~15FFFFh	0A8000h~0AFFFFh
	BA29	L	L	H	L	H	H	L	*	*	*	160000h~16FFFFh	0B0000h~0B7FFFh
	BA30	L	L	H	L	H	H	H	*	*	*	170000h~17FFFFh	0B8000h~0BFFFFh

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE	
		BANK ADDRESS											
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	BYTE MODE	WORD MODE
BK1	BA31	L	L	H	H	L	L	L	*	*	*	180000h~18FFFFh	0C0000h~0C7FFFh
	BA32	L	L	H	H	L	L	H	*	*	*	190000h~19FFFFh	0C8000h~0CFFFFh
	BA33	L	L	H	H	L	H	L	*	*	*	1A0000h~1AFFFFh	0D0000h~0D7FFFh
	BA34	L	L	H	H	L	H	H	*	*	*	1B0000h~1BFFFFh	0D8000h~0DFFFFh
	BA35	L	L	H	H	H	L	L	*	*	*	1C0000h~1CFFFFh	0E0000h~0E7FFFh
	BA36	L	L	H	H	H	L	H	*	*	*	1D0000h~1DFFFFh	0E8000h~0EFFFFh
	BA37	L	L	H	H	H	H	L	*	*	*	1E0000h~1EFFFFh	0F0000h~0F7FFFh
	BA38	L	L	H	H	H	H	H	*	*	*	1F0000h~1FFFFFh	0F8000h~0FFFFFh
	BA39	L	H	L	L	L	L	L	*	*	*	200000h~20FFFFh	100000h~107FFFh
	BA40	L	H	L	L	L	L	H	*	*	*	210000h~21FFFFh	108000h~10FFFFh
	BA41	L	H	L	L	L	H	L	*	*	*	220000h~22FFFFh	110000h~117FFFh
	BA42	L	H	L	L	L	H	H	*	*	*	230000h~23FFFFh	118000h~11FFFFh
	BA43	L	H	L	L	H	L	L	*	*	*	240000h~24FFFFh	120000h~127FFFh
	BA44	L	H	L	L	H	L	H	*	*	*	250000h~25FFFFh	128000h~12FFFFh
	BA45	L	H	L	L	H	H	L	*	*	*	260000h~26FFFFh	130000h~137FFFh
	BA46	L	H	L	L	H	H	H	*	*	*	270000h~27FFFFh	138000h~13FFFFh
	BA47	L	H	L	H	L	L	L	*	*	*	280000h~28FFFFh	140000h~147FFFh
	BA48	L	H	L	H	L	L	H	*	*	*	290000h~29FFFFh	148000h~14FFFFh
	BA49	L	H	L	H	L	H	L	*	*	*	2A0000h~2AFFFFh	150000h~157FFFh
	BA50	L	H	L	H	L	H	H	*	*	*	2B0000h~2BFFFFh	158000h~15FFFFh
	BA51	L	H	L	H	H	L	L	*	*	*	2C0000h~2CFFFFh	160000h~167FFFh
	BA52	L	H	L	H	H	L	H	*	*	*	2D0000h~2DFFFFh	168000h~16FFFFh
	BA53	L	H	L	H	H	H	L	*	*	*	2E0000h~2EFFFFh	170000h~177FFFh
	BA54	L	H	L	H	H	H	H	*	*	*	2F0000h~2FFFFFh	178000h~17FFFFh
	BA55	L	H	H	L	L	L	L	*	*	*	300000h~30FFFFh	180000h~187FFFh
	BA56	L	H	H	L	L	L	H	*	*	*	310000h~31FFFFh	188000h~18FFFFh
	BA57	L	H	H	L	L	H	L	*	*	*	320000h~32FFFFh	190000h~197FFFh
	BA58	L	H	H	L	L	H	H	*	*	*	330000h~33FFFFh	198000h~19FFFFh
	BA59	L	H	H	L	H	L	L	*	*	*	340000h~34FFFFh	1A0000h~1A7FFFh
	BA60	L	H	H	L	H	L	H	*	*	*	350000h~35FFFFh	1A8000h~1AFFFFh
	BA61	L	H	H	L	H	H	L	*	*	*	360000h~36FFFFh	1B0000h~1B7FFFh
	BA62	L	H	H	L	H	H	H	*	*	*	370000h~37FFFFh	1B8000h~1BFFFFh

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE	
		BANK ADDRESS											
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	BYTE MODE	WORD MODE
BK1	BA63	L	H	H	H	L	L	L	*	*	*	380000h~38FFFFh	1C0000h~1C7FFFh
	BA64	L	H	H	H	L	L	H	*	*	*	390000h~39FFFFh	1C8000h~1CFFFFh
	BA65	L	H	H	H	L	H	L	*	*	*	3A0000h~3AFFFFh	1D0000h~1D7FFFh
	BA66	L	H	H	H	L	H	H	*	*	*	3B0000h~3BFFFFh	1D8000h~1DFFFFh
	BA67	L	H	H	H	H	L	L	*	*	*	3C0000h~3CFFFFh	1E0000h~1E7FFFh
	BA68	L	H	H	H	H	L	H	*	*	*	3D0000h~3DFFFFh	1E8000h~1EFFFFh
	BA69	L	H	H	H	H	H	L	*	*	*	3E0000h~3EFFFFh	1F0000h~1F7FFFh
	BA70	L	H	H	H	H	H	H	*	*	*	3F0000h~3FFFFFh	1F8000h~1FFFFFh
BK2	BA71	H	L	L	L	L	L	L	*	*	*	400000h~40FFFFh	200000h~207FFFh
	BA72	H	L	L	L	L	L	H	*	*	*	410000h~41FFFFh	208000h~20FFFFh
	BA73	H	L	L	L	L	H	L	*	*	*	420000h~42FFFFh	210000h~217FFFh
	BA74	H	L	L	L	L	H	H	*	*	*	430000h~43FFFFh	218000h~21FFFFh
	BA75	H	L	L	L	H	L	L	*	*	*	440000h~44FFFFh	220000h~227FFFh
	BA76	H	L	L	L	H	L	H	*	*	*	450000h~45FFFFh	228000h~22FFFFh
	BA77	H	L	L	L	H	H	L	*	*	*	460000h~46FFFFh	230000h~237FFFh
	BA78	H	L	L	L	H	H	H	*	*	*	470000h~47FFFFh	238000h~23FFFFh
	BA79	H	L	L	H	L	L	L	*	*	*	480000h~48FFFFh	240000h~247FFFh
	BA80	H	L	L	H	L	L	H	*	*	*	490000h~49FFFFh	248000h~24FFFFh
	BA81	H	L	L	H	L	H	L	*	*	*	4A0000h~4AFFFFh	250000h~257FFFh
	BA82	H	L	L	H	L	H	H	*	*	*	4B0000h~4BFFFFh	258000h~25FFFFh
	BA83	H	L	L	H	H	L	L	*	*	*	4C0000h~4CFFFFh	260000h~267FFFh
	BA84	H	L	L	H	H	L	H	*	*	*	4D0000h~4DFFFFh	268000h~26FFFFh
	BA85	H	L	L	H	H	H	L	*	*	*	4E0000h~4EFFFFh	270000h~277FFFh
	BA86	H	L	L	H	H	H	H	*	*	*	4F0000h~4FFFFFh	278000h~27FFFFh
	BA87	H	L	H	L	L	L	L	*	*	*	500000h~50FFFFh	280000h~287FFFh
	BA88	H	L	H	L	L	L	H	*	*	*	510000h~51FFFFh	288000h~28FFFFh
	BA89	H	L	H	L	L	H	L	*	*	*	520000h~52FFFFh	290000h~297FFFh
	BA90	H	L	H	L	L	H	H	*	*	*	530000h~53FFFFh	298000h~29FFFFh
	BA91	H	L	H	L	H	L	L	*	*	*	540000h~54FFFFh	2A0000h~2A7FFFh
	BA92	H	L	H	L	H	L	H	*	*	*	550000h~55FFFFh	2A8000h~2AFFFFh
	BA93	H	L	H	L	H	H	L	*	*	*	560000h~56FFFFh	2B0000h~2B7FFFh
	BA94	H	L	H	L	H	H	H	*	*	*	570000h~57FFFFh	2B8000h~2BFFFFh

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE	
		BANK ADDRESS											
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	BYTE MODE	WORD MODE
BK2	BA95	H	L	H	H	L	L	L	*	*	*	580000h~58FFFFh	2C0000h~2C7FFFh
	BA96	H	L	H	H	L	L	H	*	*	*	590000h~59FFFFh	2C8000h~2CFFFFh
	BA97	H	L	H	H	L	H	L	*	*	*	5A0000h~5AFFFFh	2D0000h~2D7FFFh
	BA98	H	L	H	H	L	H	H	*	*	*	5B0000h~5BFFFFh	2D8000h~2DFFFFh
	BA99	H	L	H	H	H	L	L	*	*	*	5C0000h~5CFFFFh	2E0000h~2E7FFFh
	BA100	H	L	H	H	H	L	H	*	*	*	5D0000h~5DFFFFh	2E8000h~2EFFFFh
	BA101	H	L	H	H	H	H	L	*	*	*	5E0000h~5EFFFFh	2F0000h~2F7FFFh
	BA102	H	L	H	H	H	H	H	*	*	*	5F0000h~5FFFFFh	2F8000h~2FFFFFh
	BA103	H	H	L	L	L	L	L	*	*	*	600000h~60FFFFh	300000h~307FFFh
	BA104	H	H	L	L	L	L	H	*	*	*	610000h~61FFFFh	308000h~30FFFFh
	BA105	H	H	L	L	L	H	L	*	*	*	620000h~62FFFFh	310000h~317FFFh
	BA106	H	H	L	L	L	H	H	*	*	*	630000h~63FFFFh	318000h~31FFFFh
	BA107	H	H	L	L	H	L	L	*	*	*	640000h~64FFFFh	320000h~327FFFh
	BA108	H	H	L	L	H	L	H	*	*	*	650000h~65FFFFh	328000h~32FFFFh
	BA109	H	H	L	L	H	H	L	*	*	*	660000h~66FFFFh	330000h~337FFFh
	BA110	H	H	L	L	H	H	H	*	*	*	670000h~67FFFFh	338000h~33FFFFh
	BA111	H	H	L	H	L	L	L	*	*	*	680000h~68FFFFh	340000h~347FFFh
	BA112	H	H	L	H	L	L	H	*	*	*	690000h~69FFFFh	348000h~34FFFFh
	BA113	H	H	L	H	L	H	L	*	*	*	6A0000h~6AFFFFh	350000h~357FFFh
	BA114	H	H	L	H	L	H	H	*	*	*	6B0000h~6BFFFFh	358000h~35FFFFh
	BA115	H	H	L	H	H	L	L	*	*	*	6C0000h~6CFFFFh	360000h~367FFFh
	BA116	H	H	L	H	H	L	H	*	*	*	6D0000h~6DFFFFh	368000h~36FFFFh
	BA117	H	H	L	H	H	H	L	*	*	*	6E0000h~6EFFFFh	370000h~377FFFh
	BA118	H	H	L	H	H	H	H	*	*	*	6F0000h~6FFFFFh	378000h~37FFFFh
BK3	BA119	H	H	H	L	L	L	L	*	*	*	700000h~70FFFFh	380000h~387FFFh
	BA120	H	H	H	L	L	L	H	*	*	*	710000h~71FFFFh	388000h~38FFFFh
	BA121	H	H	H	L	L	H	L	*	*	*	720000h~72FFFFh	390000h~397FFFh
	BA122	H	H	H	L	L	H	H	*	*	*	730000h~73FFFFh	398000h~39FFFFh
	BA123	H	H	H	L	H	L	L	*	*	*	740000h~74FFFFh	3A0000h~3A7FFFh
	BA124	H	H	H	L	H	L	H	*	*	*	750000h~75FFFFh	3A8000h~3AFFFFh
	BA125	H	H	H	L	H	H	L	*	*	*	760000h~76FFFFh	3B0000h~3B7FFFh
	BA126	H	H	H	L	H	H	H	*	*	*	770000h~77FFFFh	3B8000h~3BFFFFh

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE	
		BANK ADDRESS											
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	BYTE MODE	WORD MODE
BK3	BA127	H	H	H	H	L	L	L	*	*	*	780000h~78FFFFh	3C0000h~3C7FFFh
	BA128	H	H	H	H	L	L	H	*	*	*	790000h~79FFFFh	3C8000h~3CFFFFh
	BA129	H	H	H	H	L	H	L	*	*	*	7A0000h~7AFFFFh	3D0000h~3D7FFFh
	BA130	H	H	H	H	L	H	H	*	*	*	7B0000h~7BFFFFh	3D8000h~3DFFFFh
	BA131	H	H	H	H	H	L	L	*	*	*	7C0000h~7CFFFFh	3E0000h~3E7FFFh
	BA132	H	H	H	H	H	L	H	*	*	*	7D0000h~7DFFFFh	3E8000h~3EFFFFh
	BA133	H	H	H	H	H	H	L	*	*	*	7E0000h~7EFFFFh	3F0000h~3F7FFFh
	BA134	H	H	H	H	H	H	H	*	*	*	7F0000h~7FFFFFh	3F8000h~3FFFFFh

BLOCK SIZE TABLE

(1) TC58FVM6T2A (top boot block)

BLOCK #	BLOCK SIZE		BANK #	BANK SIZE		BLOCK COUNT
	BYTE MODE	WORD MODE		BYTE MODE	WORD MODE	
BA0~BA15	64 Kbytes	32 Kwords	BK0	1024 Kbytes	512 Kwords	16
BA16~BA63	64 Kbytes	32 Kwords	BK1	3072 Kbytes	1536 Kwords	48
BA64~BA111	64 Kbytes	32 Kwords	BK2	3072 Kbytes	1536 Kwords	48
BA112~BA126	64 Kbytes	32 Kwords	BK3	960 Kbytes	480 Kwords	15
BA127~BA134	8 Kbytes	4 Kwords	BK3	64 Kbytes	32 Kwords	8

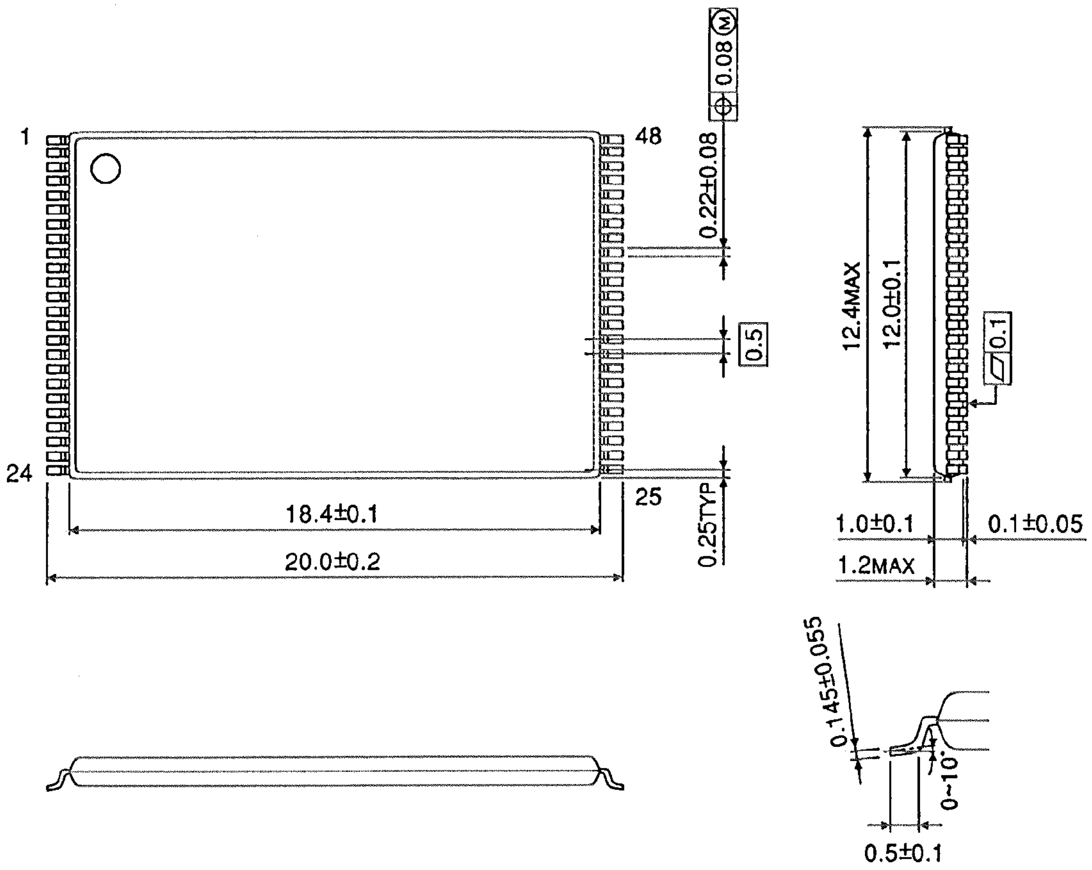
(2) TC58FVM6B2A (bottom boot block)

BLOCK #	BLOCK SIZE		BANK #	BANK SIZE		BLOCK COUNT
	BYTE MODE	WORD MODE		BYTE MODE	WORD MODE	
BA0~BA7	8 Kbytes	4 Kwords	BK0	64 Kbytes	32 Kwords	8
BA8~BA22	64 Kbytes	32 Kwords	BK0	960 Kbytes	480 Kwords	15
BA23~BA70	64 Kbytes	32 Kwords	BK1	3072 Kbytes	1536 Kwords	48
BA71~BA118	64 Kbytes	32 Kwords	BK2	3072 Kbytes	1536 Kwords	48
BA119~BA134	64 Kbytes	32 Kwords	BK3	1024 Kbytes	512 Kwords	16

PACKAGE DIMENSIONS

Unit: mm

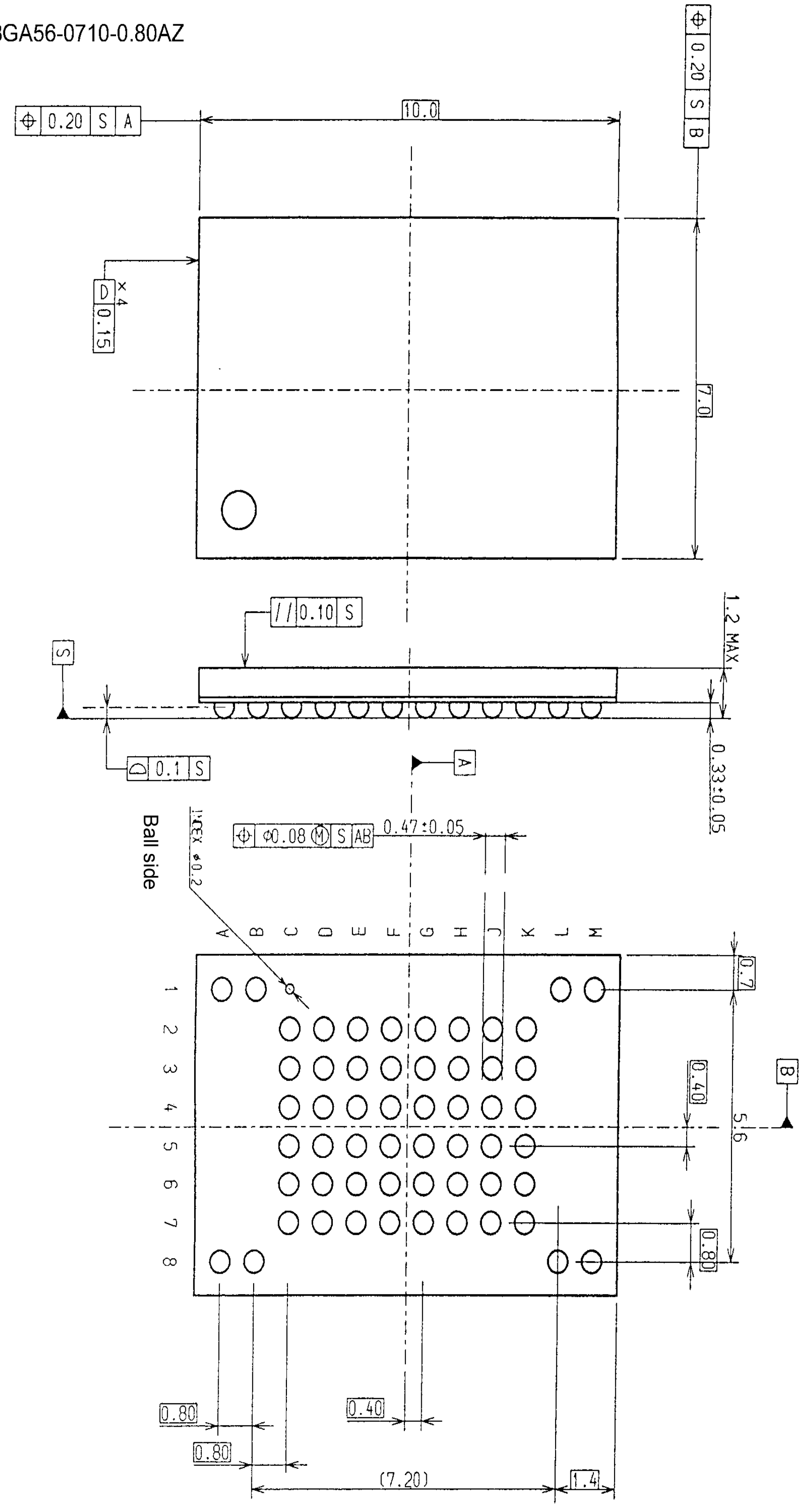
TSOPI48-P-1220-0.50



PACKAGE DIMENSIONS

Unit: mm

P-TFBGA56-0710-0.80AZ



Revision History

Date	Rev.	Description
2002-03-14	1.00	Original version
2002-06-21	1.01	P.6 Corrected bank addresses. P.15 Corrected CFI CODE (31H). P.23 Changed t_{SUSP} Spec. P.25 Added timing diagram of read after command input.
2002-07-31	1.02	P.17 Added explanation of $\overline{\text{DATA}}$ polling in case of page program operation. P.20 Added V_{ID}/V_{ACC} comments.
2002-08-07	1.03	P21 Added I_{DDO8} Spec P23 Added t_{BEH} (Erase Hold Time) Spec
2002-08-07	1.04	P21 Added DC Typical Value
2002-10-17	1.05	Added FBGA package. Added Ordering information.
2002-10-24	1.07	Generalize
2003-01-29	1.08	Added the PIN Capacitance. Added the Block protect 2 at mode selection. Added a part of comment (CMD ID-READ). Modified the comment of Hidden ROM Area. Modified the absolute maximum range of Power Dissipation. Deleted the spec of t_{AHW}. Modified the block address table. Annotated Absolute Maximum Ratings. Deleted annotation of Recommended DC operating conditions.
2003-05-15	1.09	Added the minimum interval between resume and the following suspend command
2003-06-30	1.11	Modified the timing diagrams ($\overline{\text{BYTE}}$ during Read Operation). Add the spec of t_{OEH}. P13 Modified the comment of Verify Block Protect. P10-12 Modified the comment for host processor. Add the spec of t_{CEHT}.

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