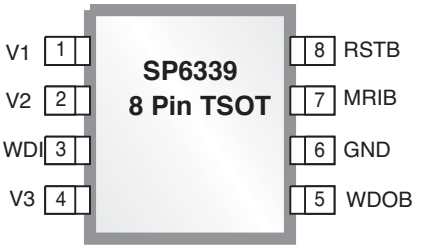
SP6339, SP6341

Triple μPower Supervisory Circuit with Manual Reset and Watchdog

FEATURES

- Low operating voltage of 1.6V
- Low operating current of 20μA typical
- Monitors up to 3 supplies simultaneously
- Adjustable input monitors down to 0.5V
- Reset asserted down to 0.9V
- 2% accuracy over temperature range
- Open Drain (OD) or CMOS RSTB output
- 4 Reset Timeout Periods: 50mS, 100mS, 200mS, and 400mS
- Watch Dog Timer Function -- WDI
- Independent OD or CMOS Watchdog Output (Active Low) -- WDOB
- Manual Reset Input (Active Low) -- MRIB
- 8 Pin TSOT package



Open Drain $\overline{\text{RESET}}$

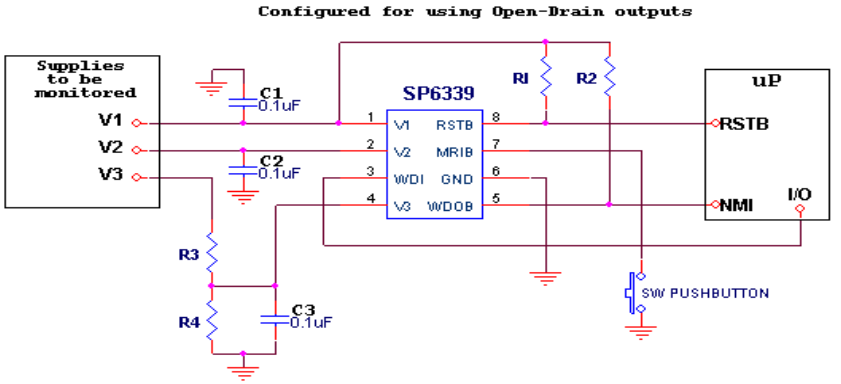
SEE PAGE 2 FOR OTHER AVAILABLE PINOUTS

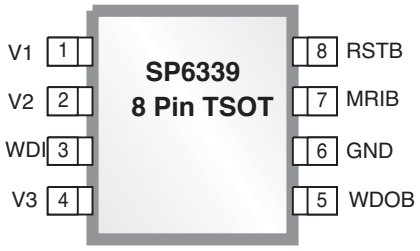
Now Available in Lead Free Packaging

DESCRIPTION

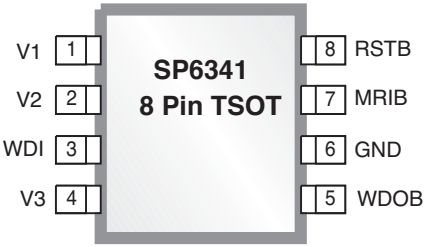
SP6339-SP6341 Triple μPower Supervisory Circuit Family is a family of microprocessor reset supervisory circuits with multiple reset voltages. The family provides low voltage monitoring ability for up to three supplies with two precision factory-set thresholds and one user defined custom threshold. These circuits perform a single function: if any of the input supply voltages drops below its associated threshold, reset outputs are asserted. Products in the family offer manual reset and watchdog functionalities. SP6339 and SP6341 are packaged in an 8-pin TSOT package. All devices are fully specified over -40°C to +85°C temperature range.

TYPICAL APPLICATION CIRCUIT





Open Drain $\overline{\text{RESET}}$



CMOS $\overline{\text{RESET}}$

PART NUMBER	V1	V2	V3	Reset	MRIB	WDI	WDOB
SP6339	√	√	√	OD Active Low	√	√	OD Active Low
SP6341	√	√	√	CMOS Active Low	√	√	CMOS Active Low

Feature and Pinout Diagram

Representative Samples Available

Sipex Product	Product Description	Package	V1 (Volts)	V2 (Volts)	V3 (Volts)	V4 (Volts)	Reset (ms)	Ordering #
SP6339	Triple Supervisor Open Drain low	8 Pin TSOT	4.625	2.313	0.5	N/A	200	SP6339EK1-L-Z-J-C

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

Terminal Voltage (with respect to GND)
V1, V2..... -0.3 to +6V

Open-Drain RSTB,
WDOB.....-0.3 to +6V

CMOS RST, RSTB,
WDOB..... -0.3 to (V1+0.3V)

Input Current/Output
Current.....,,.....20mA

V3, MRIB, WDI.....-0.3 to (V1+0.3V)

Operating Temperature
Range.....-40°C to +85°C

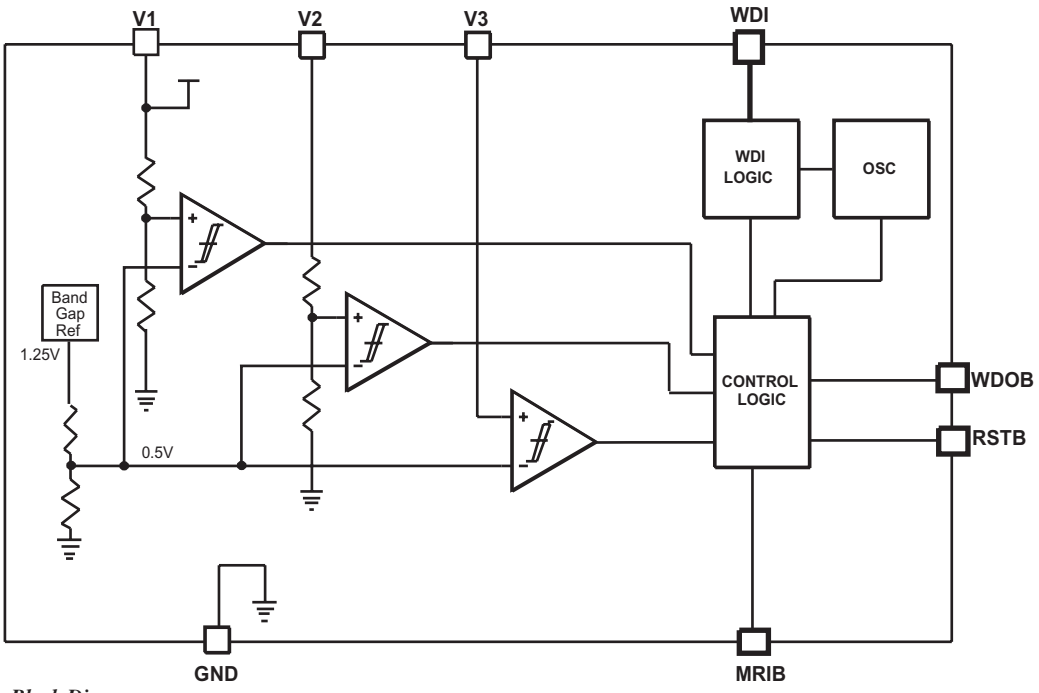
Storage Temperature
Range.....-65°C to 150°C

Thermal Resistance Θ_{JA}.....134°C/W

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V1 = 1.6V to 5.5V; TA = -40ºC to +85ºC; unless otherwise noted. Typical values are at TA =+25ºC					
Operating Voltage Range	0.9		5.5	V	T_A = -40ºC to +85ºC
Supply Current		20	30	uA	V1 < 5.5V, V2 < 3.60V, all I/O pins open
		15	25		V1 < 3.6V, V2 < 2.75V, all I/O pins open
V1 Reset Threshold	4.532	4.625	4.718	V	Z (valid for V1 falling)
	4.287	4.375	4.463		Y (valid for V1 falling)
	3.013	3.075	3.137		X (valid for V1 falling)
	2.866	2.925	2.984		W (valid for V1 falling)
	2.572	2.625	2.678		V (valid for V1 falling)
	2.273	2.320	2.367		U (valid for V1 falling)
	2.146	2.190	2.234		T (valid for V1 falling)
	1.636	1.670	1.704		S (valid for V1 falling)
	1.548	1.580	1.612		R (valid for V1 falling)
V2 Reset Threshold	2.266	2.313	2.360	V	J (valid for V2 falling)
	2.144	2.188	2.232		I (valid for V2 falling)
	1.631	1.665	1.698		H (valid for V2 falling)
	1.543	1.575	1.607		G (valid for V2 falling)
	1.360	1.388	1.416		F (valid for V2 falling)
	1.286	1.313	1.340		E (valid for V2 falling)
	1.087	1.110	1.133		D (valid for V2 falling)
	1.029	1.050	1.071		C (valid for V2 falling)
	0.816	0.833	0.850		B (valid for V2 falling)
	0.772	0.788	0.804		A (valid for V2 falling)
Threshold 1 Tempco		0.06		mV/ºC	
Threshold 2 Tempco		0.04		mV/ºC	
Threshold 1 Hysteresis		0.65		%	reference to Vth1 typical
Threshold 2 Hysteresis		0.5		%	reference to Vth2 typical
V1 to RST/RSTB Delay		50		us	V1 = Vth1 to (Vth1-0.1V), Vth1 = 3.075
V2 to RST/RSTB Delay		50		us	V2 = Vth2 to (Vth2-0.1V), Vth2 = 1.575
Reset Timeout Period (T1)	37	50	63	ms	TOPT-1
Reset Timeout Period (T2)	74	100	126	ms	TOPT-2
Reset Timeout Period (T3)	148	200	252	ms	TOPT-3
Reset Timeout Period (T4)	296	400	504	ms	TOPT-4

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V1 = 1.6V to 5.5V; T_A = -40ºC to +85ºC; unless otherwise noted. Typical values are at T_A =+25ºC					
V3 RESET COMPARATOR INPUT					
V3 Input Threshold	490	500	510	mV	
V3 Input Current	-50		50	nA	T_A = +25ºC
V3 Threshold Hysteresis		1.5		mV	
MRIB - MANUAL RESET INPUT					
MRIB Input Threshold			0.4	V	Vil
MRIB Input Threshold	0.8*V1			V	Vih
MRIB Minimum Input Pulse Width	1			us	
MRIB Glitch Rejection		150		ns	
MRIB to RST/RSTB Delay		100		ns	
MRIB Pull-Up Resistance	30	55	85	kΩ	
WDI - WATCHDOG INPUT					
Watchdog Timeout Period	1.2	1.6	2	sec	
WDI Pulse Width	0.1			us	
WDI Input Threshold			0.4	V	Vil
WDI Input Threshold	0.8*V1			V	Vih
WDI Input Current	-500		500	nA	WDI = 0.0V or V1
RESET / WATCHDOG OUTPUTS		**RSTB / WDOB**			
RSTB (CMOS or OD)			0.4	V	V1 = Vth1 - 0.1V, Isink = 1mA, output asserted
RSTB (CMOS)	0.8*V1			V	V1 = Vth1 + 0.1V, Isource = 1mA, output not asserted
WDOB (CMOS or OD)			0.4	V	WDI = 0.0V or V1, V1 > Vth1, V2 > Vth2, V3 > 0.5, MRIB float, Isink = 1mA, WDOB output asserted
WDOB (CMOS)	0.8*V1			V	V1 > Vth1, V2 > Vth2, V3 > 0.5, MRIB float, WDOB not asserted, Isource = 1mA
RSTB / WDOB Output OD Leakage Current		2		nA	T_A = +25ºC

Pin #	Name	Description
1	V1	First supply voltage input. Also powers internal circuitry. Trip threshold voltage internally set.
2	V2	Second supply voltage input. Trip threshold voltage internally set.
3	WDI	Watch-Dog Input pin. When no transition is detected at the WDI pin for the duration of WDI timeout period, reset is asserted. RSTB output is used to signal watchdog timeout overflow -- RSTB output pulses high/low (depending on the active reset polarity) for the reset timeout period after each watchdog timeout overflow. WDOB remains at “LOW” logic level after watchdog timeout period is expired and it remains “LOW” until WDI makes a transition. RSTB output is not affected by the watchdog functionality. The watchdog timer clears whenever the reset is asserted or manual reset is asserted or a transition is observed at WDI pin.
4	V3	Input for the third supply voltage. Trip threshold is 0.5V.
5	WDOB	Watch Dog Output. Open-Drain or CMOS, active LOW. If WDI remains at “HIGH” or “LOW” logic level for longer than the watchdog timeout period, the internal watchdog timer overflows and WDOB is asserted. WDOB does not de-assert until the watchdog is cleared via transition at the WDI pin. Another scenario for WDOB to assert is when the reset output is asserted due to an under-voltage V1, V2, V3 condition. WDO de-asserts without a reset timeout period. Floating WDI will not disable watchdog timer in devices with dedicated WDOB output. Open-drain WDOB outputs require an external pull-up resistor. CMOS outputs are referenced to V1.
6	GND	Common ground reference pin.
7	MRIB	Manual Reset Input pin. Active low. It has an internal pull-up resistor. Reset asserted when MRIB is pulled low and is kept asserted for 200ms after MRIB is released or pulled high. Leave open if not used.
8	RSTB	Reset output. Open-Drain or CMOS, active low. Reset is asserted when any of the three supply inputs is below its trip threshold. It stays asserted for 200 ms (typical / default) after the last supply input traverses its trip threshold. Reset is guaranteed to be in the correct state for V1>0.9V. RSTB asserts when V1 or V2 or V3 drop below their corresponding reset thresholds, or MRIB is pulled “LOW”. RSTB remains asserted for the reset timeout period after V1 and V2 and V3 exceed their corresponding reset thresholds or MRIB goes “LOW” to “HIGH”. Open-drain outputs require an external pull-up resistor. CMOS outputs are referenced to V1.



Block Diagram

The SP6339 and SP6341 include a low-voltage precision bandgap reference, three precision comparators, an oscillator, a digital counter chain, a logic control block, trimmed resistor divider chains and additional supporting circuitry. The family is designed to supervise up to 3 independent supply voltages. V1 and V2 supply inputs have their resistor dividers on the chip. Their trip thresholds are factory trimmed. The V3 input allows users to customize an additional supply threshold to be monitored by means of an external resistor divider. The parts are furnished with manual reset and watchdog output functionalities. The watchdog functionality cannot be disabled.

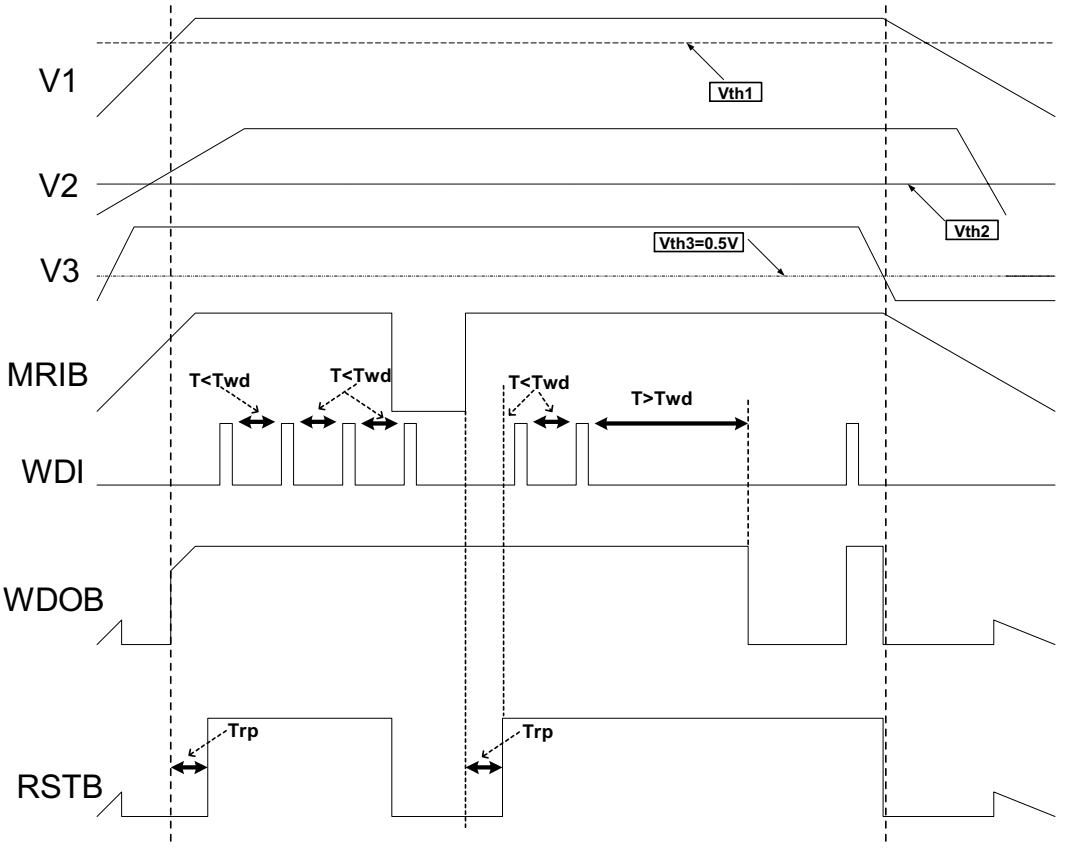
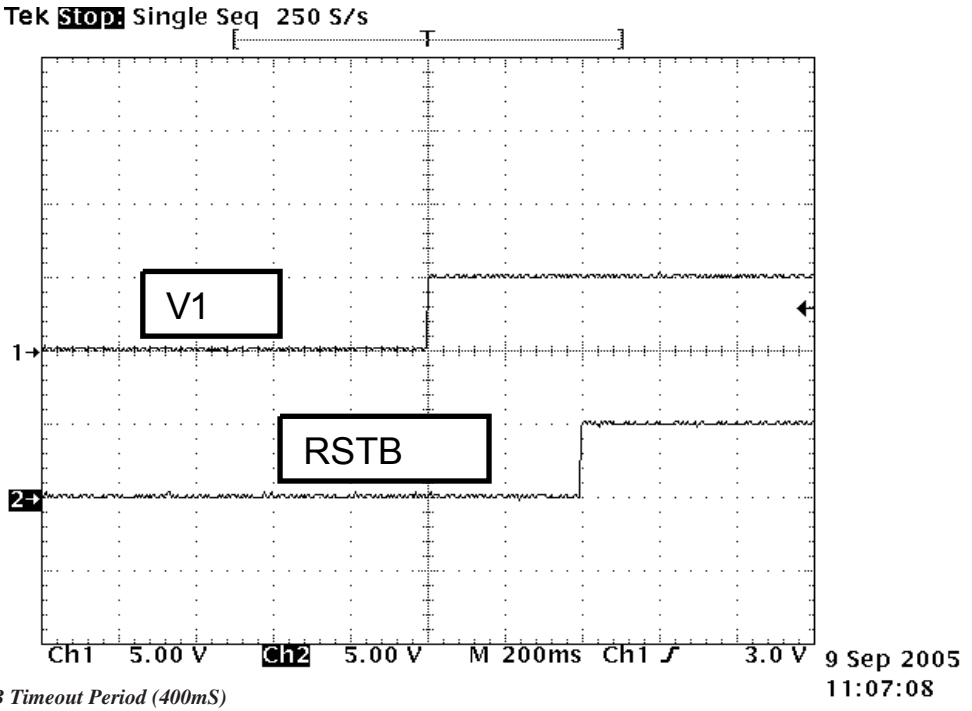
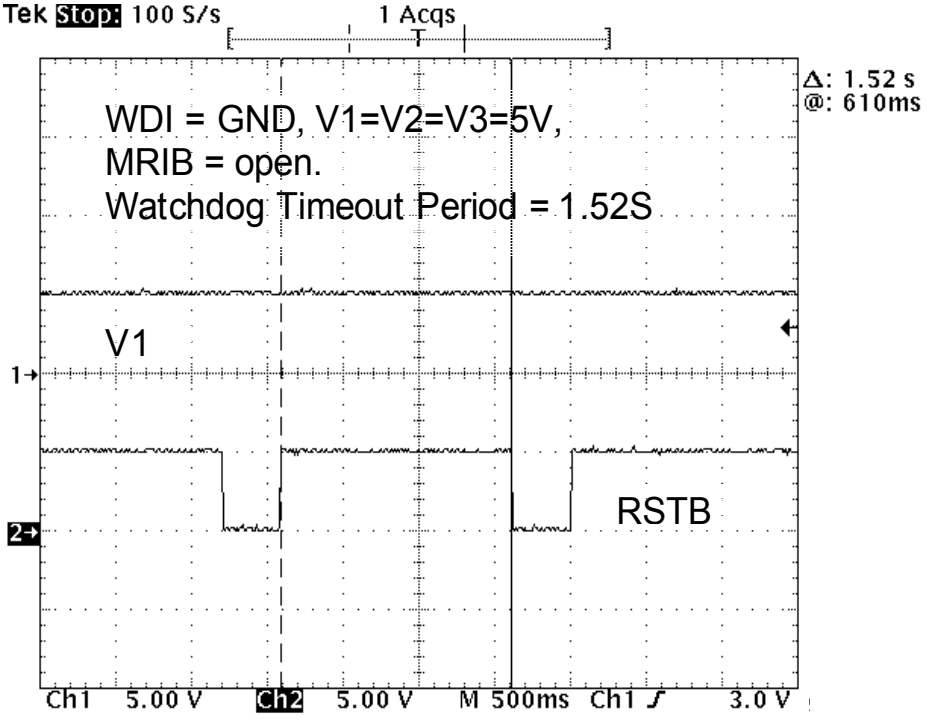


Figure 1: functionality of the SP6339 and SP6341.

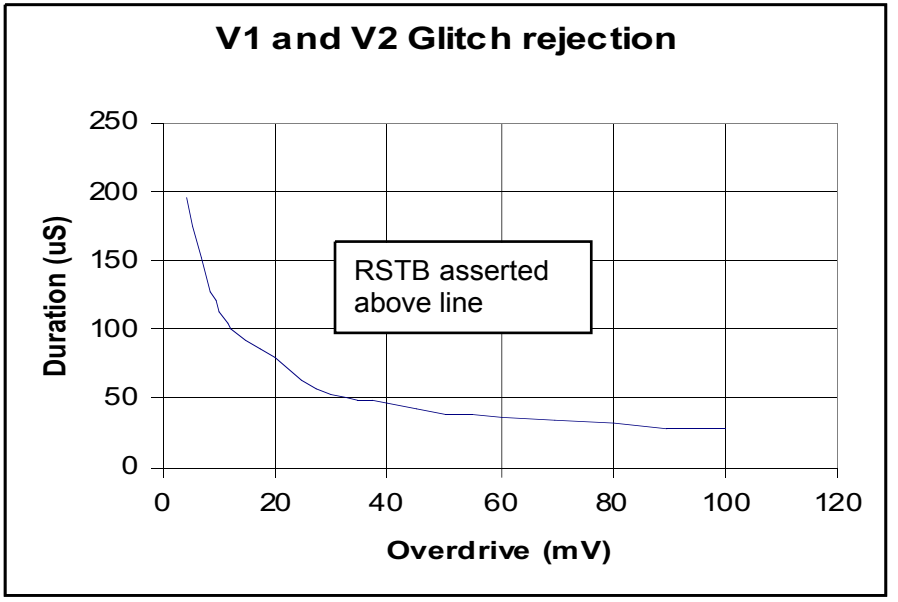
- V1 > Vth1, V2 > Vth2 , and V3 > Vth3 (all supplies over their corresponding thresholds)----> RSTB is de-asserted after reset timeout period (Trp) & WDOB de-asserts immediately without waiting for reset timeout period.
- MRIB goes to “LOW” to force “Reset” ----> RSTB is asserted immediately & WDOB is not affected by MRIB and is not asserted.
- WDI keeps making transitions within watchdog timeout period (t<Twd) ----> neither RSTB nor WDOB changes state.
- One of the supplies drops below its corresponding threshold (in this case V3) ----> RSTB is asserted immediately & WDOB is asserted immediately too. Whenever V1, V2, V3 are below their specified thresholds WDOB is asserted.



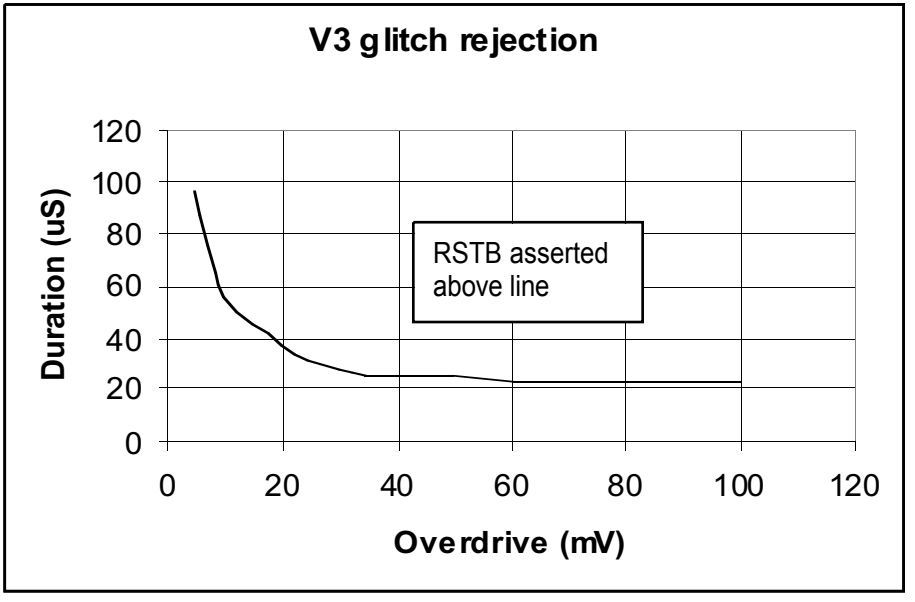
RESETB Timeout Period (400mS)



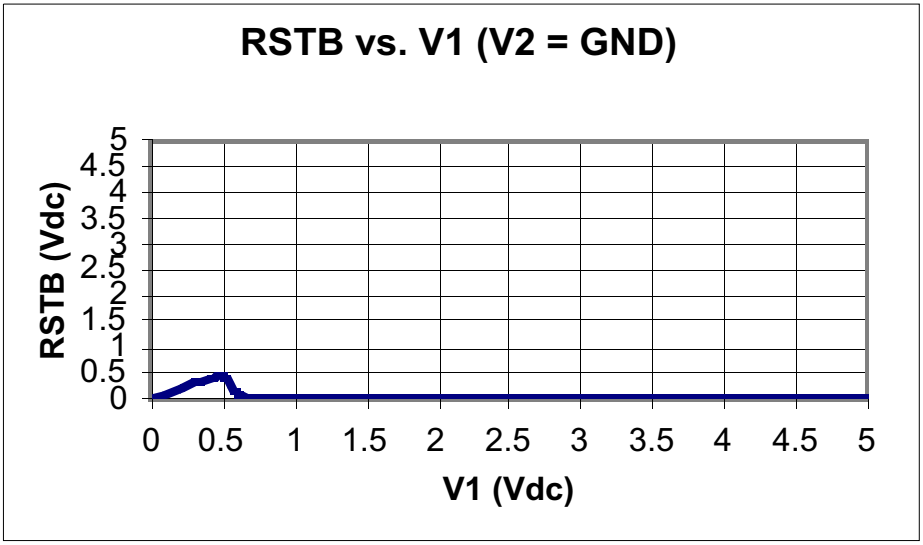
SP6339Watchdog Timeout Period



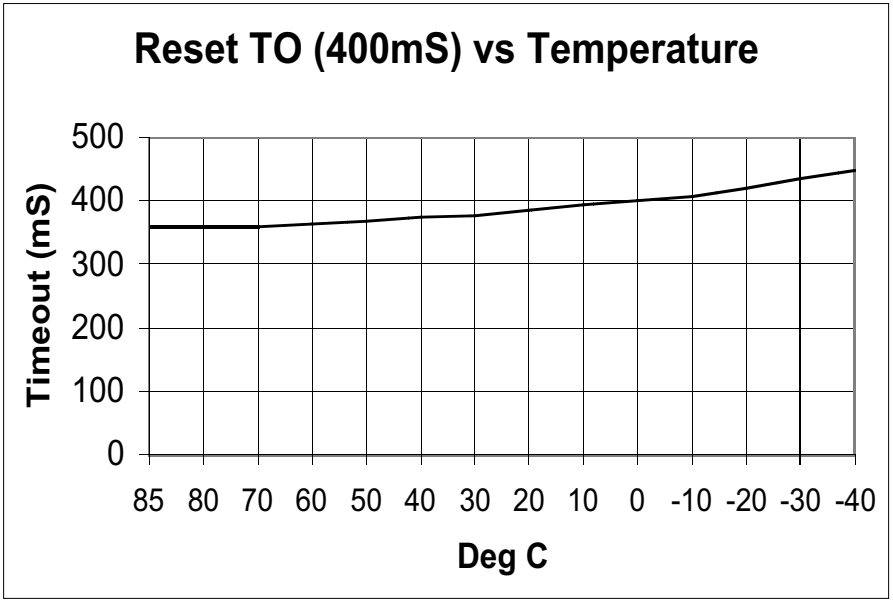
V1 and V2 Glitch Rejection



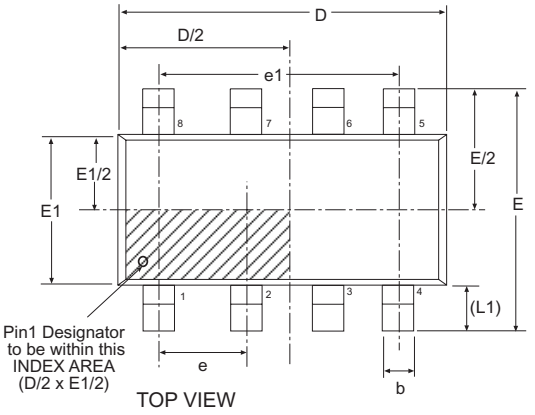
V3Glitch Rejection

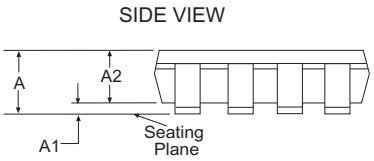


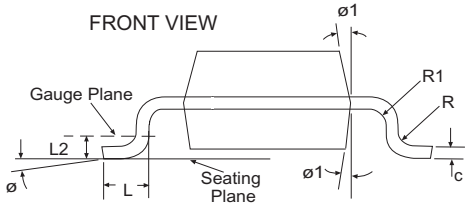
Reset Good



Reset Timeout vs. Temperature







8 Pin TSOT JEDEC MO-193 Variation BA						
SYMBOL	Dimensions in Millimeters: Controlling Dimension			Dimensions in Inches Conversion Factor: 1 Inch = 25.40 mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.10	-	-	0.043
A1	0.00	-	0.10	0.000	-	0.004
A2	0.70	0.90	1.00	0.028	0.036	0.039
c	0.08	-	0.20	0.003	-	0.008
D	2.90 BSC			0.114 BSC		
E	2.80 BSC			0.110 BSC		
E1	1.60 BSC			0.063 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF			0.024 REF		
L2	0.25 BSC			0.010 BSC		
Ø	0˚	4º	8º	0º	4º	8º
Ø1	4˚	10º	12º	4º	10º	12º
R	0.10	-	-	0.004	-	-
R1	0.10	-	0.25	0.004	-	0.010
b	0.22	-	0.38	0.009	-	0.015
e	0.65 BSC			0.026 BSC		
e1	1.95 BSC			0.077 BSC		
SIPEX Pkg Signoff Date/Rev:				JL Oct3-05 / Rev A		

Part Naming Nomenclature

SP63N - Th1 - Th2 - TOPT

TOPT

- A -- 50 ms
- B -- 100 ms
- C -- 200 ms
- D -- 400 ms

Th2

- A -- 0.788 V
- B -- 0.833 V
- C -- 1.050 V
- D -- 1.110 V
- E -- 1.313 V
- F -- 1.388 V
- G -- 1.575 V
- H -- 1.665 V
- I -- 2.188 V
- J -- 2.313 V

Example:
JZJD means:
SP6339 in TSOT-8 lead package
V1 Threshold is 4.625V
V2 Threshold is 2.313V
Reset Timeout is 400ms

Th1

- Z -- 4.625 V
- Y -- 4.375 V
- X -- 3.075 V
- W -- 2.925 V
- V -- 2.625 V
- U -- 2.320 V
- T -- 2.190 V
- S -- 1.670 V
- R -- 1.580 V

SP63N

- A 30 -- Quad Sp, MR, WDI, OD RSTB
- B 31 -- Quad Sp, OD RSTB
- C 32 -- Quad Sp, MR, WDI, CMOS RSTB
- D 33 -- Quad Sp, CMOS RSTB
- E 34 -- Quad Sp, MR, WDI, CMOS RST
- F 35 -- Quad Sp, CMOS RST
- G 36 -- Triple Sp, WDI, PF, OD RSTB
- H 37 -- Triple Sp, WDI, PF, CMOS RSTB
- I 38 -- Triple Sp, WDI, PF, CMOS RST
- J 39 -- Triple Sp, MR, WDI, OD RSTB - WDOB
- K 40 -- Dual Sp, WDI, OD RSTB - WDOB
- L 41 -- Triple Sp, WDI, PF, CMOS RSTB - WDOB
- M 42 -- Dual Sp, WDI, CMOS RSTB - WDOB

Model	Temperature Range	Package Type
SP6339EK1-L-X-X-X	-40°C to +85°C	Lead Free 8-Pin TSOT
SP6339EK1-L-X-X-X/TR	-40°C to +85°C	Lead Free 8-Pin TSOT
SP6341EK1-L-X-X-X	-40°C to +85°C	Lead Free 8-Pin TSOT
SP6341EK1-L-X-X-X/TR	-40°C to +85°C	Lead Free 8-Pin TSOT

Available in lead free packaging only.

/TR = Tape and Reel

Pack quantity 2,500 for TSOT.

Contact Factory for availability of particular voltage threshold and reset timeout options. Note that the Ordering Information denoting those options corresponds to the Part Naming Nomenclature shown on the previous page.

Ordering example: SP6339EK1-L-W-G-C/TR == W -- 2.925V for Voltage Threshold 1; G -- 1.575V for Voltage Threshold 2; and C -- 200ms reset timeout.

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Appendix and Web Link Information

For further assistance:

Email:	Sipexsupport@sipex.com
WWW Support page:	http://www.sipex.com/content.aspx?p=support
Sipex Application Notes:	http://www.sipex.com/applicationNotes.aspx
Product Change Notices:	http://www.sipex.com/content.aspx?p=pcn

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Headquarters and
Sales Office
233 South Hillview Drive
Milpitas, CA95035
tel: (408) 934-7500
faX: (408) 935-7600

The following sections contain information which is more changeable in nature and is therefore generated as appendices.

1) **Package Outline Drawings**
2) **Ordering Information**

If Available:

3) **Frequently Asked Questions**
4) **Evaluation Board Manuals**
5) **Reliability Reports**
6) **Product Characterization Reports**
7) **Application Notes for this product**
8) **Design Solutions for this product**

Product Lines

Power Management
- Boost Regulators
- Buck Regulators
- Charge Pumps
- LED Drivers
- Linear Regulators
- Power Blox™
- PWM Controllers
- References
- Supervisors
- USB Vbus Switches

Interface
- Multiprotocol
- RS232
- RS422
- RS485
- USB

Optical Storage
- Advanced Power Control
- Photo Detector IC

SP6341 product details

You are here : Home : Products : Supervisors :

Triple micropower Supervisory Circuit with Manual Reset and Watchdog

Features

- Low operating voltage of 1.6V
- Low operating current of 20uA typical
- Monitors up to 3 supplies simultaneously
- Adjustable inputs monitor down to 0.5V
- Reset asserted down to 0.9V
- 2% accuracy over temperature range
- CMOS RSTB output
- 4 Reset Timeout Periods: 50ms, 100ms, 200ms and 400 ms
- Watch Dog timer Functionality -- WDI
- Independent OD watchdog output (Active Low) -- WDOB
- 8 Pin TSOT package

Quick Links
- Download Datasheet
- Check Price Availability

Design-In Supp
- Email: Tech
- Supervisors Selector
- Applications
- Evaluation B
- Quality Infor
- Part Nomen
- SP6341 FAQ

Representative Samples are available using the SP6339 for V1= 4.625V, V2=2.313V, V3 = V4 (Factory Set) = 0.5V and 200ms Reset Timeout. **** Contact factory for availability of particular threshold and reset timeout options.****

Ordering Part Number

Part Number	Package Code	RoHS	MIN. Temp. (° C)	MAX. Temp.(° C)	Status	Buy
SP6341EK1-L SUPERVISORS TRIPLE						
SP6341 : CONTACT FACTORY FOR VOLTAGE OPTIONSNew!	TSOT8	▪	-40	85	CF_	

Part Status Legend

Active - the part is released for sale, standard product.

EOL (End of Life) - the part is no longer being manufactured, there may or may not be inventory still in stock.

CF (Contact Factory) - the part is still active but customers should check with the factory for availability. Longer lead-times may apply.

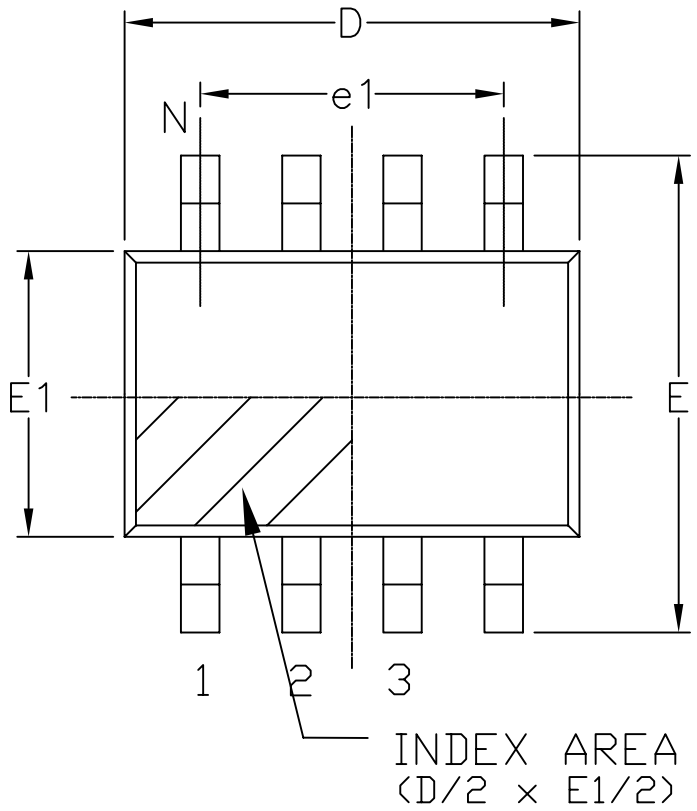
PRE (Pre-introduction) - the part has not been introduced or the part number is an early version available for sample only.

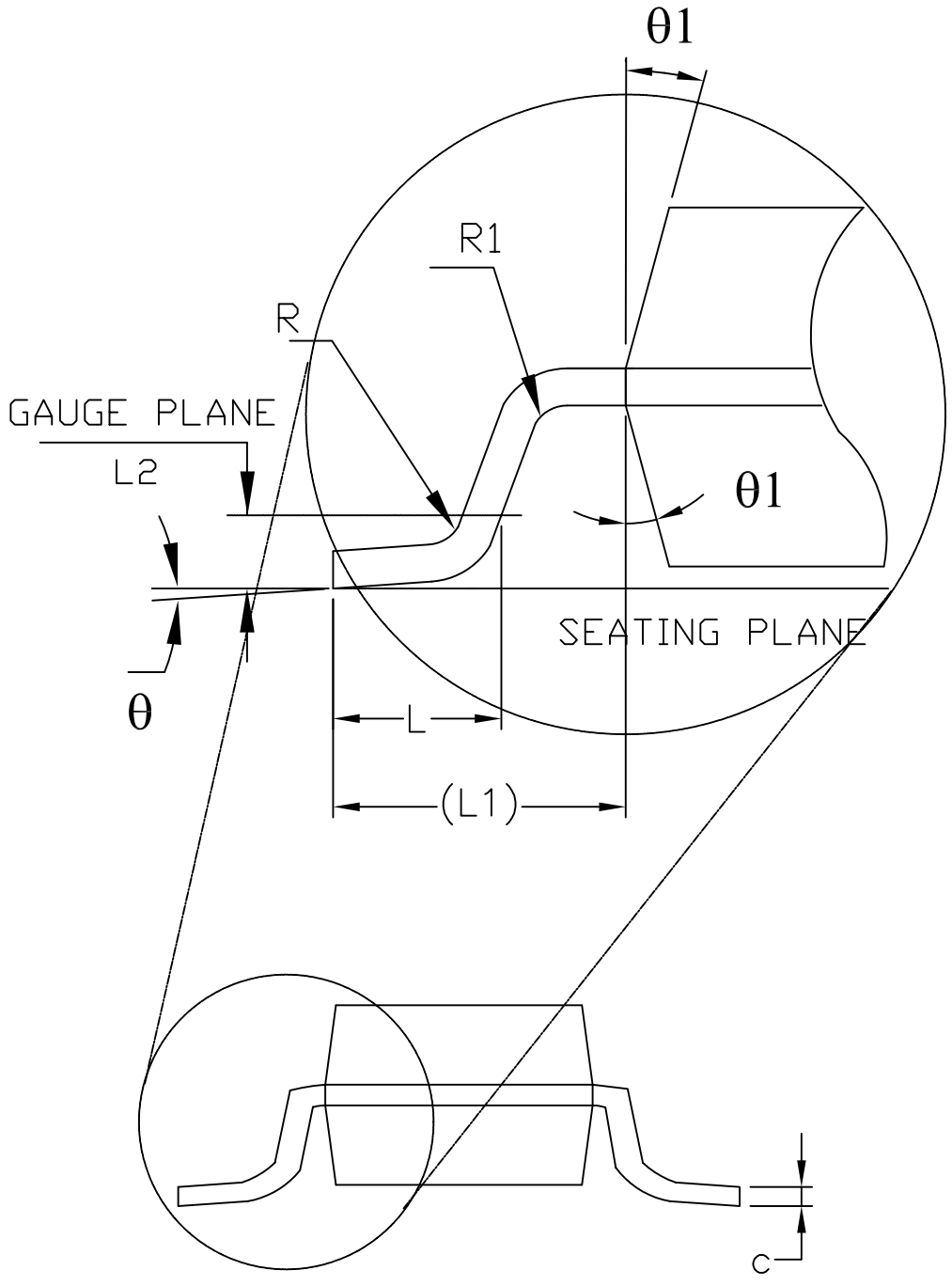
OBS (Obsolete) - the part is no longer being manufactured and may not be ordered.

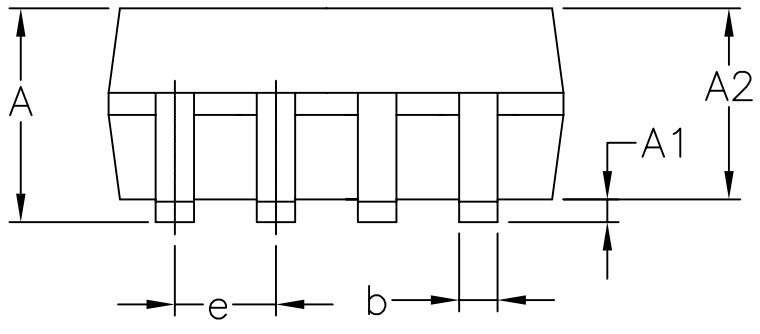
NRND (Not Recommended for New Designs) - the part is not recommended for new designs.

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	10/03/05	JL
B	DRAWING FORMAT MODIFICATION	09/13/06	JL

Top View







Side View

Front View

8 Pin TSOT JEDEC MO-193 Variation BA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.10	—	—	0.043
A1	0.00	—	0.10	0.000	—	0.004
A2	0.70	0.90	1.00	0.028	0.036	0.039
b	0.22	—	0.38	0.009	—	0.015
c	0.08	—	0.20	0.003	—	0.008
D	2.90 BSC			0.114 BSC		
E	2.80 BSC			0.110 BSC		
E1	1.60 BSC			0.063 BSC		
e	0.65 BSC			0.026 BSC		
e1	1.95 BSC			0.077 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF			0.024 REF		
L2	0.25 BSC			0.010 BSC		
R	0.10	—	—	0.004	—	—
R1	0.10	—	0.25	0.004	—	0.010
θ	0°	4°	8°	0°	4°	8°
θ1	4°	10°	12°	4°	10°	12°
N	8			8		

Solved by Sipex™

SIPEX CORPORATION

8 PIN TSOT PACKAGE OUTLINE

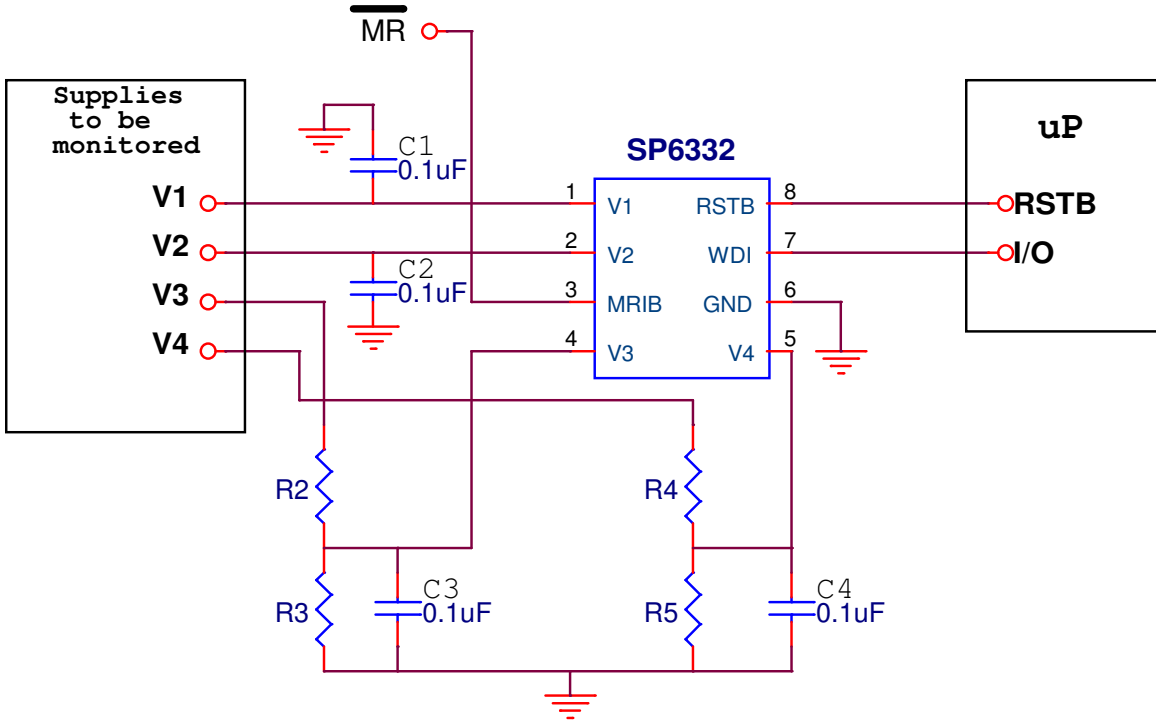
Packaging Approval:		Drawing No: 8-PIN TSOT	
By: JL	Date: 09/13/06	Revision: B	Sheet: 1 OF 1

APPLICATION NOTE ANP14

Understanding and Selecting a Multi-Voltage Supervisor Featuring the SP6330 Family

Introduction

The primary function of a microprocessor (µP) supervisor circuit is to ensure that the input supply voltage of a microprocessor is at proper levels during power up, power down and brownout conditions. If the input supply voltage to a microprocessor is below its required operating range, it could cause code-execution errors, memory corruption and latch up. The supervisor will constantly monitor the input supply to the microprocessor, and in the event this supply voltage falls below a certain threshold, the RESET output will be asserted. Many of today's power products require several different voltage rails for powering various components. The microprocessor itself can have a separate core voltage and logic voltage. Other components such as DSPs, ASICs and microcontrollers can have their own unique voltage requirements. To service this demand of monitoring multi-voltage systems, Sipex has developed the SP6330 family. The SP6330 family is a series of multi-voltage supervisors that offer monitoring of up to 4 separate supplies and are equipped with specialized features. A complete listing of products and features are listed in Figure 4 at the end of this note.



SP6332 typical applications circuit for monitoring 4 supplies with Master Reset, Watchdog input and CMOS Reset output

Inputs to the SP6330 Family

The SP6330 family has the ability to monitor up to 4 different voltages. Two of these inputs (V1 and V2) have precision factory-set thresholds while the remaining two inputs (V3 and V4) are adjustable. V3 and V4 inputs allow the user to customize two additional supply thresholds by means of an external divider. The threshold for V3 and V4 inputs is 0.5Volts. The V1 input supplies power to the device and will have the highest threshold for a given application; its minimum operating voltage for is 1.8V. The factory set threshold range for V1 and V2 inputs are shown in Figure 1.

V1 Typical Threshold	V2 Typical Threshold
4.625	2.313
4.375	2.188
3.075	1.665
2.925	1.575
2.625	1.388
2.320	1.313
2.190	1.110
1.670	1.050
1.580	0.833
	0.788

Figure 1

Reset Output – RST or RSTB

The reset output can be either active low or active high depending on each device. The reset output can also be either open-drain or push-pull outputs. The open drain output requires an external pull-up resistor to V1 for normal operation. The output high voltage (V_{OH}) of the reset output will be approximately equal to the V1 input voltage.

Reset Timeout Period

The reset timeout period is a built-in time delay for the reset output. This timeout period is activated at power up or when all monitored voltages have risen above their respective thresholds. Reset timeout period for the SP6330 family is offered in four different time intervals: 50ms, 100ms, 200ms and 400ms. The actual selection of timeout period depends on the applications requirements of the system voltage settle time. The reset timeout period is used to ensure that all voltage rails and system clocks have stabilized prior to executing code to prevent errors or data corruption.

Manual Reset Input (Active Low) – MRIB

The manual reset input allows the user to manually trigger a reset when monitored voltages are within tolerance. This is useful for resetting the microprocessor when it locks up due to software issues. A push-button type switch can be used to allow the user to trigger a reset externally. However, since a push button switch will bounce several times, a debounce element is needed. The manual reset input signal may also be a logic signal from an I/O line, watchdog timer or a power fail output.

Watchdog Input – WDI

The watchdog checks for proper software execution. If the software locks up or enters into an unwanted, loop the watchdog timer can either assert a reset output or a watchdog output. Some members of the SP6330 family offer a watchdog output while others do not. The watchdog has an internal timer that has a typical watchdog timeout period of 1.6 seconds. If the watchdog input (WDI) does not detect a transition within 1.6 seconds, a reset or watchdog output (WDO) will be generated. The watchdog input is usually connected to an I/O line for monitoring software activity. The watchdog circuit is useful for generating a reset or Non-Maskable Interrupt (NMI) signal during software lock up conditions without human intervention. Floating the WDI will disable the watchdog feature.

Watchdog Output (Active Low) – WDOB

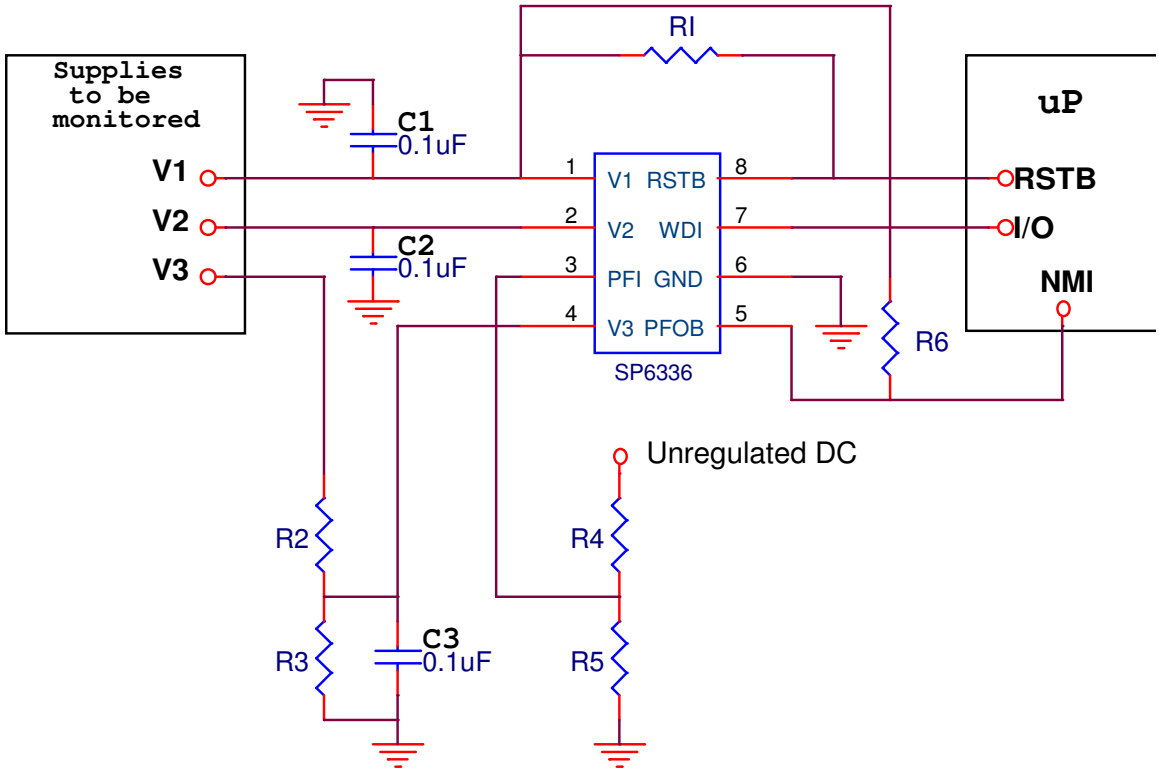
The Watchdog output is active low and can be either an open drain or push-pull output. If WDI remains at “HIGH” or “LOW” logic level for longer than the watchdog timeout period, the internal watchdog timer overflows and the WDOB will be asserted. Additionally, if the reset output is asserted due to an under-voltage condition, at any voltage input the WDOB would also be asserted. Floating WDI will not disable the watchdog timer in devices with dedicated WDOB output.

Power Fail Input (PFI)

The power fail input is used to monitor the unregulated DC voltage or other upstream voltage and to alert the system that a brownout or power failure is imminent. When the PFI input is tripped, it can inform the system to start a power-down routine in order to save important data before a reset output is asserted. The power fail input has a threshold of 0.5V. By using a voltage divider the user can monitor any upstream voltage. Connect PFI to V1 or GND if not used.

Power Fail Output (Active Low) - PFOB

The PFOB pin is an open drain, active low output. When the input voltage at PFI is <0.5V, PFOB will be asserted.



SP6336 Typical Applications circuit for monitoring 3 supplies with Power Fail Input / Output function and open drain RESET output

Glitch Immunity at Voltage Inputs

The V1, V2, V3 and V4 inputs have a built-in glitch immunity feature that prevents nuisance resets during normal operation. Noise and normal voltage transients can cause these unwanted resets without some type of glitch immunity. Figure 2 shows the combination of voltage overdrive and duration that will not cause a reset for V1 and V2 inputs. Figure 3 shows the same data as applied to the V3 and V4 inputs. Adding a small bypass capacitor to voltage inputs can improve glitch rejection for very harsh environments.

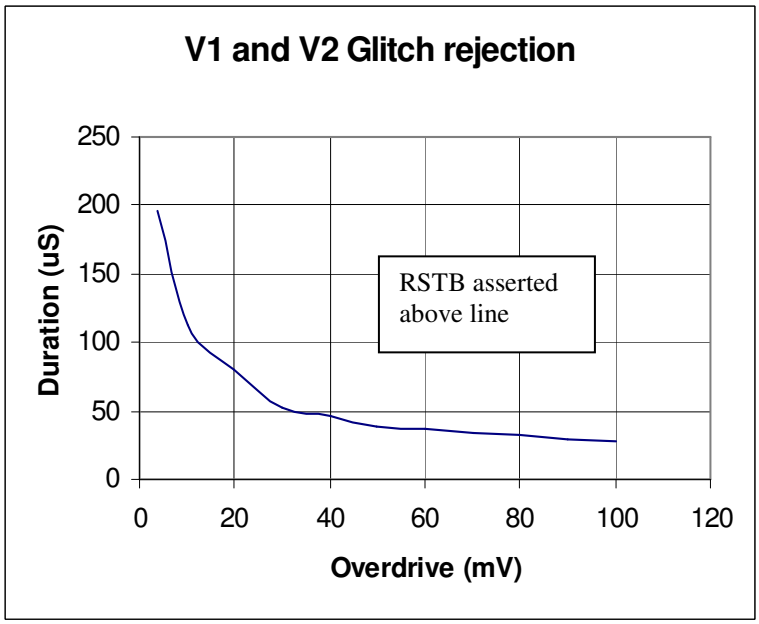


Figure 2

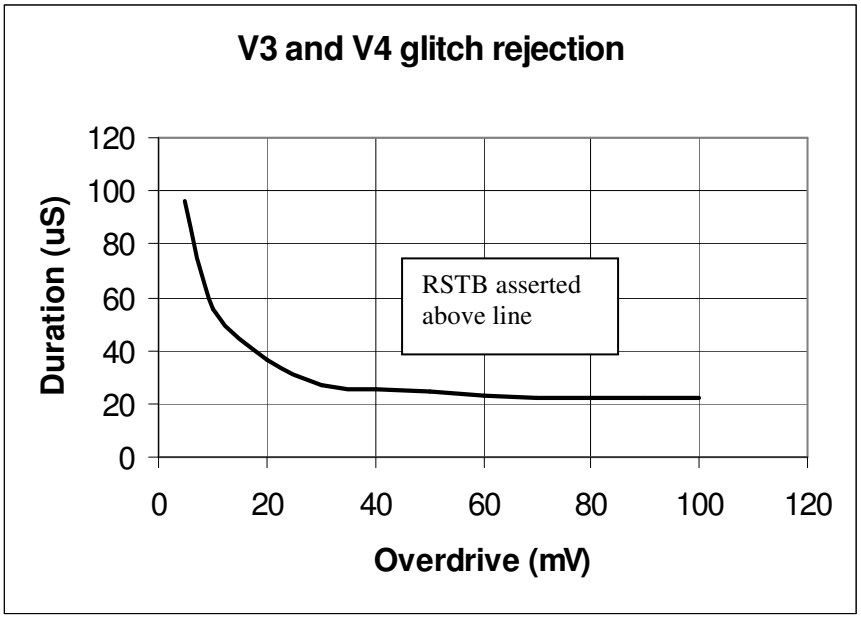


Figure 3

SP633X Features

- Quad, triple or dual supply monitoring
- Very low operating voltage down to 1.6V
- Low 20µA typical operating current
- Adjustable inputs monitor down to 0.5V
- Open drain or CMOS reset outputs
- 4 reset timeout periods: 50ms, 100ms, 200ms and 400ms
- Glitch immunity inputs
- Tiny 6 pin or 8 pin TSOT package

P/N	V1	V2	V3	V4	Reset	Reset	MRIB	WDI	WDOB	WDOB	PFI	PFOB	Package
					Output	Active			OD	CMOS			
SP6330	X	X	X	X	OD	LOW	X	X					8-TSOT
SP6332	X	X	X	X	CMOS	LOW	X	X					8-TSOT
SP6334	X	X	X	X	CMOS	HIGH	X	X					8-TSOT
SP6331	X	X	X	X	OD	LOW							6-TSOT
SP6333	X	X	X	X	CMOS	LOW							6-TSOT
SP6335	X	X	X	X	CMOS	HIGH							6-TSOT
SP6336	X	X	X		OD	LOW		X			X	X	8-TSOT
SP6337	X	X	X		CMOS	LOW		X			X	X	8-TSOT
SP6338	X	X	X		CMOS	HIGH		X			X	X	8-TSOT
SP6339	X	X	X		OD	LOW	X	X	X				8-TSOT
SP6341	X	X	X		CMOS	LOW	X	X		X			8-TSOT
SP6340	X	X			OD	LOW		X	X				6-TSOT
SP6342	X	X			CMOS	LOW		X		X			6-TSOT

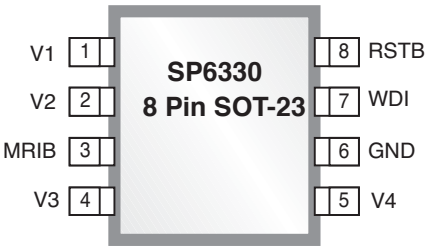
Figure 4: Product Selection Guide

FAQ SP6330 - SP6342

Dual/Triple/Quad μPower Supervisory Circuit Family

FEATURES

- Low operating voltage of 1.8V
- Low operating current of 20μA typical
- Monitors up to four supplies simultaneously
- Adjustable inputs monitor down to 0.5V
- Reset asserted down to 0.9V
- 2% accuracy over temperature range
- Power Fail function
- Open Drain (OD) or CMOS RSTB output or CMOS RST output
- 200ms Reset Timeout Period
- Watch Dog Timer Function
- Independent Open Drain Watchdog Output
- Manual Reset Input
- SOT23-6/8 packages



Open Drain $\overline{\text{RESET}}$

SEE PAGE 3 FOR OTHER AVAILABLE PINOUTS

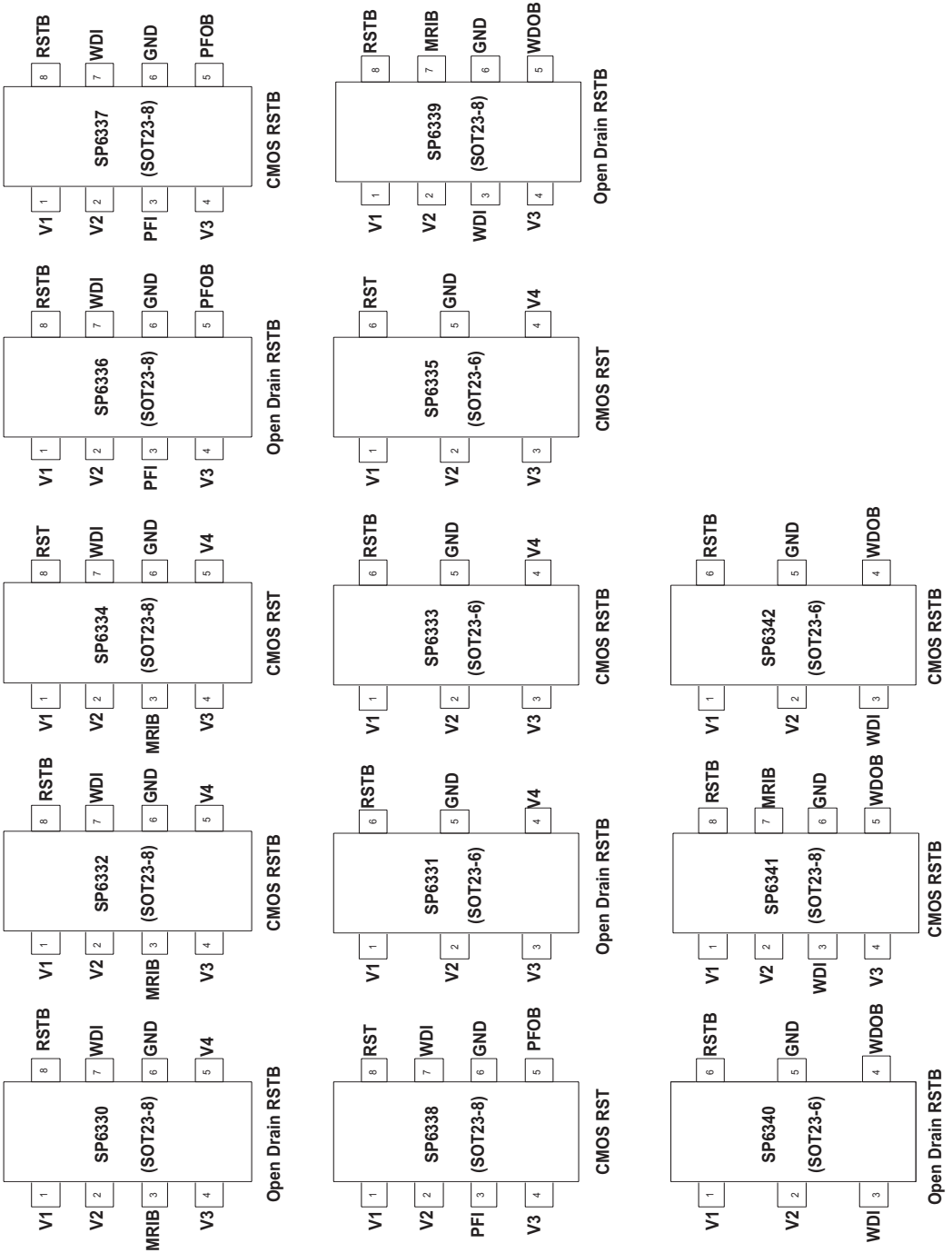
Available in Lead Free Packaging

DESCRIPTION

SP6330-SP6342 Dual/Triple/Quad Power Supervisory Circuit Family is a family of microprocessor reset supervisory circuits with multiple reset voltages. The SP6330 family provides low voltage monitoring ability for up-to four supplies with two precision factory-set thresholds and two user defined custom thresholds. These circuits perform a single function: if any of the input supply voltages drops below its associated threshold, reset outputs are asserted. Some of the products in the family offer manual reset,power fail and watchdog functionalities. The SP63XX family includes a low-voltage precision bandgap reference, four precision comparators, an oscillator, a digital counter chain, a logic control block, trimmed resistor divider chains and additional supporting circuitry. V1 and V2 supply inputs have their resistor dividers on the chip. Their trip thresholds are factory trimmed. V3 and V4 inputs allow user to customize two additional supply thresholds to be monitored by means of external resistor dividers. Some members of the family are furnished with manual reset, power fail indication, watchdog functionalities.SP6330 thru SP6342 are housed in a 6-pin or 8-pin SOT23 package. All devices are fully specified over -40°C to +85°C temperature range.

FEATURE MAPPING DIAGRAM

PART NUMBER	V1	V2	V3	V4	Reset	Manual Reset Input BAR	WatchDog Input	WatchDog Output BAR	Power Fail Input	Power Fail Output BAR	# of Pins	Data-sheet Group
SP6330	√	√	√	-	OD Active Low	√	√	-	-	-	8	1
SP6331	√	√	√	√	OD Active Low	-	-	-	-	-	6	5
SP6332	√	√	√	-	CMOS Active Low	√	√	-	-	-	8	1
SP6333	√	√	√	√	CMOS Active Low	-	-	-	-	-	6	5
SP6334	√	√	√	-	CMOS Active High	√	√	-	-	-	8	1
SP6335	√	√	√	√	CMOS Active High	-	-	-	-	-	6	5
SP6336	√	√	√	-	OD Active Low	-	√	-	√	√	8	2
SP6337	√	√	√	-	CMOS Active Low	-	√	-	√	√	8	2
SP6338	√	√	√	-	CMOS Active High	-	√	-	√	√	8	2
SP6339	√	√	√	-	OD Active Low	√	√	OD Active Low	-	-	8	3
SP6340	√	√	-	-	OD Active Low	-	√	OD Active Low	-	-	6	4
SP6341	√	√	√	-	CMOS Active Low	√	√	CMOS Active Low	-	-	8	3
SP6342	√	√	-	-	CMOS Active Low	-	√	CMOS Active Low	-	-	6	4



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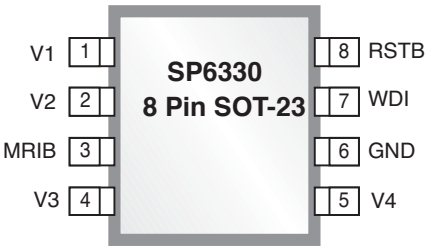

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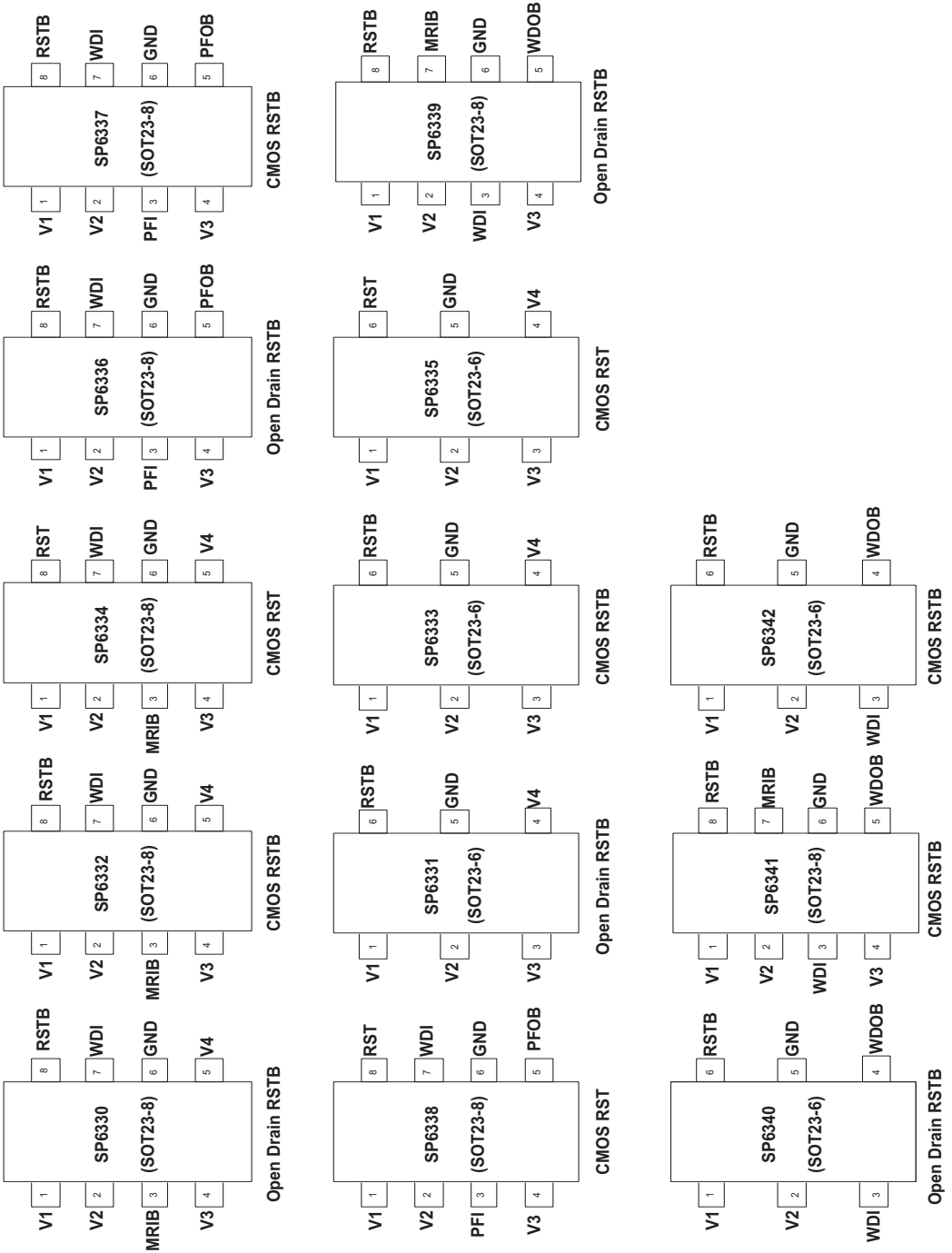
SP6332	√	√	√	-	CMOS Active Low	√	√	-	-	-	8	1
SP6333	√	√	√	√	CMOS Active Low	-	-	-	-	-	6	5
SP6334	√	√	√	-	CMOS Active High	√	√	-	-	-	8	1
SP6335	√	√	√	√	CMOS Active High	-	-	-	-	-	6	5
SP6336	√	√	√	-	OD Active Low	-	√	-	√	√	8	2
SP6337	√	√	√	-	CMOS Active Low	-	√	-	√	√	8	2
SP6338	√	√	√	-	CMOS Active High	-	√	-	√	√	8	2
SP6339	√	√	√	-	OD Active Low	√	√	OD Active Low	-	-	8	3
SP6340	√	√	-	-	OD Active Low	-	√	OD Active Low	-	-	6	4
SP6341	√	√	√	-	CMOS Active Low	√	√	CMOS Active Low	-	-	8	3
SP6342	√	√	-	-	CMOS Active Low	-	√	CMOS Active Low	-	-	6	4



Reliability and Qualification Report

SP6330

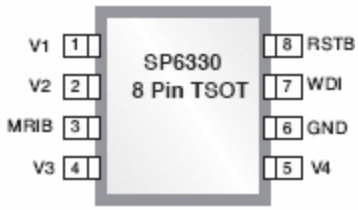
Prepared by: G. West
Manager, Quality Assurance
Date: April 7, 2006

Reviewed by: Fred Claussen
VP Quality & Reliability
Date: April 7, 2006

Table Of Contents

Device Description:

SP6330-SP6332- SP6334 Quad Power Supervisory Circuit Family is a family of microprocessor reset supervisory circuits with multiple reset voltages. The family provides low voltage monitoring ability for up-to four supplies with two precision factory-set thresholds and two user defined custom thresholds. These circuits perform a single function: if any of the input supply voltages drops below its associated threshold, reset outputs are asserted. The SP6330, SP6332, and SP6334 are packaged in an 8-pin TSOT package. All devices are fully specified over -40ºC to +85ºC temperature range.



SP6330 Pin Out

Manufacturing Information:

Products:	SP6330
Description:	Quad Power Supervisory Circuit
Mask Set(s):	MS1512AZ
Process:	CMOS
Process Name:	PBC4
Wafer Manufacturer:	Polar Semiconductor, Inc.
Assembly Location:	Carsem – Malaysia
Qualification Lot #'s:	3522A001A.11, 3638A001.8, 3638A001.6

Package Information:

Package Type: 8 pin TSOT
Die Size: 45 x 67 mil

Reliability Qualification Test Summary:

Stress Level	Device	Burn-In Temp	Sample Size	No. Fail
168Hrs	SP6330	125 °C	240	0
500Hrs	SP6330	125 °C	240	0
1000Hrs	SP6330	125 °C	240	0

Life Test

Life testing is conducted to determine if there are any fundamental reliability related failure mechanism(s) present in the device.

These failure mechanisms can be divided roughly into four groups:

1. Process or die related failures, such as oxide-related defects, metalization-related defects and diffusion-related defects.
2. Assembly-related defects such as chip mount wire bond or package-related failures.
3. Design related defects.
4. Miscellaneous, undetermined or application-induced failures.

Life Test Results

As part of the Sipex design qualification program, the Engineering group had subjected 80 parts from each of 3 lots of SP6330 for a 1000 hour reliability life test at 125° C.

168 hour Life test

240 parts of SP6330 parts were subjected to the life test profile and completed 168hr the test without any part failures.

500 hour Life test

The 240 parts of SP6330 we reintroduced to the second phase of the test, where the parts again showed successfully completing the 500-hour life test without any failures.

1000 hour Life test

The 240 parts of the SP6330 were reintroduced to the final phase of the test, where the parts again successfully completed 1000-hour life test without any shift on the process parameters.

FIT Rate Calculations

The FIT (failures in time) rate is the predicted number of failures per billion device-hours. This predicted value is based upon the:

1. Life Test conditions (time and temperature, device quantity and number of failures) are summarized under HTOL test table.
2. Activation Energy (E_a) of the potential failure modes.

The weighted Activation Energy, E_a, of observed failure mechanisms of Sipex products has been determined to be 0.8 eV.

Based on the above criteria, the FIT rates at 25°, 55° and 70°C operation at both 60% and 90% confidence levels for the **SP6330** product lines have been calculated and are listed below.

FIT Failure Rates SP6330 Product

Confidence Level	+25°C	+55°C	+70°C
60%	1.6	26.6	90.8
90%	4.1	68.4	233.1

1 FIT = 1 Failure per Billion Device-Hours

MTBF Calculation for SP6330 Product

Confidence Level	+25°C	+55°C	+70°C
60%	6.30E+08	3.75E+07	1.10E+07
90%	2.46E+08	1.46E+07	4.29E+06

ESD Testing

HBM ESD Testing - 5 units from each of three lots were subjected to 4000 V Human Body Model (HBM) ESD stress. Each pin was subjected to three positive and three negative pulses with respect to ground. All units passed testing after ESD stress.

Latch-up Testing - 5 units from each of three lots were subjected to latch-up testing at +/- 100mA. All units passed.