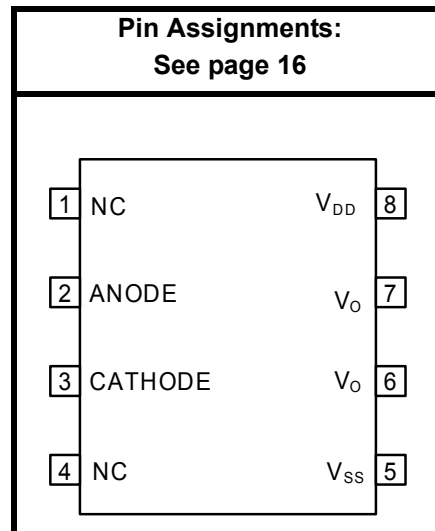# Si8220

2.5 AMP ISODRIVER WITH OPTO INPUT

Features

- Upgrade for HCPL 3120, TLP250, and similar opto-drivers
- 50 ns propagation delay (independent of input drive current)
- 14x tighter part-to-part matching versus opto-drivers
- 600 VDC (2.5 kV$_{RMS}$) output-to-input differential voltage
- 35 kV/s common-mode transient immunity
- Under-voltage lockout protection with hysteresis
- Resistant to temperature and aging effects
- Gate driver supply voltage: 8 V to 24 V
- Operating temperature range: –40 to +125 °C
- Cost-effective
- Pb-Free and RoHS Compliant

Applications

- IGBT/ MOSFET gate drives
- Industrial control systems
- Switch mode power supplies
- UPS systems
- Motor control drives

Pin Assignments:
See page 16

1	NC	V$_{DD}$	8
2	ANODE	V$_O$	7
3	CATHODE	V$_O$	6
4	NC	V$_{SS}$	5

Patent pending

Description

The Si8220 is a high-performance, pin-compatible upgrade for opto-coupled drivers, such as the HCPL-3120. It utilizes Silicon Laboratories' proprietary silicon isolation technology, which provides 600 Vdc (2.5 kVac$_{RMS}$) withstand voltage per UL1577. This technology enables higher performance, reduced variation with temperature and age, tighter part-to-part matching, and superior common-mode rejection compared to opto-isolated drivers. While the input circuit mimics the characteristics of an LED, less drive current is required, resulting in increased efficiency. Propagation delay time is independent of input drive current, resulting in consistently short propagation time, tighter unit-to-unit variation, and greater input circuit design flexibility.
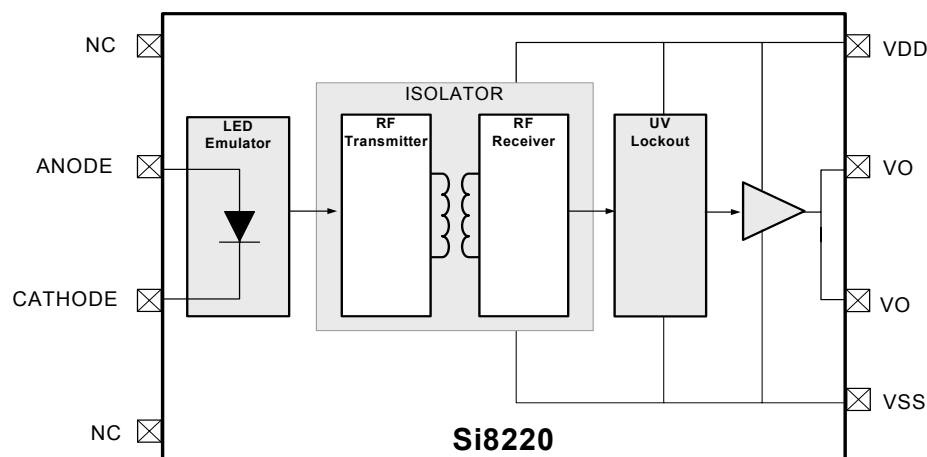
This information applies to a product under development. Its characteristics and specifications are subject to change without notice.

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Si8220

1. Electrical Specifications

Table 1. Absolute Maximum Ratings*

Parameter	Conditions	Min	Typ	Max	Units
Storage temperature	T_{STG}	–65	—	+150	°C
Ambient temperature under bias		–40	—	+125	°C
Supply voltage		–0.6	—	30	V
Input voltage		–0.5	—	V_{DD} + 0.5	V
Lead solder temperature (10 s)	$IF_{(AVG)}$	—	—	260	°C
Maximum isolation voltage	$(V_{DD} - V_{SS})$	—	—	3,000	V_{DC}
*Note: Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions specified in the operational sections of this data sheet.					

Table 2. Electrical Characteristics

V_{DD} = 12 V, V_{SS} = GND, T_A = –40 to +125 °C; typical specs at 25 °C.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DC Specifications						
Power supply voltage	V_{DD}	$(V_{DD} - V_{EE})$	8	—	24	V
Input current (ON)	$I_{F(ON)}$		5	—	10	mA
Input voltage (OFF)	$V_{F(OFF)}$	Measured at ANODE with respect to CATHODE.	–0.6	—	1.6	V
Input forward voltage	V_F	Measured at ANODE with respect to CATHODE. I_F = 5 mA.	1.7	—	2.8	V
Output resistance high	RoH		—	2.7	—	Ω
Output resistance low	RoL		—	1.0	—	
Output high current	I_{OH}	I_F = 0, Figure A2	—	1.5	—	A
Output low current	I_{OL}	I_F = 10 mA, Figure A1	—	2.5	—	A
High-level output voltage	V_{OH}	I_{OUT} = –100 mA	—	$V_{DD} - 0.3$	—	V
Low-level output voltage	V_{OL}	V_{SS} = GND	—	0.1	—	V
High level supply current		Output open I_F = 10 mA	—	5	—	mA
Low level supply current		Output open V_F = –0.6 to +1.6 V	—	5	—	mA
Input reverse breakdown voltage	BV_R	I_R = 10 µA. Measured at ANODE with respect to CATHODE.	–0.5	—	–0.8	V
Input capacitance	C_{IN}		—	20	—	pF

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Table 2. Electrical Characteristics (Continued)

V_{DD} = 12 V, V_{SS} = GND, T_A = –40 to +125 °C; typical specs at 25 °C.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Undervoltage threshold – V_{DD}	V_{DDUV+}	V_{DD} rising	8	9	10	V
Undervoltage threshold hysteresis – V_{DD}	V_{DDHYS}	V_{DD} falling	—	500	—	mV
AC Specifications						
Propagation delay time to high output level	t_{PLH}	CL = 2000 pF	—	—	50	ns
Propagation delay time to low output level	t_{PHL}	CL = 2000 pF	—	—	50	ns
UVLO turn-on delay	$t_{UVLO\ ON}$		—	—	50	ns
UVLO turn-off delay	$t_{UVLO\ OFF}$		—	—	50	
Output rise and fall time	t_R, t_F	CL = 200 pF	—	—	20	ns
Device start-up time	t_{START}	Time from V_{DD} = V_{DD_UV+} to V_O	—	—	2	µs

Si8220

2. Test Circuits

Figure 1. IOL Test Circuit

Figure 2. IOH Test Circuit
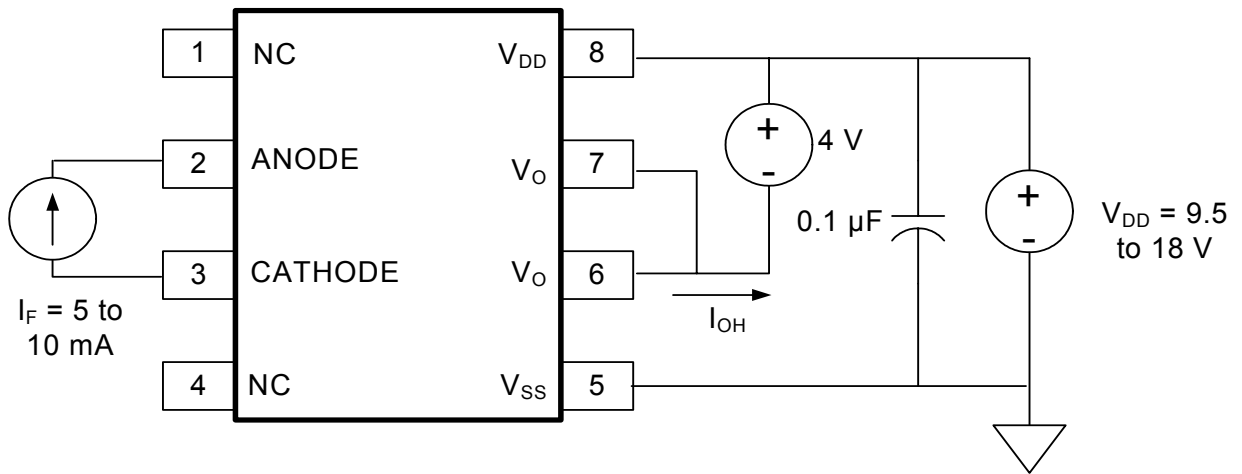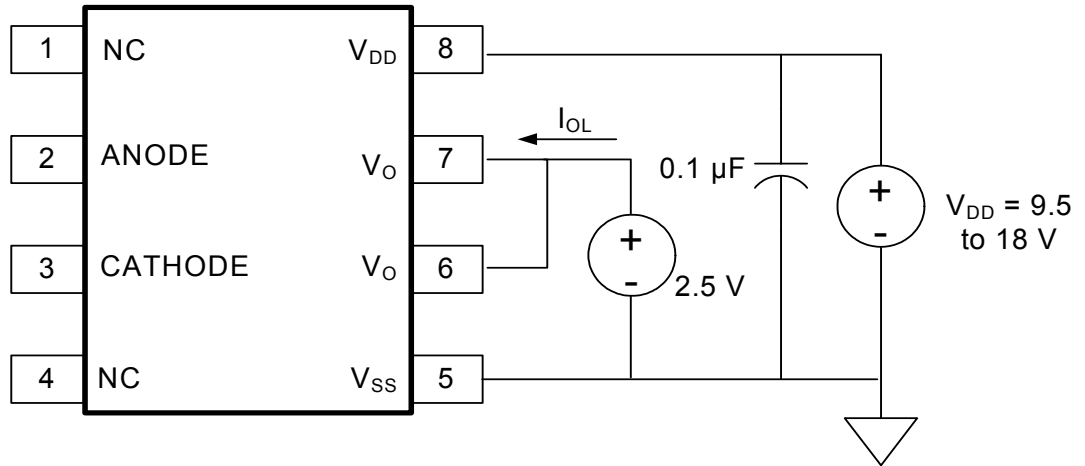
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3. Overview

The Si8220 is a pin-compatible upgrade for popular opto-isolated drivers, such as the HP/Agilent/Avago HCPL-3120, Toshiba TLP250, and others. These products utilize Silicon Laboratories' proprietary silicon isolator technology, enabling fast propagation time while withstanding 600 VDC (2.5 kV$_{RMS}$) from the input to output. The operation of this isolator is analogous to that of an opto-coupler, except that an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. As shown in Figure 3, an isolation channel consists of an RF transmitter and receiver separated by an RF transformer.
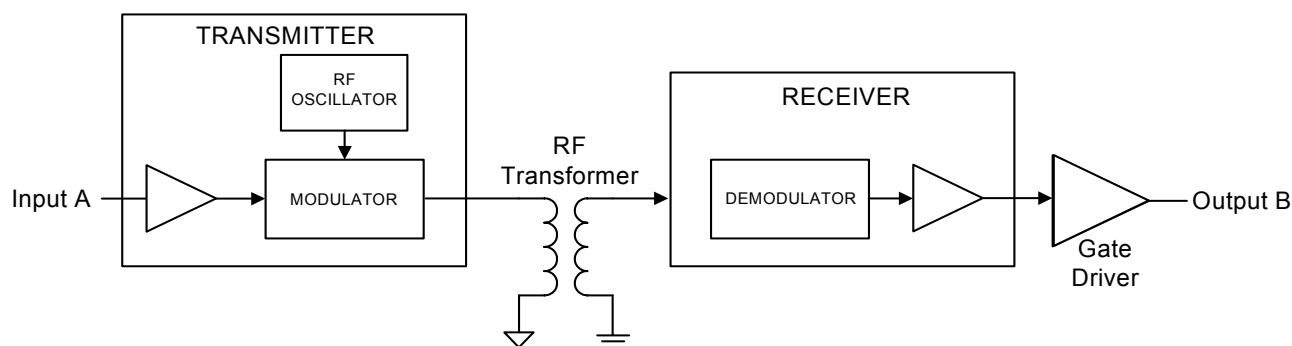
Figure 3. Isolator Operation

Input "A" turns the RF carrier on when high and off when low. The carrier is transmitted through the RF transformer to the output side demodulator, which consists of a receiver tuned to the carrier frequency. The demodulator asserts output "B" when sufficient in-band energy is detected. The driver output state follows that of output B.

4. Technical Description

4.1. Device Behavior

Truth tables for the Si8220 are summarized in Table 3.

Table 3. Si8220 Truth Table Summary

Cathode	Anode	Diode Current (I_F)	V_{DD}	VO	Comments
X	X	X	< UVLO	Hi-Z	Device turned off
Hi-Z	X	0	> UVLO	L	Logic low state
X	Hi-Z	0	> UVLO	L	Logic low state
GND	GND	0	> UVLO	L	Logic low state
VF	VF	0	> UVLO	L	Logic low state
GND1	VF	< $I_{F(ON)}$	> UVLO	L	Logic low state
GND1	VF	≥ $I_{F(ON)}$	> UVLO	H	Logic high state
Note: "X" = don't care.					

4.2. Device Startup

Output V_O is held low during power-up until V_{DD} rises above the UVLO threshold for a minimum time period of t_{START}. Following this, the output is high when the current flowing from anode to cathode is > $I_{F(ON)}$. Device startup, normal operation, and shutdown behavior is shown in Figure 4.
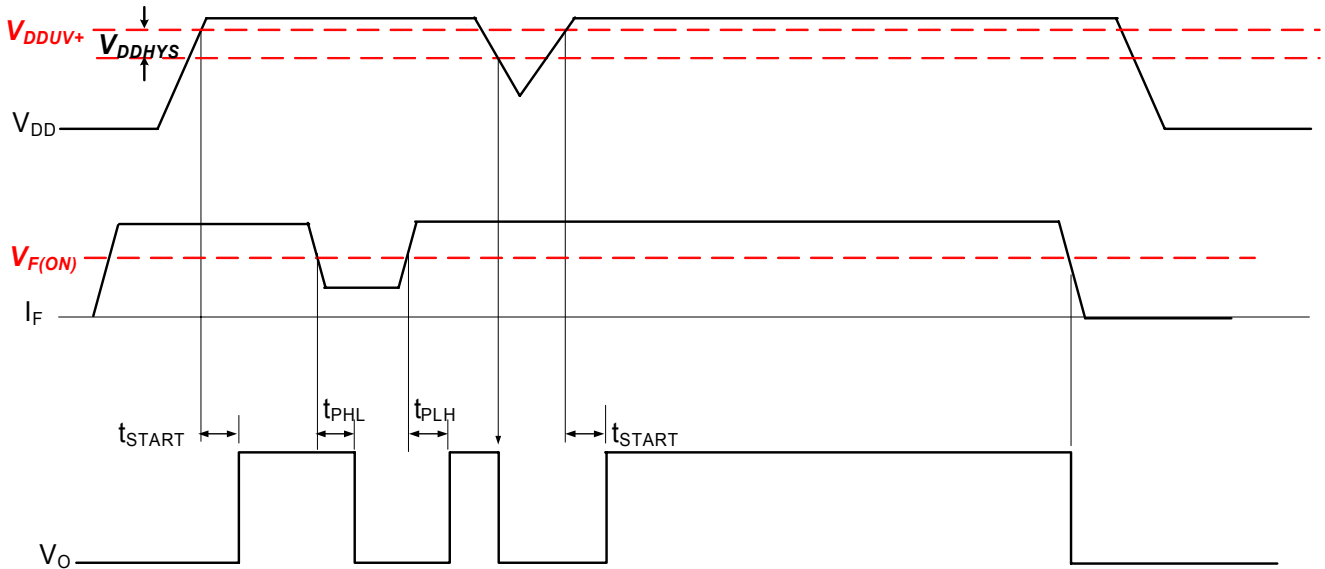

Figure 4. Si8220 Operating Behavior ($I_F ≥ I_{F(MIN)}$ when $V_F ≥ V_{F(MIN)}$)

4.3. Under Voltage Lockout (UVLO)

The UVLO circuit unconditionally drives V_O low when V_{DD} is below the lockout threshold. Referring to Figure 5, upon power up, the Si8220 is maintained in UVLO until V_{DD} rises above V_{DDUV+}. During power down, the Si8220 enters UVLO when V_{DD} falls below the UVLO threshold plus hysteresis (i.e., $V_{DD} \leq V_{DDUV+} - V_{DDHYST}$).
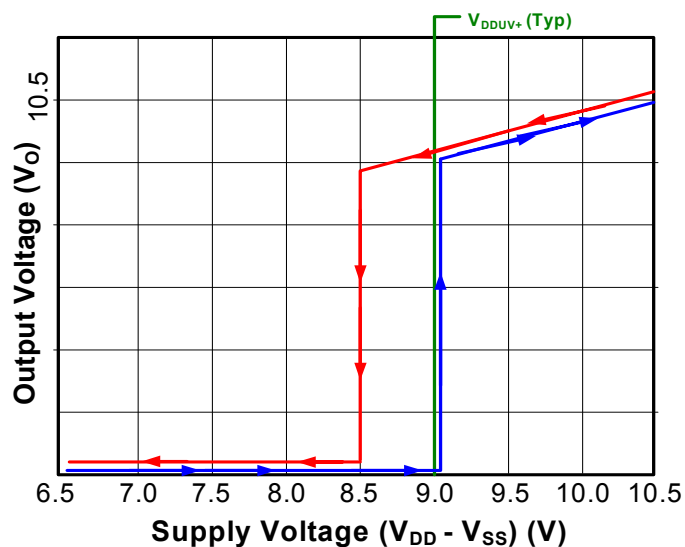

Figure 5. Si8220 UVLO Response

5. Applications

5.1. Power Supply Connections

V_{SS} can be biased at, above, or below ground as long as the voltage on V_{DD} with respect to V_{SS} is a maximum of 24 V. V_{DD} decoupling capacitors should be placed as close to the package pins as possible. The optimum values for these capacitors depend on load current and the distance between the chip and its power source. A minimum 1 µF capacitor is recommended.

5.2. Layout Considerations

It is most important to minimize ringing in the drive path and noise on the V_{DD} lines. Care must be taken to minimize parasitic inductance in these paths by locating the Si8220 as close to the device it is driving as possible. In addition, the V_{DD} supply and ground trace paths must be kept short. For this reason, the use of power and ground planes is highly recommended. A split ground plane system having separate ground and V_{DD} planes for power devices and small signal components provides the best overall noise performance.

5.3. Power Dissipation Considerations

Proper system design must assure that the Si8220 operates within safe thermal limits across the entire load range. The Si8220 total power dissipation is the sum of the power dissipated by bias supply current, internal switching losses, and power delivered to the load, as shown in Equation 1.

$$P_D = (V_F)(I_F) + (V_{DD})(I_{QOUT}) + (C_{int})(V_{DD}^2)(F) + 2(C_L)(V_{DD}^2)(F)$$

where:

P_D is the total Si8220 device power dissipation (W)

I_F is the diode current (10 mA max)

V_F is the diode anode voltage (2.8 V max)

I_{QOUT} is the driver maximum bias curent (5 mA)

C_{int} is the internal parasitic capacitance (370 pF)

V_{DD} is the driver-side supply voltage (24 V max)

F is the switching frequency (Hz)

Equation 1.

The maximum allowable power dissipation for the Si8220 is a function of the package thermal resistance, ambient temperature, and maximum allowable junction temperature, as shown in Equation 2.

$$P_{D(MAX)} \leq \frac{T_{jmax} - T_A}{\theta_{ja}}$$

where:

$P_{D(MAX)}$ is the maximum allowable Si8220 device power dissipation (W)

T_{jmax} is the Si8220 maximum junction temperature (145 °C)

T_A is the ambient temperature (°C)

θ_{ja} is the Si8220 package junction-to-air thermal resistance (125 °C/W)

Equation 2.

Substituting values for $P_{D(MAX)}$, T_{jmax}, T_A, and θ_{ja} into Equation 2 results in a maximum allowable total power dissipation of 0.95 W. The maximum allowable load is found by substituting this limit and the appropriate datasheet values from Table 2 on page 4 into Equation 1 and simplifying. The result is Equation 3, where V_F = 2.8 V, I_F = 10 mA, and V_{DD} = 18 V.

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$$C_{L(max)} = \frac{1.35 \times 10^{-3}}{F} - 1.85 \times 10^{-10}$$

where:

$C_{L(max)}$ is the maximum load (pF) allowable at switching frequency F

Equation 3.

A graph of Equation 3 is shown in Figure 6. Each point along the load line in this graph represents the package dissipation-limited value of C_L for the corresponding switching frequency.
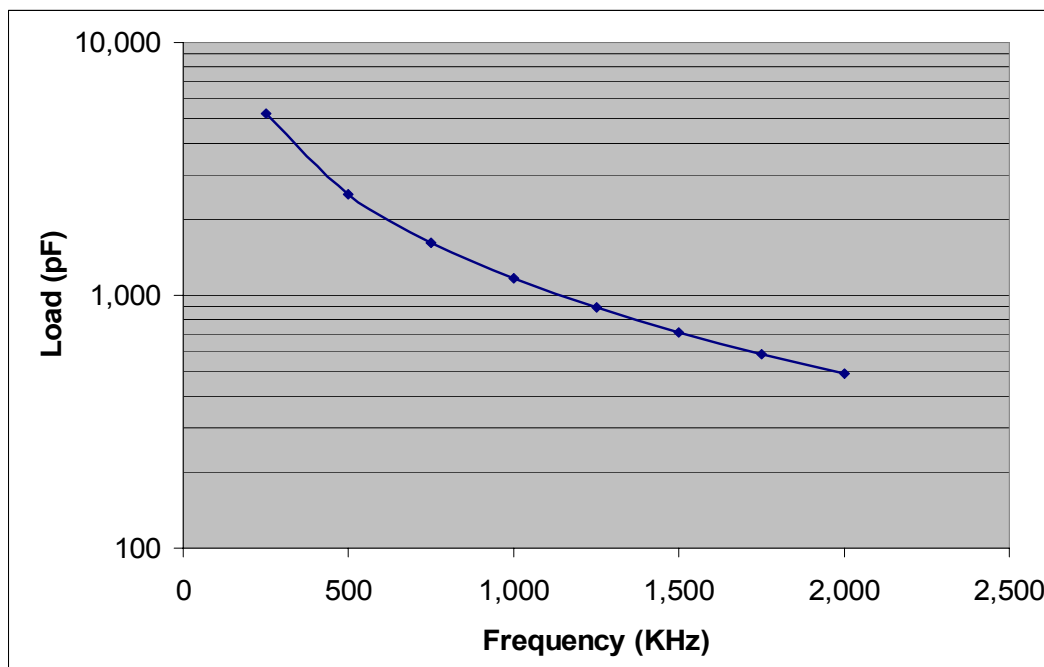

Figure 6. Maximum Load vs. Switching Frequency

5.4. Input Circuit Design

Opto driver manufacturers typically recommend the circuits shown in Figures 7 and 8. These circuits are specifically designed to improve opto-coupler input common-mode rejection and increase noise immunity.
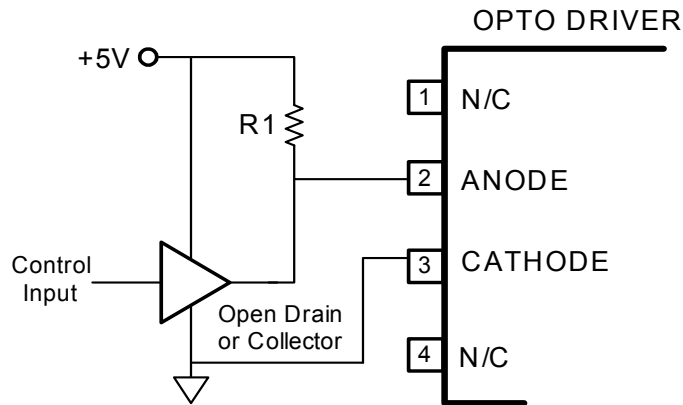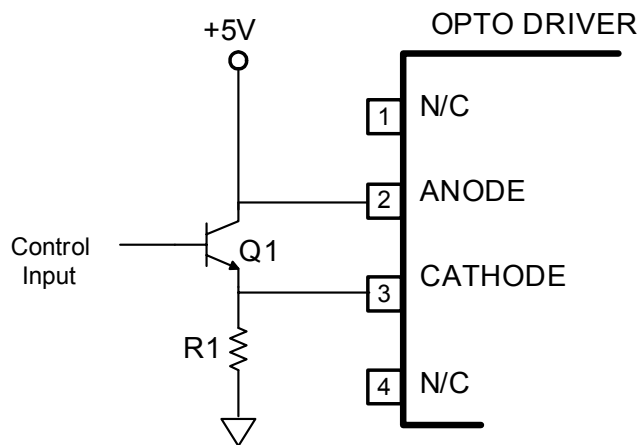
Figure 7. Opto Driver Input Circuit

Figure 8. High CMR Opto Driver Input Circuit

The optically-coupled driver circuit of Figure 7 turns the LED on when the control input is high. However, internal capacitive coupling from the LED to the power and ground conductors can momentarily force the LED into its off state when the anode and cathode inputs are subjected to a high common-mode transient. The circuit shown in Figure 8 addresses this issue by using a value of R1 sufficiently low to overdrive the LED, ensuring it remains on during an input common-mode transient. Q1 shorts the LED off in the low output state, again increasing common-mode transient immunity. Some opto driver applications also recommend reverse-biasing the LED when the control input is off to prevent coupled noise from energizing the LED.

The Si8220 can be used with the input circuits shown in Figures 7 and 8; however, some applications will require increasing the value of R1 in order to limit I_F to a maximum of 10 mA. The Si8220 propagation delay and output drive do not change for values of I_F between $I_{F(MIN)}$ and $I_{F(MAX)}$. New designs should consider the input circuit configurations of Figure 9, which are more efficient than those of Figures 7 and 8. As shown, S1 represents any suitable switch, such as a BJT or MOSFET, analog transmission gate, processor I/O, etc. Also, note that the Si8220 input can be driven from the I/O port of any MCU or FPGA capable of sourcing a minimum of 5 mA (see Figure 9C).
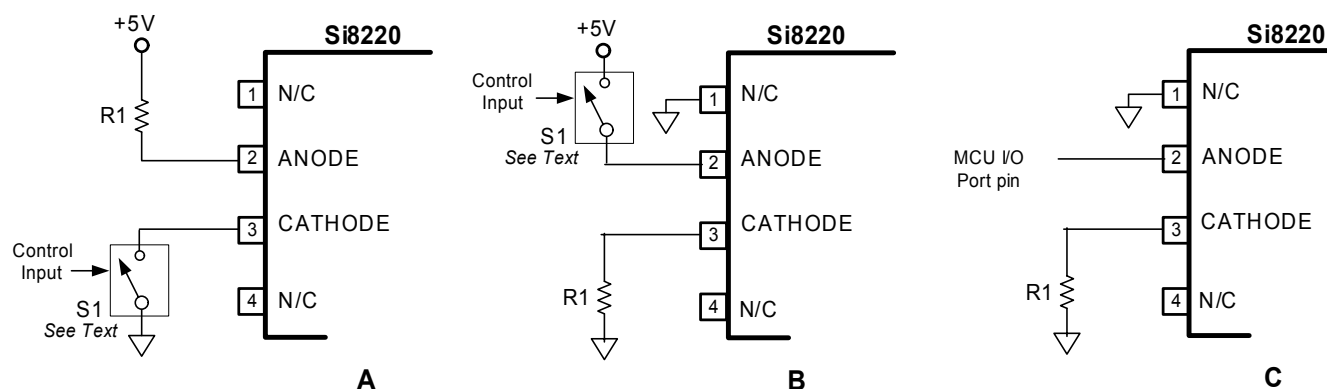
Figure 9. Si8220 Other Input Circuit Configurations

5.5. Parametric Differences between Si8220 and HCPL-3120 Opto Driver

The Si8220 is designed to directly replace HCPL-3120 and similar opto drivers. Parametric differences are summarized in Table 4 below.

Table 4. Parametric Differences of Si8220 vs. HCPL-3120

Parameter	Si8220	HCPL-3120	Units
Max supply voltage	24	30	V
ON state forward input current	5 to 10	7 to 16	mA
OFF state input voltage	–0.6 to +1.6	–0.3 to +0.8	V
Max reverse input voltage ($I_R = -10$ µA)	–0.5 to –0.8	–5	V
UVLO threshold (rising)	8.0 to 10.0	13.5 to 11.0	V
UVLO threshold (falling)	9.3 to 7.3	12.0 to 9.7	V
UVLO hysteresis	0.5	1.6	V
Rise/fall time into 10 Ω in series with 10 nF	TBD	100	ns

5.5.1. Supply Voltage and UVLO

The supply voltage of the Si8220 is limited to 24 V, and the UVLO voltage thresholds are scaled accordingly. This will not be an issue for opto replacement applications operating with supply voltages of 24 V and below.

5.5.2. Input Diode Differences

The Si8220 input circuit requires less current and has twice the off-state noise margin compared to opto drivers. However, high CMR opto driver designs that overdrive the LED (see Figure 8) may require increasing the value of R1 to limit input current to 10 mA max. In addition, there is no benefit in driving the Si8220 input diode into reverse bias when in the off state. Consequently, opto driver circuits using this technique should either leave the negative bias circuitry unpopulated or modify the circuitry (e.g. add a clamp diode) to ensure that the anode pin of the Si8220 is no more than -0.8 V with respect to the cathode when reverse-biased.

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6. Regulatory Information

Table 5. Regulatory Information

UL
The Si8220 is certified under the UL1577 component recognition program to provide basic insulation to 2500 V_{RMS} (1 minute). It is production tested at $\geq$ 3000 V_{RMS} for 1 second. For more details, see File TBD.

Table 6. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value	Unit
Minimum Air Gap (Clearance)	L(IO1)		7.1	mm
Minimum External Tracking (Creepage)	L(IO2)		7.4	mm
Minimum Internal Gap (Internal Clearance)			TBD	mm
Resistance (Input-Output)[1]	R_{IO}		10^{12}	Ω
Capacitance (Input-Output)[1]	C_{IO}	f = 1 MHz	TBD	pF
Input Capacitance[2]	C_I		TBD	pF

Notes:
1. To determine resistance and capacitance, the Si8220 is converted into a 2-terminal device. Pins 1–4 are shorted together to form the first terminal, and pins 5–8 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

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7. Pin Descriptions: Si8220
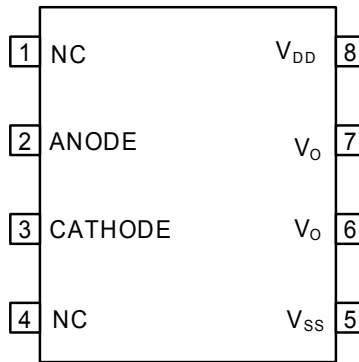
Figure 10. Pin Configuration

Table 7. Pin Descriptions

Pin	Name	Description
1	NC	No connect.
2	ANODE	Anode of LED emulator. V_O follows the signal applied to this input with respect to the CATHODE input.
3	CATHODE	Cathode of LED emulator. V_O follows the signal applied to ANODE with respect to this input.
4	NC	No connect.
5	V_{SS}	External MOSFET source connection and ground reference for V_{DD}. This terminal is typically connected to ground but may be tied to a negative or positive voltage.
6	V_O	Output signal. Pins 6 and 7 are connected together internally.
7	V_O	Output signal. Pins 6 and 7 are connected together internally.
8	V_{DD}	Output-side power supply input referenced to V_{SS} (24 V max).

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8. Ordering Guide

Part Number	Package	Temp Range
Si8220-B-IP	DIP-8	–40 to +125 °C

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9. Package Outline: 8-Pin PDIP
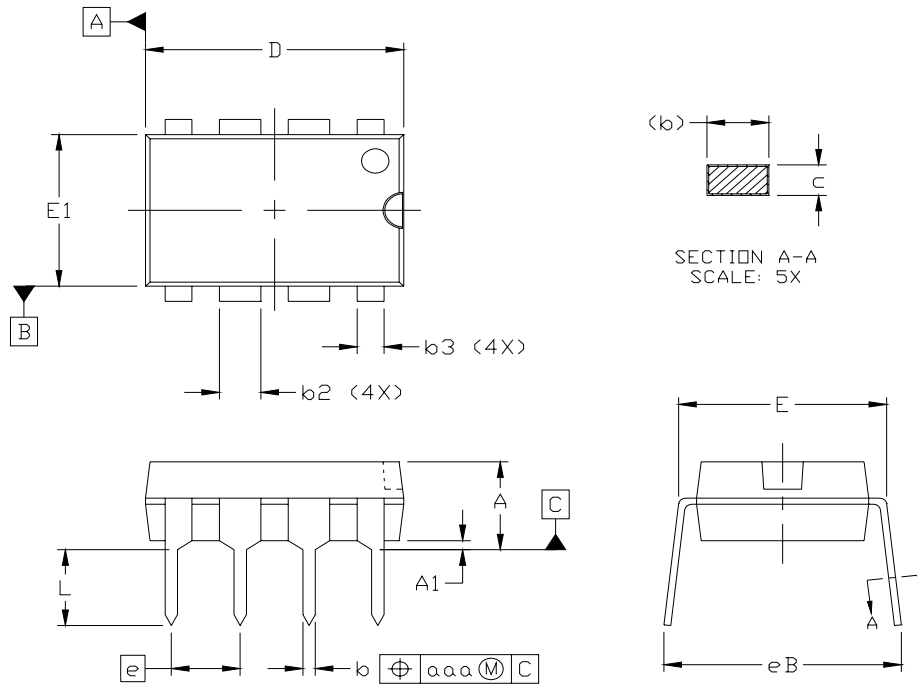
Figure 11. 8-Pin PDIP

Table 8. Package Dimensions

Dimension	MIN	NOM	MAX
A	—	—	.210
A1	.015	—	—
b	.014	.018	.022
b2	.045	.060	.070
b3	.030	.039	.045
c	.008	.010	.014
D	.355	.365	.400
E	.300	.310	.325
E1	.240	.250	.280
e	.100 BSC.		
eB	—	—	.430
L	.115	.130	.150
aaa	—	—	.010

Notes:
1. All dimensions shown are in inches unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MS-001, Variation BA.

NOTES:

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Si8220

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