

### DESCRIPTION

The HY531000A is the 2nd generation and fast dynamic RAM organized 1,048,576 x 1-bit. The HY531000A utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY531000A to be packaged in a standard 300mil 18 pin PDIP 20/26 pin SOJ.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 5V± 10% tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

### FEATURES

- Low power dissipation  
**Max. battery back-up 2.2mW (L-part)**  
**Max. CMOS standby 1.1mW (L-part)**  
**5.5mW**  
**Max. TTL standby 11.0mW**  
**Max. operating**

Speed	Power
60	467.5mW
70	412.5mW
80	357.5mW

- Single power supply of 5V± 10%
- TTL compatible inputs and outputs
- Fast access Time

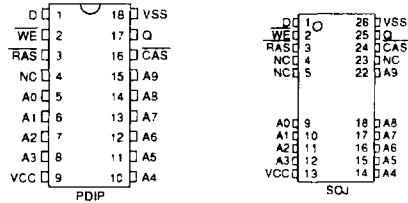
Speed	tRAC	tCAC	tPC
60	60ns	15ns	40ns
70	70ns	20ns	40ns
80	80ns	20ns	45ns

- Fast page mode operation
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden refresh
- 512 refresh cycles / 64ms (L-part)  
 512 refresh cycles / 8ms

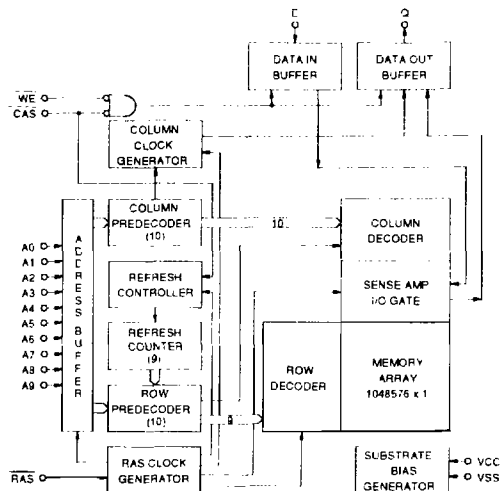
### PIN DESCRIPTION

RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
A0-A9	Address Input
D	Data Input
Q	Data Output
Vcc	Power (+ 5V)
VSS	Ground

### PIN CONNECTION



### BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to VSS	-1.0 to 7.0	V
VCC	Voltage on VCC Relative to VSS	-1.0 to 7.0	V
IOS	Short Circuit Output Current	50	mA
Pd	Power Dissipation	0.90	W
TSOLDER	Soldering Temperature•Time	260•10	°C•sec

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

**RECOMMENDED DC OPERATING CONDITIONS**

(TA=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	VCC+1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to VSS.

**DC CHARACTERISTICS**

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pins)	VSS ≤ VIN ≤ VCC All other pins not under test= VSS		-10	10	μA	
ILO	Output Leakage Current (High Impedance State)	VSS ≤ VOUT ≤ VCC RAS & CAS at VIH		-10	10	μA	
ICC1	VCC Supply Current, Operating	tRC= tRC (min.)	60 70 80	- - -	85 75 65	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ VSS		-	2	mA	
ICC3	VCC Supply Current, RAS-only refresh	tRC= tRC (min.)	60 70 80	- - -	85 75 65	mA	1,3
ICC4	VCC Supply Current, Fast Page mode	tPC= tPC (min.)	60 70 80	- - -	70 55 45	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC-0.2V	L-part	- -	1 0.2	mA	5
ICC6	VCC Supply Current, CAS-before-RAS refresh	tRC= tRC (min.)	60 70 80	- - -	85 75 65	mA	1,3
ICC7	VCC Supply Current, Battery Back Up (L-part only)	tRC= 125μs, CAS= CBR cycling or 0.2V WE= VCC-0.2V A0-A9= VCC-0.2V or 0.2V D= VCC-0.2V, 0.2V or open Q= open	tRAS ≤ 300ns  tRAS ≤ 1μs	- - -	300  400	μA	1,4,5
VOL	Output Low Voltage	IOL= 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH= -5mA		2.4	-	V	

**NOTE :**

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rate.
2. ICC1 and ICC4 depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while RAS= VIL and CAS= VIH.
4. Only tRAS(max.)= 1μs is applied to refresh of battery backup but tRAS(max.)= 10μs is applied to normal functional operation.
5. ICC5(max.)= 0.2mA and ICC7 are applied to L-part only(HY531000ALS and HY531000ALJ).

**AC CHARACTERISTICS**

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS= 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HY531000AS/AJ/ALS/ALJ						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	130	-	155	-	175	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	40	-	45	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	60	-	65	-	70	-	ns	
5	tRAC	Access Time from RAS	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from CAS	-	15	-	20	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	35	-	35	-	40	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	60	100K	70	100K	70	100K	ns	
15	tRSH	RAS Hold Time	15	-	20	-	20	-	ns	
16	tCSH	CAS Hold Time	60	-	70	-	80	-	ns	
17	tCAS	CAS Pulse Width	15	10K	20	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	20	45	20	50	20	60	ns	9
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	45	-	50	-	55	-	ns	
27	tRAL	Column Address to RAS Lead Time	25	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	15	-	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from RAS	45	-	50	-	55	-	ns	
33	tWP	Write Command Pulse Width	10	-	15	-	15	-	ns	
34	tRWL	Write Command to RAS Lead Time	15	-	20	-	20	-	ns	
35	tCWL	Write Command to CAS Lead Time	15	-	20	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	45	-	50	-	55	-	ns	
39	tREF	Refresh Period (512 cycles)	-	8	-	8	-	8	ms	
		L-part	-	64	-	64	-	64		11
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

**AC CHARACTERISTICS**

(continued)

#	SYMBOL	PARAMETER	HY531000AS/AJ/ALS/ALJ						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCWD	CAS to WE Delay Time	15	-	20	-	20	-	ns	8
42	tRWD	RAS to WE Delay Time	60	-	70	-	80	-	ns	8
43	tAWD	Column Address to WE Delay Time	30	-	35	-	40	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	CAS Hold Time (CBR Cycle)	15	-	15	-	15	-	ns	
46	tRPC	RAS to CAS Precharge Time	0	-	0	-	0	-	ns	
47	tCPT	CAS Precharge Time (CBR Counter Test)	40	-	40	-	40	-	ns	
48	tCPWD	WE Delay Time from CAS Precharge	30	-	35	-	35	-	ns	8
49	tRHCP	RAS Hold Time from CAS Precharge	30	-	35	-	35	-	ns	

**NOTE :**

1. An initial pause of 200 $\mu$ s is required after power-up followed by 8  $\overline{\text{RAS}}$  cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  initialization cycles instead of 8  $\overline{\text{RAS}}$  cycles are required.
2. AC measurements assume  $t_t = 5$ ns.
3.  $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5.  $t_{OFF}(\text{max.})$  defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
7. These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early write cycles and to  $\overline{\text{WE}}$  leading edge in Read-Modify-Write cycles.
8.  $t_{WCS}$ ,  $t_{RWd}$ ,  $t_{CWD}$ ,  $t_{AWd}$  and  $t_{CPWd}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If  $t_{RWd} \geq t_{RWd}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$ ,  $t_{AWd} \geq t_{AWd}(\text{min.})$ , and  $t_{CPWd} \geq t_{CPWd}(\text{min.})$ , the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the  $t_{RCD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
10. Operation within the  $t_{RAD}(\text{max.})$  limit insures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled by  $t_{AA}$ .
11.  $t_{REF}(\text{max.}) = 64$ ms is applied to L-part only (HY531000ALS and HY531000ALJ).

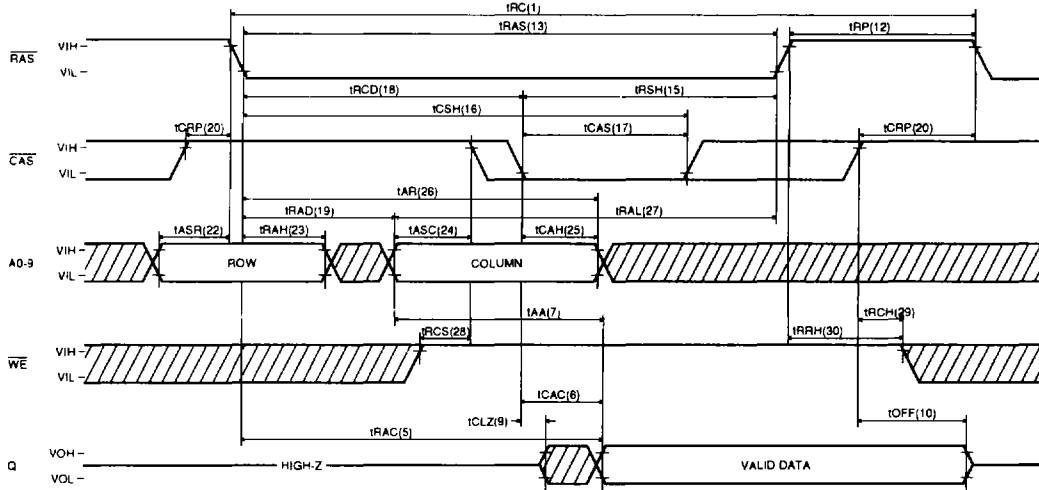
**CAPACITANCE**

( $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ,  $f = 1\text{MHz}$ , unless otherwise noted.)

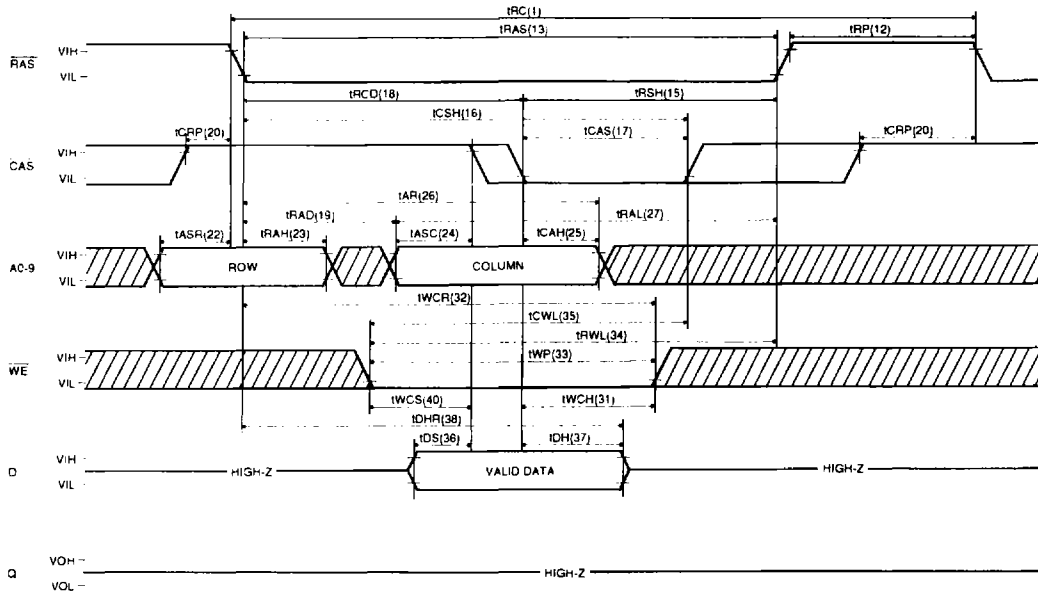
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A9, D)	-	5	pF
CIN2	Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ )	-	7	pF
COU	Output Capacitance (Q)	-	7	pF

TIMING DIAGRAM

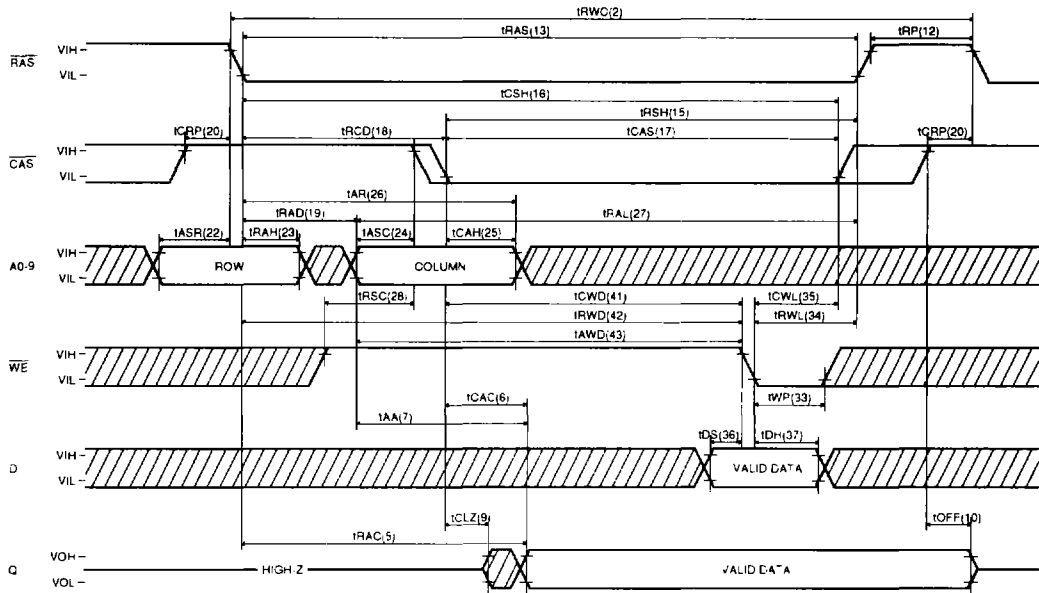
READ CYCLE



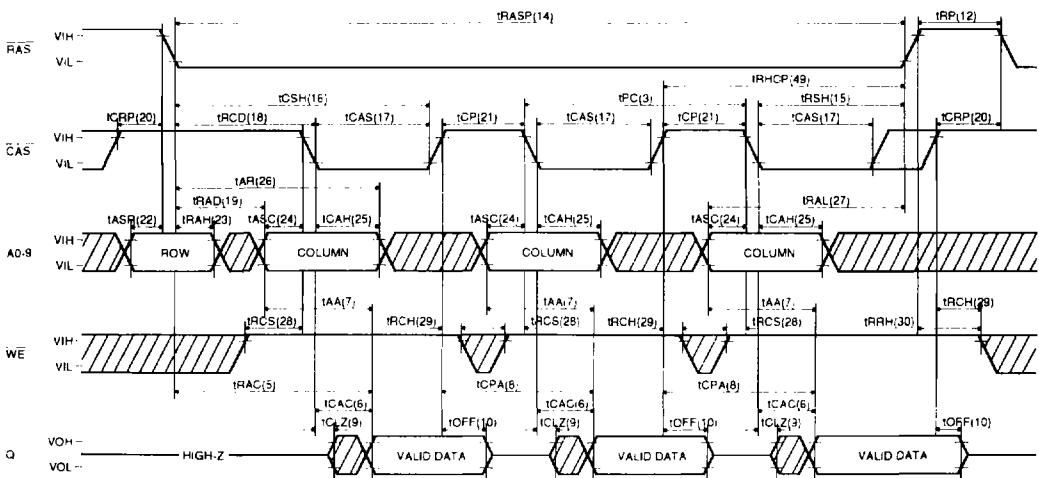
EARLY WRITE CYCLE



**READ-MODIFY-WRITE CYCLE**



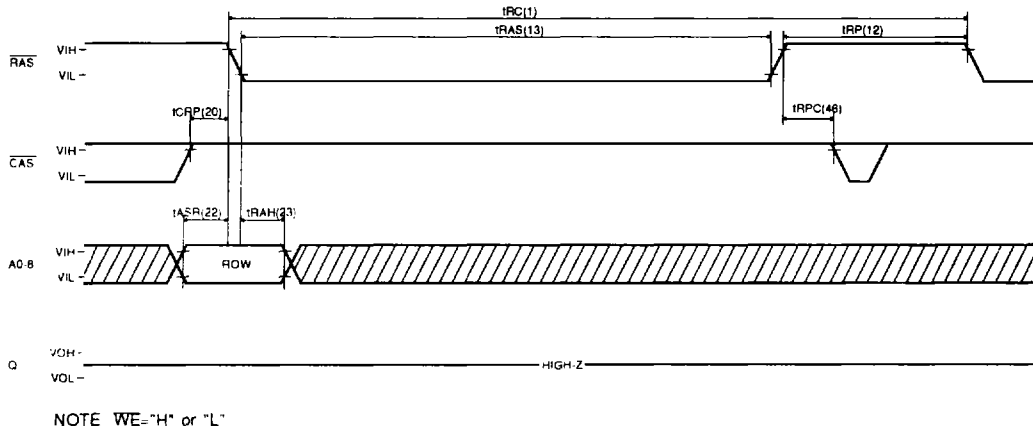
**FAST PAGE MODE READ CYCLE**



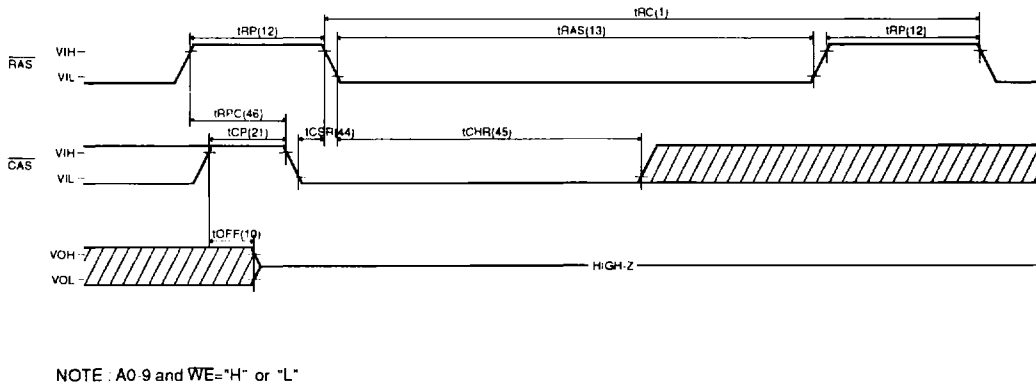




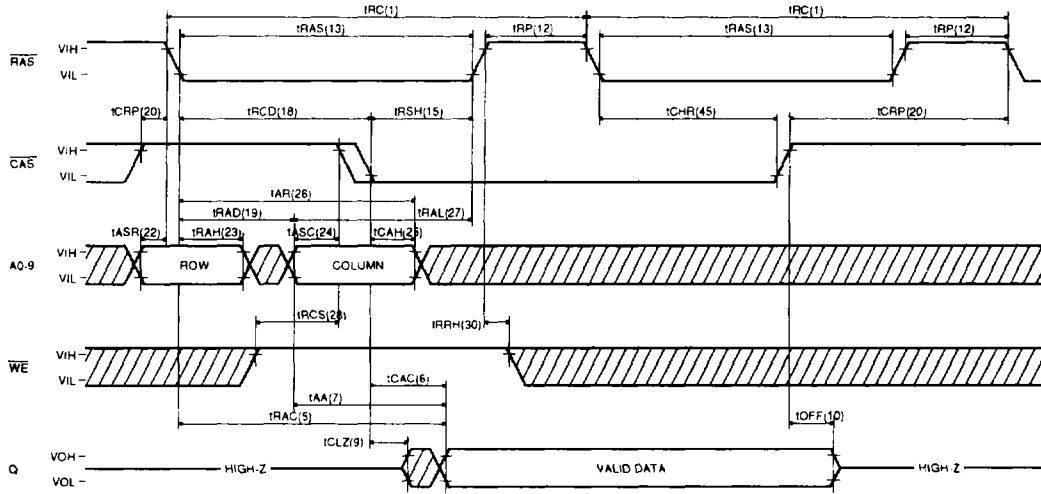
**$\overline{\text{RAS}}$ -ONLY REFRESH CYCLE**



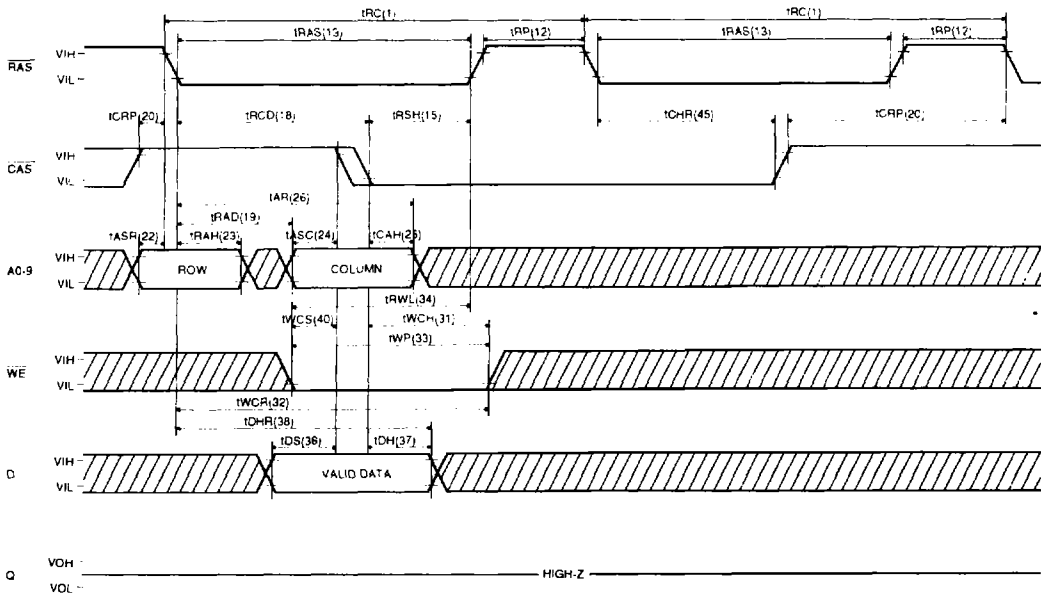
**$\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  REFRESH CYCLE**



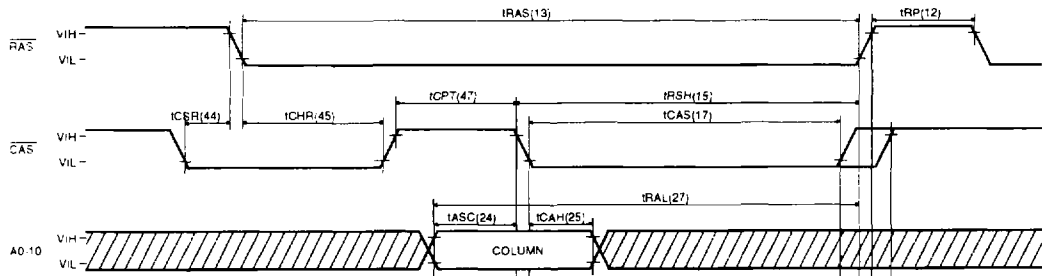
**HIDDEN REFRESH CYCLE (READ)**



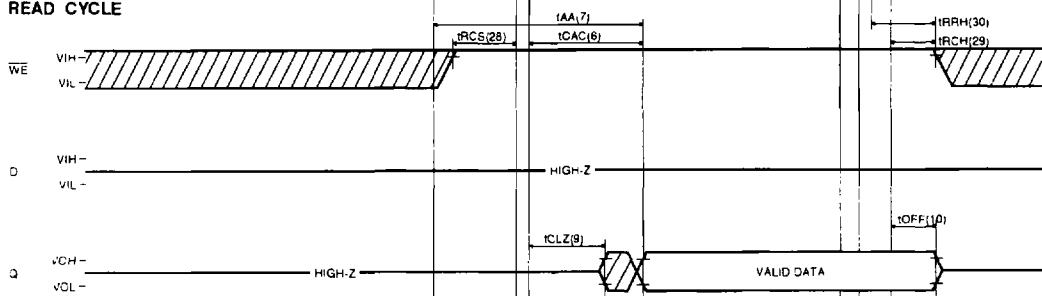
**HIDDEN REFRESH CYCLE (WRITE)**



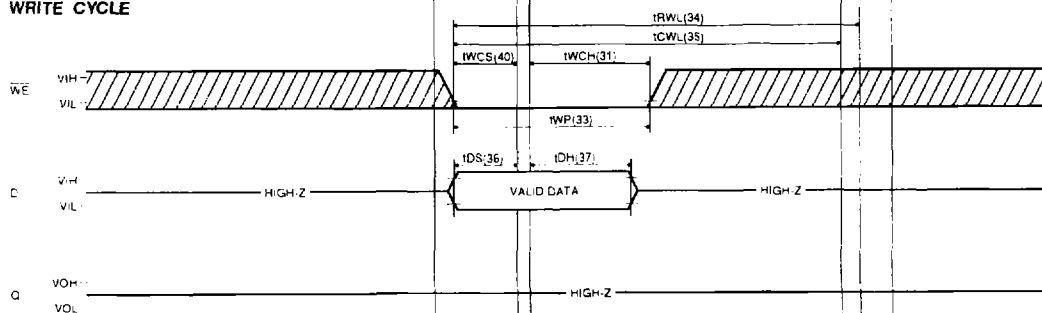
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



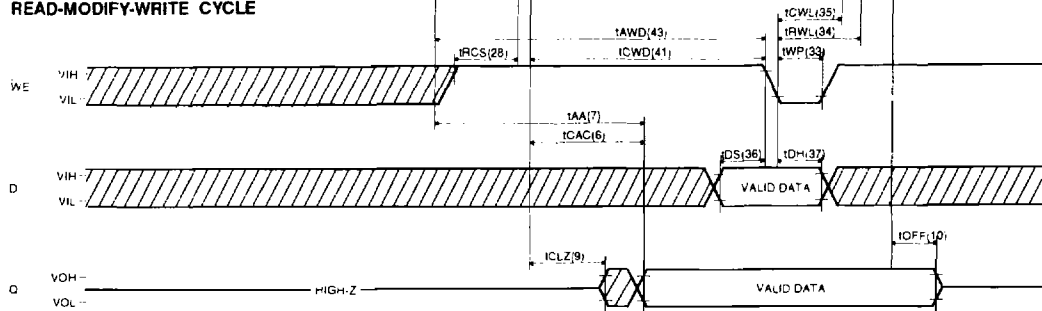
READ CYCLE



WRITE CYCLE

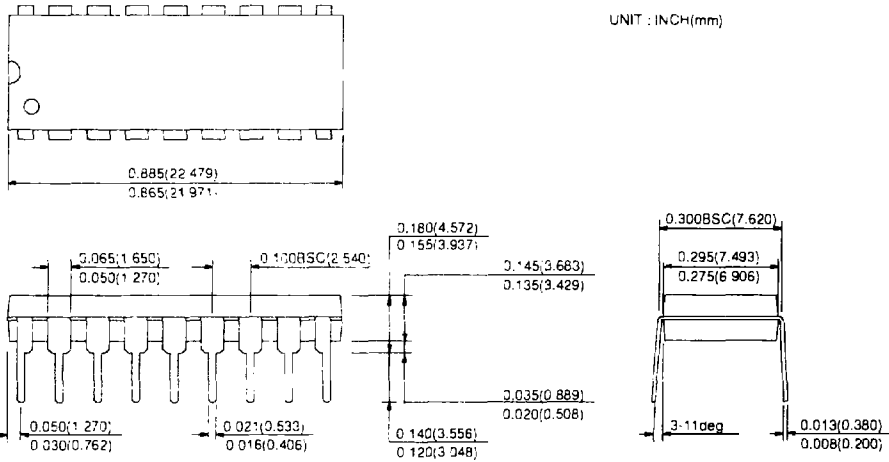


READ-MODIFY-WRITE CYCLE

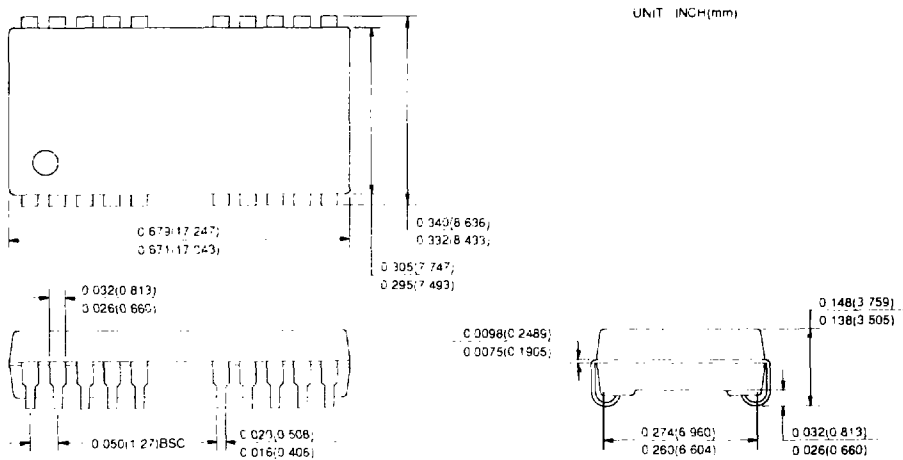


PACKAGE INFORMATION

300 mil 18 pin Plastic Dual In Line Package (S)



300 mil 20/26 pin Small Outline Package (J)



**ORDERING INFORMATION**

<b>PART NUMBER</b>	<b>SPEED</b>	<b>POWER</b>	<b>PACKAGE</b>
HY531000AS	60/70/80		PDIP
HY531000ALS	60/70/80	L-part	PDIP
HY531000AJ	60/70/80		SOJ
HY531000ALJ	60/70/80	L-part	SOJ