3.3V CMOS Buffer Clock Driver

Features

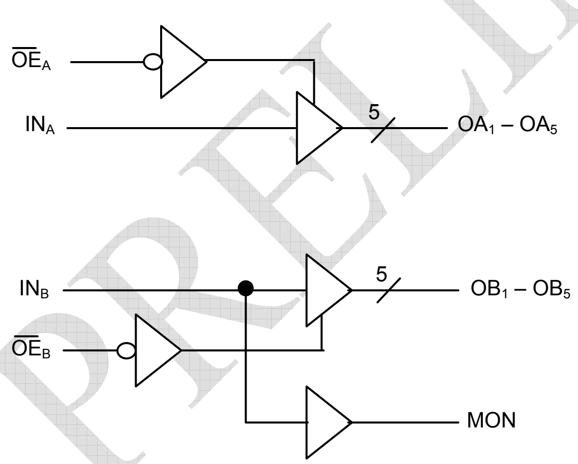
- Advanced CMOS Technology
- Guaranteed low skew < 500pS (max.)
- Very low duty cycle distortion < 1.0nS (max)
- Very low CMOS power levels
- TTL compatible inputs and outputs
- Inputs can be driven from 3.3V or 5V components
- Two independent output banks with 3-state control
- 1:5 fanout per bank
- "Heartbeat" monitor output
- V_{CC} = 3.3V ± 0.3V
- Available in SSOP, SOIC and QSOP Packages

Functional Description

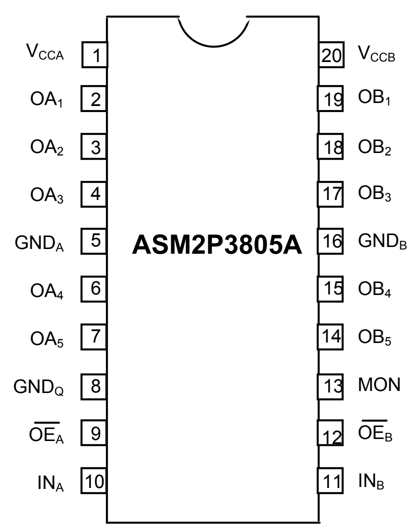
The ASM2P3805A is a 3.3V, non-inverting clock driver built using advanced CMOS technology. The device consists of two banks of drivers, each with a 1:5 fanout and its own output enable control. The device has a "heartbeat" monitor for diagnostics and PLL driving. The MON output is identical to all other outputs and complies with the output specifications in this document. The ASM2P3805A offers low capacitance inputs.

The ASM2P3805A is designed for high speed clock distribution where signal quality and skew are critical. The ASM2P3805A also allows single point-to-point transmission line driving in applications such as address distribution, where one signal must be distributed to multiple receivers with low skew and high signal quality.

Block Diagram



Pin Diagram



Pin Description

Pin #	Pin Names	Description
9,12	$\overline{OE}_A$, $\overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
10,11	IN_A, IN_B	Clock Inputs
2,3,4,6,7	OA_1-OA_5	Clock Outputs
19,18,17,15,14	OB_1-OB_5	Clock Outputs
1	V_{CCA}	Power supply for Bank A
20	V_{CCB}	Power supply for Bank B
5	GND_A	Ground for Bank A
16	GND_B	Ground for Bank B
8	GND_Q	Ground
13	MON	Monitor Output

Function Table

Inputs		Outputs	
$\overline{OE}_A$, $\overline{OE}_B$	**IN_A, IN_B**	**OA_n, OB_n**	**MON**
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H
Note: H = HIGH; L = LOW; Z = High-Impedance			

Capacitance (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN}= 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8	pF
Note: 1 This parameter is measured at characterization but not tested.					

Absolute Maximum Ratings[1]

Symbol	Description	Max	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	-0.5 to +7	V
V_{TERM}[4]	Terminal Voltage with Respect to GND	-0.5 to V_{CC}+0.5	V
I_{OUT}	DC Output Current	-60 to +60	mA
T_{STG}	Storage Temperature	-65 to +150	° C
T_J	Junction Temperature	150	° C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: 1 These are stress ratings only and are not implied for functional use. Exposure to absolute maximum ratings for prolonged periods of time may affect device reliability.

2. V_{CC} terminals.
3. Input terminals.
4. Outputs and I/O terminals.

DC Electrical Characteristics over Operating Range

Following Conditions Apply Unless Otherwise Specified
Commercial: T_A = 0°C to +70°C, V_{CC} = 3.3V ± 0.3V; Industrial: T_A = -40 0°C to +85°C, V_{CC} = 3.3V ± 0.3V

Symbol	Parameter	Test Conditions[1]		Min	Typ[2]	Max	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2	-	5.5	V
	Input HIGH Level (I/O pins)			2	-	V_{CC}+ 0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	-	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC}= Max.	V_I = 5.5V	-	-	±1	µA
	Input HIGH Current (I/O pins)		V_I = V_{CC}	-	-	±1	
I_{IL}	Input LOW Current (Input pins)	V_{CC}= Max.	V_I = GND	-	-	±1	
	Input LOW Current (I/O pins)		V_I = GND	-	-	±1	
I_{OZH}	High Impedance Output Current (3-State Output Pins)	V_{CC}= Max.	V_O = V_{CC}	-	-	±1	µA
I_{OZL}			V_O = GND	-	-	±1	
V_{IK}	Clamp Diode Voltage	V_{CC}= Min., I_{IN} = -18mA		-	-0.7	-1.2	V
I_{ODH}	Output HIGH Current	V_{CC}= 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		-36	-60	-110	mA
I_{ODL}	Output LOW Current	V_{CC}= 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC}= Min. V_{IN} = V_{IH} or V_{IL}	I_{OH}= -0.1mA	V_{CC}–0.2	-	-	V
			I_{OH}= -8mA	2.4[5]	3	-	
V_{OL}	Output LOW Voltage	V_{CC}= Min. V_{IN} = V_{IH} or V_{IL}	I_{OL}= 0.1mA	-	-	0.2	V
			I_{OL}= 16mA	-	0.2	0.4	
			I_{OL}= 24mA	-	0.3	0.5	
I_{OFF}	Input Power Off Leakage	V_{CC}= 0V, V_{IN} = 4.5V		-	-	±1	µA
I_{OS}	Short Circuit Current[4]	V_{CC}= Max., V_O = GND[3]		-60	-135	-240	mA
V_H	Input Hysteresis	-		-	150	-	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC}= Max. V_{IN} = GND or V_{CC}		-	0.1	10	µA

Notes:1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} - 0.6V at rated current.

Power Supply Characteristics

Symbol	Parameter	Test Conditions[1]		Min	Typ[2]	Max	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC}= Max. V_{IN} = V_{CC} –0.6V[3]		-	10	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	VCC= Max. Outputs Open $\overline{OE}_A$ = $\overline{OE}_B$= GND Per Output Toggling 50% Duty Cycle	V_{IN}= V_{CC} V_{IN}= GND	-	0.035	0.06	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC}= Max. Outputs Open f_O= 25MHz 50% Duty Cycle $\overline{OE}_A$ = $\overline{OE}_B$= V_{CC} Mon. Output Toggling	V_{IN}= V_{CC} V_{IN}= GND	-	0.9	1.6	mA
			V_{IN}= V_{CC}-0.6V V_{IN}= GND	-	0.9	1.6	
		V_{CC}= Max. Outputs Open f_O= 50MHz 50% Duty Cycle OE_A = OE_B= GND Eleven Outputs Toggling	V_{IN}= V_{CC} V_{IN}= GND	-	20	33[5]	
			V_{IN}= V_{CC}-0.6V V_{IN}= GND	-	20	33[5]	

Notes:

1. For conditions shown as Max or Min, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input (V_{IN} = V_{CC} -0.6V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT + IINPUTS + IDYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_O N_O)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = V_{CC} -0.6V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_O = Output Frequency
   N_O = Number of Outputs at f_O
   All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics Over Operating Range – Commercial[3,4]

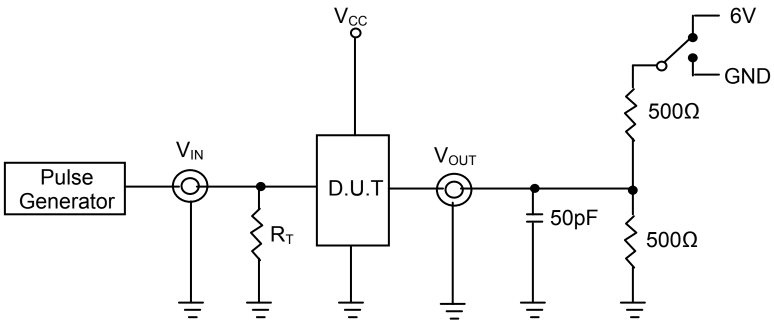
Symbol	Parameter	Conditions[1]	ASM2P3805A		Unit
			Min[2]	Max	
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_n, IN_B to OB_n	C_L= 50pF R_L= 500Ω	1.5	5	nS
t_R	Output Rise Time (0.8V to 2.0V)		-	2	nS
t_F	Output Fall Time (2.0V to 0.8V)		-	2	nS
$t_{SK(O)}$	Output skew: skew between outputs of all banks of same package (inputs tied together)		-	0.5	nS
$t_{SK(P)}$	Pulse skew: skew between opposite transitions of same output ($\|t_{PHL} - t_{PLH}\|$)		-	1	nS
$t_{SK(T)}$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		-	1.2	nS
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	6	nS
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	5	nS

Switching Characteristics Over Operating Range – Industrial[3,4]

Symbol	Parameter	Conditions[1]	ASM2P3805A		Unit
			Min[2]	Max	
t_{PLH} t_{PHL}	Propagation Delay IN_A to OA_n, IN_B to OB_n	C_L= 50pF R_L= 500Ω	1.5	5.2	nS
t_R	Output Rise Time (0.8V to 2.0V)		-	2	nS
t_F	Output Fall Time (2.0V to 0.8V)		-	2	nS
$t_{SK(O)}$	Output skew: skew between outputs of all banks of same package (inputs tied together)		-	0.6	nS
$t_{SK(P)}$	Pulse skew: skew between opposite transitions of same output ($\|t_{PHL} - t_{PLH}\|$)		-	1	nS
$t_{SK(T)}$	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		-	1.2	nS
t_{PZL} t_{PZH}	Output Enable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	6	nS
t_{PLZ} t_{PHZ}	Output Disable Time $\overline{OE}_A$ to OA_n, $\overline{OE}_B$ to OB_n		1.5	5	nS

Note: 1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, $t_{SK(t)}$ are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{CC}, operating temperature and process parameters. These propagation delay limits do not imply skew.

Test Circuits and Waveforms



Test Circuits for All Outputs

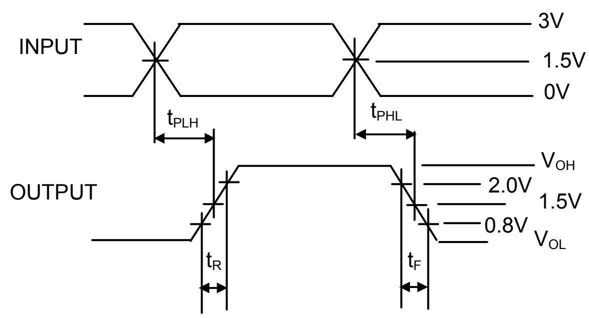
Switch Position

Test	Switch
Disable Low Enable Low	6V
Disable High Enable High	GND

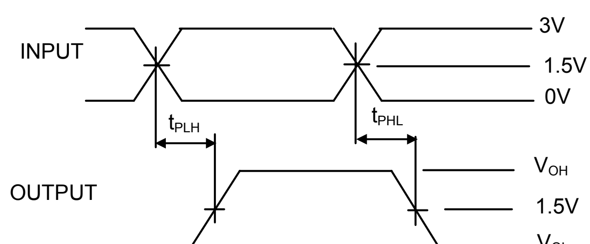
Definitions:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

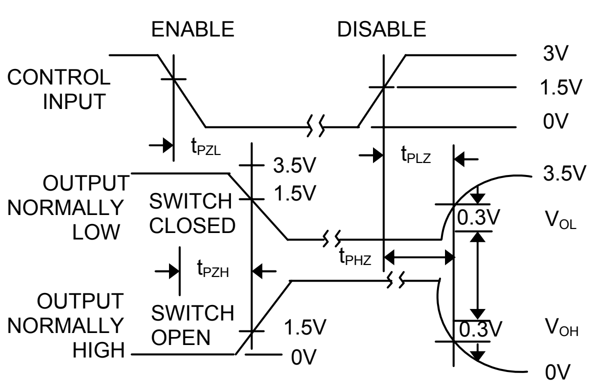


Package Delay



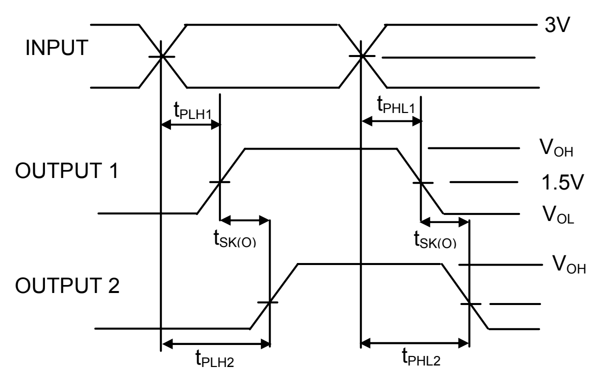
$t_{SK(P)} = | t_{PLH} - t_{PLH} |$

Pulse Skew



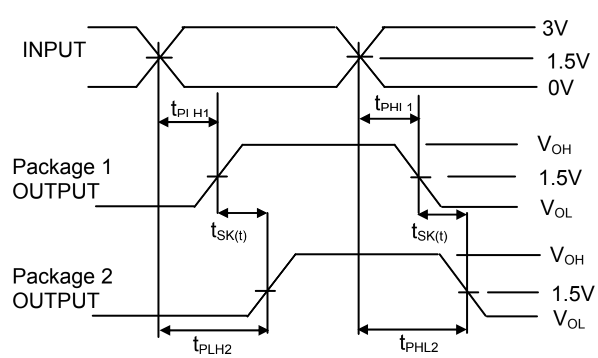
Enable and Disable Times

Note:
Diagram shown for input Control Enable-LOW and input Control Disable-HIGH



$t_{SK(O)} = | t_{PLH2} - t_{PLH1} |$ or $| t_{PHL2} - t_{PHL1} |$

Output Skew – $t_{SK(o)}$



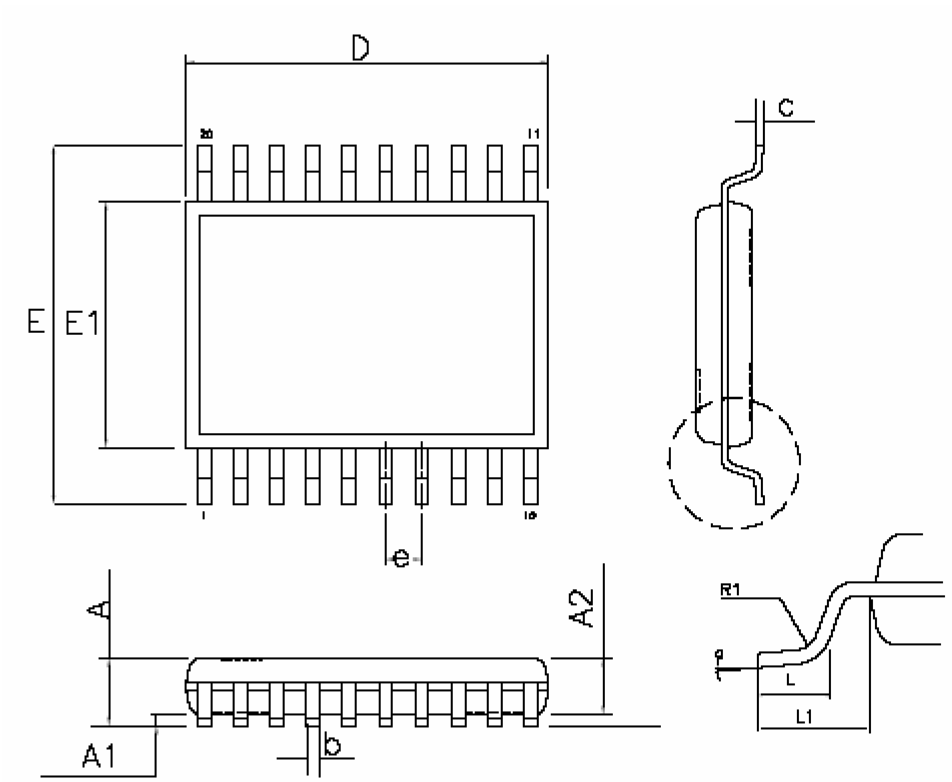
$t_{SK(t)} = | t_{PLH2} - t_{PLH1} |$ or $| t_{PHL2} - t_{PHL1} |$

Package Skew – $t_{SK(t)}$

Note:
Pulse Generator for all Pulses: $f \le 10MHz$; $t_F \le 2.5nS$; $t_R \le 2.5nS$

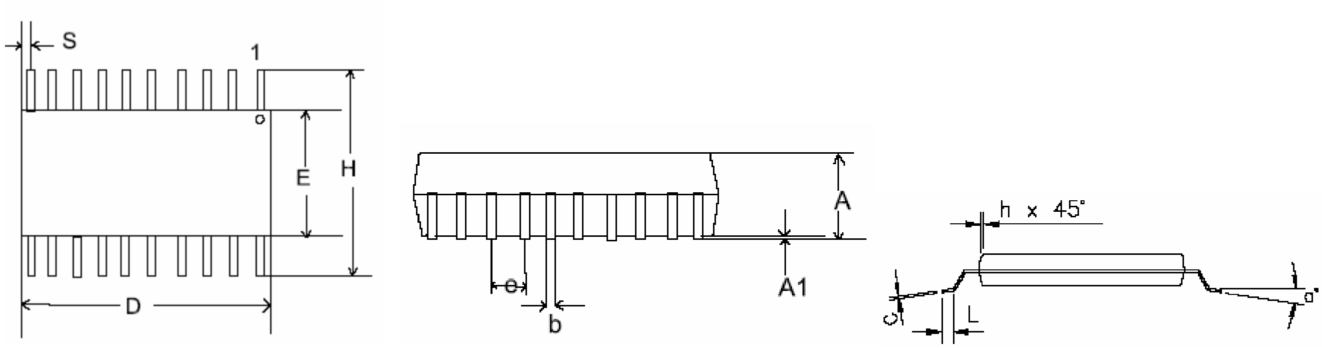
Package Information

20-lead SSOP (209 mil) Package



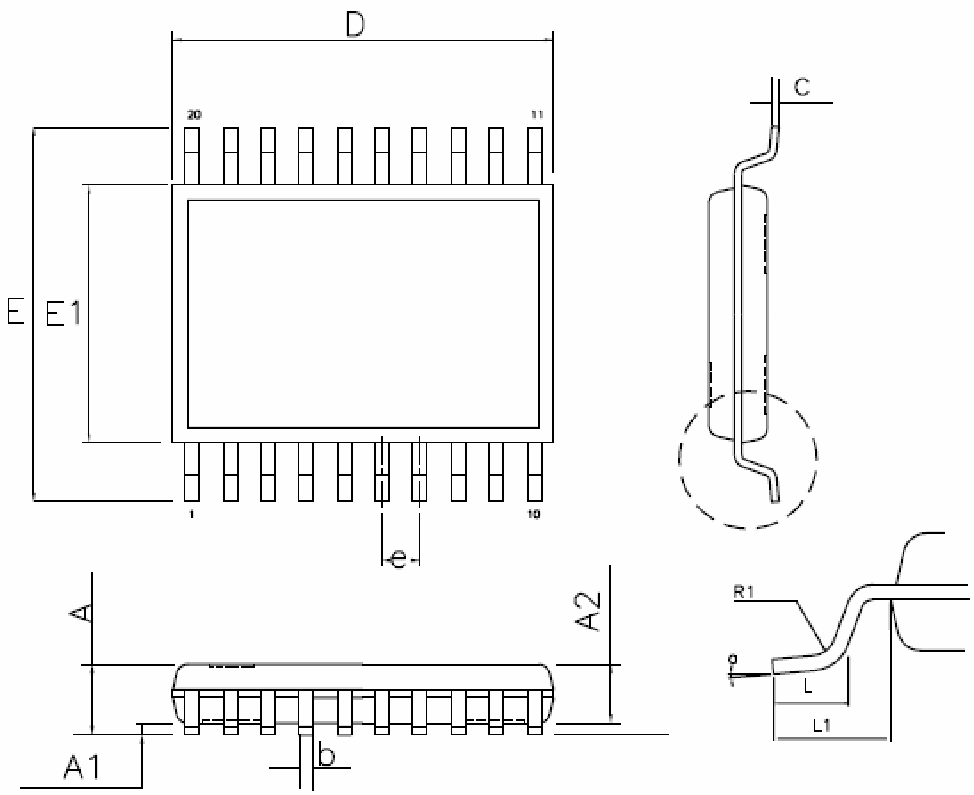
Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	….	0.079	…	2.0
A1	0.002	…	0.05	…..
A2	0.065	0.073	1.65	1.85
D	0.275	0.291	7.00	7.40
c	0.004	0.010	0.09	0.25
E	0.295	0.319	7.50	8.10
E1	0.197	0.220	5.00	5.60
L	0.021	0.037	0.55	0.95
L1	0.050 REF		1.25 REF	
b	0.009	0.015	0.22	0.38
R1	0.004	….	0.09	….
a	0°	8°	0°	8°
e	0.0197 BASE		0.65 BASE	

20-lead QSOP Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.060	0.068	1.52	1.73
A1	0.004	0.008	0.10	0.20
b	0.009	0.012	0.23	0.30
c	0.007	0.010	0.18	0.25
D	0.337	0.344	8.56	8.74
E	0.150	0.157	3.81	3.99
e	0.025 BSC		0.64 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
S	0.056	0.060	1.42	1.52
a	0°	8°	0°	8°

20L SOIC Package (300 mil)



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
A2	0.088	0.094	2.25	2.40
D	0.496	0.512	12.60	13.00
L	0.016	0.050	0.40	1.27
E1	0.291	0.299	7.40	7.60
R1	0.003	….	0.08	…..
b	0.013	0.022	0.33	0.56
c	0.009	0.015	0.23	0.38
E	0.394	0.419	10.00	10.65
e	0.050 BSC		1.27 BSC	
a	0°	8°	0°	8°

Ordering Information

Part Number	Marking	Package Type	Temperature
ASM2P3805AG-20-AR	2P3805AG	20-Pin SSOP, TAPE & REEL, Green	Commercial
ASM2P3805AG-20-AT	2P3805AG	20-Pin SSOP, TUBE, Green	Commercial
ASM2P3805AG-20-DR	2P3805AG	20-Pin QSOP, TAPE & REEL, Green	Commercial
ASM2P3805AG-20-DT	2P3805AG	20-Pin QSOP, TUBE, Green	Commercial
ASM2P3805AG-20-SR	2P3805AG	20-Pin SOIC, TAPE & REEL, Green	Commercial
ASM2P3805AG-20-ST	2P3805AG	20-Pin SOIC, TUBE, Green	Commercial
ASM2I3805AG-20-AR	2I3805AG	20-Pin SSOP, TAPE & REEL, Green	Industrial
ASM2I3805AG-20-AT	2I3805AG	20-Pin SSOP, TUBE, Green	Industrial
ASM2I3805AG-20-DR	2I3805AG	20-Pin QSOP, TAPE & REEL, Green	Industrial
ASM2I3805AG-20-DT	2I3805AG	20-Pin QSOP, TUBE, Green	Industrial
ASM2I3805AG-20-SR	2I3805AG	20-Pin SOIC, TAPE & REEL, Green	Industrial
ASM2I3805AG-20-ST	2I3805AG	20-Pin SOIC, TUBE, Green	Industrial
ASM2P3805A-20-AR	2P3805A	20-Pin SSOP, TAPE & REEL	Commercial
ASM2P3805A-20-AT	2P3805A	20-Pin SSOP, TUBE	Commercial
ASM2P3805A-20-DR	2P3805A	20-Pin QSOP, TAPE & REEL	Commercial
ASM2P3805A-20-DT	2P3805A	20-Pin QSOP, TUBE	Commercial
ASM2P3805A-20-SR	2P3805A	20-Pin SOIC, TAPE & REEL	Commercial
ASM2P3805A-20-ST	2P3805A	20-Pin SOIC, TUBE	Commercial
ASM2I3805A-20-AR	2I3805A	20-Pin SSOP, TAPE & REEL	Industrial
ASM2I3805A-20-AT	2I3805A	20-Pin SSOP, TUBE	Industrial
ASM2I3805A-20-DR	2I3805A	20-Pin QSOP, TAPE & REEL	Industrial
ASM2I3805A-20-DT	2I3805A	20-Pin QSOP, TUBE	Industrial
ASM2I3805A-20-SR	2I3805A	20-Pin SOIC, TAPE & REEL	Industrial
ASM2I3805A-20-ST	2I3805A	20-Pin SOIC, TUBE	Industrial

Device Ordering Information

A S M 2 P 3 8 0 5 A G - 2 0 - D R

R = Tape & reel, T = Tube or Tray

O = SOT	U = MSOP
S = SOIC	E = TQFP
T = TSSOP	L = LQFP
A = SSOP	U = MSOP
V = TVSOP	P = PDIP
B = BGA	D = QSOP
Q = QFN	X = SC-70

DEVICE PIN COUNT

F = LEAD FREE AND RoHS COMPLIANT PART
G = GREEN PACKAGE

PART NUMBER

X= Automotive (-40C to +125C)	I= Industrial (-40C to +85C)	P or n/c = Commercial (0C to +70C)

1 = Reserved	6 = Power Management
2 = Non PLL based	7 = Power Management
3 = EMI Reduction	8 = Power Management
4 = DDR support products	9 = Hi Performance
5 = STD Zero Delav Buffer	0 = Reserved

ALLIANCE SEMICONDUCTOR MIXED SIGNAL PRODUCT

Licensed under US patent #5,488,627, #6,646,463 and #5,631,920.

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Note: This product utilizes US Patent # 6,646,463 Impedance Emulator Patent issued to Alliance Semiconductor, dated 11-11-2003