OKI

Oki, Network Solutions
for a Global Society

FEDR27V1641L-02-H1
Issue Date: April 21, 2006

OKI Semiconductor
MR27V1641L

16M × 1–Bit Serial Production Programmed ROM (P2ROM)

GENERAL DESCRIPTION

   The MR27V1641L is a 16 Mbit Production Programmed Read-Only Memory, which is configured as 16,777,216 word × 1-bit. The MR27V1641L supports a simple read operation using a single 3.0V or 3.6V power supply and a Serial Peripheral Interface (SPI) compatible serial bus.
   The MR27V1641L have data programmed and have functions tested at OKI factory. (Using the DC pins for the programming function is NOT allowed)

FEATURES

·Read Operation
- +3.0V or +3.6 V power supply
- 16,777,216 × 1-bit
- Access time: 30MHz serial clock (FAST-READ)
-                20MHz serial clock (READ)
- Read Identification Instruction
- Active read current: 25 mA (FAST-READ)
-                      20 mA (READ)
- Standby current   : 50 μA
- Serial Clock Input and Data Input/Output
- Input Data Format : 1-byte Command code, 3-byte address, 1-byte dummy (FAST-READ)
                       1-byte Command code, 3-byte address (READ)

PACKAGES

· MR27V1641L-xxxMP
-    16-pin plastic SOP (P-SOP16-375-1.27-K)
-    RoHS Compliant Part Number : Please refer to page 17

PIN CONFIGURATION (TOP VIEW)

```
      NC  1  ◯      16  SCLK
      Vcc 2          15  SI
      NC  3          14  NC
      DC  4          13  NC
      NC  5          12  NC
      NC  6          11  NC
     #CS  7          10  GND
      SO  8           9  NC
```
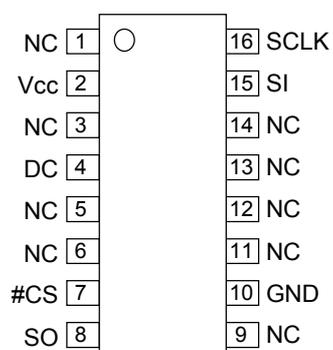
Under Read Operation

Pin name	Functions under Read Operation
#CS	Chip Select
SI	Serial Data Input
SO	Serial Data Output
SCLK	Clock Input
V_{CC}	Power supply voltage
GND	Ground
DC	Don't care (0v - Vcc) <for reference> Program power supply voltage Vpp under Programming operation
NC	Non connection

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READ COMMAND DEFINITION

Command	Read Array (byte)	Note
1st	03[H]	1
2nd	AD1	2
3rd	AD2	2
4th	AD3	2
Action	N byte read out until #CS goes high	3

Note:
1. The 1st command 03[H] is a Read command
2. AD1 to AD3 are address input data
3. Data output

Details of command and address are shown as follows.

1-byte command code								
READ	0	0	0	0	0	0	1	1
3-byte address (0 to 3FFF[H])								
AD1:	X	X	X	A20	A19	A18	A17	A16
AD2:	A15	A14	A13	A12	A11	A10	A9	A8
AD3:	A7	A6	A5	A4	A3	A2	A1	A0

Note:

X: Dummy bit

FAST READ COMMAND DEFINITION

Command	Read Array (byte)	Note
1st	0B[H]	1
2nd	AD1	2
3rd	AD2	2
4th	AD3	2
5th	X	3
Action	N byte read out until #CS goes high	4

Note:

1. The 1st command 0B[H] is a Read command
2. AD1 to AD3 are address input data
3. X is a dummy cycle
4. Data output

Details of command and address are shown as follows.

1-byte command code								
FAST-READ	0	0	0	0	1	0	1	1
3-byte address (0 to 3FFF[H])								
AD1:	X	X	X	A20	A19	A18	A17	A16
AD2:	A15	A14	A13	A12	A11	A10	A9	A8
AD3:	A7	A6	A5	A4	A3	A2	A1	A0

Note:

X: Dummy bit

READ IDENTIFICATION COMMAND DEFINITION

Command	Read Array (byte)	Note
1st	9F[H]	1
Action	3 byte read out	2

Note:
1. The 1st command 9F[H] is a Read Identification command
2. Identification output

Details of command and address are shown as follows.

1-byte command code								
RDID	1	0	0	1	1	1	1	1

IDENTIFICATION DEFINITION

Manufacturer Identification	Device Identification	
	Type	Capacity
AE[H]	41[H]	13[H]

DEVICE OPERATION

1. Command "03h" or "0Bh" makes this LSI become and keep active mode until next #CS High.
2. Incorrect command makes this LSI become and keep standby mode until next #CS Low. In standby mode, SO pin is High-Z.
3. At Power-up, the device must not be selected (that is #CS must follow the voltage applied on Vcc) until Vcc reaches the operating value.

COMMAND DESCRIPTION

1. Read Array
This command consists of the 4-byte code. The 1st code is a command which decides if the device becomes standby or active mode. The 1st code "03h" activates the device. The 2nd code to the 4th code are address inputs.

2. Fast Read Array
This command consists of the 5-byte code. The 1st code is a command which decides if the device becomes standby or active mode. The 1st code "0Bh" activates the device. The 2nd code to the 4th code are address. The 5th code is a dummy cycle.

3. Identification Read Array
This command consists of the 1-byte code. The 1st code is a command which decides if the device becomes standby or active mode. The 1st code "9Fh" activates the device.

4. Standby
When #CS is high, the device is put in standby mode at the next rising edge of SCLK. Maximum standby current is 50uA. When the above-mentioned 1st code is incorrect command, the device is put in standby mode at the next rising edge of SCLK.

DATA SEQUENCE

The data is serially sent out through SO pin, synchronized with the falling edge of SCLK. Meanwhile input data is also serially read in through SI pin, synchronized with the rising edge of SCLK. The bit sequence for both input and output data are bit7 (MSB) first, bit6, bit 5, …, and bit0(LSB).

ADDRESS SEQUENCE

The address assignment is described at the COMMAND DEFINITION on page 4.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Storage temperature	Tstg	—	−55 to 125	°C
Input voltage	V_I		−0.5 to V_{CC}+0.5	V
Output voltage	V_O	relative to V_{SS}	−0.5 to V_{CC}+0.5	V
Power supply voltage	V_{CC}		−0.5 to 5	V
Power dissipation per package	P_D	Ta = 25°C	1.0	W
Output short circuit current	I_{OS}	—	10	mA

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating temperature under bias	Ta		0	—	70	℃
V_{CC} power supply voltage	V_{CC}	V_{CC} = 3.0 to 3.6 V	3.0	—	3.6	V
Input "H" level	V_{IH}		2.4	—	V_{CC}+0.5∗	V
Input "L" level	V_{IL}		−0.5∗∗	—	0.6	V

Voltage is relative to V_{SS}.

∗ : Vcc+1.5V(Max.) when pulse width of positive overshoot is less than 10ns.

∗∗ : -1.5V(Min.) when pulse width of negative overshoot is less than 10ns.

PIN CAPACITANCE

(V_{CC} = 3.3 V, Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input	C_{IN1}	V_I = 0 V	—	—	10	
Output	C_{OUT}	V_O = 0 V	—	—	10	pF
DC	C_{DC}	V_I = 0 V	—	—	200	

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{CC} = 3.0 V to 3.6V, Ta = 0 to 70°C)

parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input leakage current	I_{LI}	V_I = 0 to V_{CC}	—	—	10	μA
Output leakage current	I_{LO}	V_O = 0 to V_{CC}	—	—	10	μA
V_{CC} power supply current (Standby)	I_{SB1}	#CS = V_{CC}	—	—	50	μA
	I_{SB2}	#CS = V_{IH}	—	—	1	mA

V_{CC} power supply current (Read)	I_{CC1}	#CS = V_{IL}
		f = 20MHz
		SO=open
			—	—	20	mA

V_{CC} power supply current (Fast Read)	$I_{CC1}F$	#CS = V_{IL}
		f = 30MHz
		SO=open
			—	—	25	mA

Input "H" level	V_{IH}	—	2.4	—	V_{CC}+0.5∗	V
Input "L" level	V_{IL}	—	−0.5∗∗	—	0.6	V
Output "H" level	V_{OH}	I_{OH} = −100 μA	2.4	—	—	V
Output "L" level	V_{OL}	I_{OL} = 500 μA	—	—	0.4	V

Voltage is relative to V_{SS}.

∗ : Vcc+1.5V(Max.) when pulse width of positive overshoot is less than 10ns.

∗∗ : -1.5V(Min.) when pulse width of negative overshoot is less than 10ns.

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AC Characteristics

FAST-READ

(V$_{CC}$ = 3.0 V to 3.6 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock frequency	t$_{SCLK}$	—	—	30 *	MHz
Clock High time	t$_{SKH}$	—	14	—	ns
Clock Low time	t$_{SKL}$	—	14	—	ns
Input signal Rise time	t$_R$	—	—	3	ns
Input signal Fall time	t$_F$	—	—	3	ns
#CS Lead Clock Time	t$_{CSA}$	—	10	—	ns
#CS Setup Time	t$_{CS}$	—	5	—	ns
#CS Lag Clock Time	t$_{CSB}$	—	5	—	ns
#CS Hold Time	t$_{CH}$	—	5	—	ns
#CS High Time	t$_{CSH}$	—	80	—	ns
SI Setup Time	t$_{DS}$	—	2	—	ns
SI Hold Time	t$_{DH}$	—	10	—	ns
Access time	t$_{AA}$	—	—	14	ns
SO Hold Time	t$_{DOH}$	—	0	—	ns
SO Floating Time	t$_{DOZ}$	—	—	15	ns

*: FAST-READ instructions

READ

(V$_{CC}$ = 3.0 V to 3.6 V, Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock frequency	t$_{SCLK}$	—	—	20 **	MHz
Clock High time	t$_{SKH}$	—	20	—	ns
Clock Low time	t$_{SKL}$	—	20	—	ns
Input signal Rise time	t$_R$	—	—	3	ns
Input signal Fall time	t$_F$	—	—	3	ns
#CS Lead Clock Time	t$_{CSA}$	—	10	—	ns
#CS Setup Time	t$_{CS}$	—	5	—	ns
#CS Lag Clock Time	t$_{CSB}$	—	5	—	ns
#CS Hold Time	t$_{CH}$	—	5	—	ns
#CS High Time	t$_{CSH}$	—	80	—	ns
SI Setup Time	t$_{DS}$	—	2	—	ns
SI Hold Time	t$_{DH}$	—	10	—	ns
Access time	t$_{AA}$	—	—	14	ns
SO Hold Time	t$_{DOH}$	—	0	—	ns
SO Floating Time	t$_{DOZ}$	—	—	15	ns

**: READ instructions

Measurement conditions

Input signal level------------------------------- Vcc/0v
Input timing reference level ------------------ 0.7Vcc/ 0.3Vcc
Output load ------------------------------------ 30 pF
Output timing reference level---------------- 0.5 Vcc

Output

30 pF
(Including scope and jig)
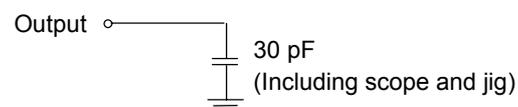
TIMING CHART (READ CYCLE)

Serial Data Input/Output Timing
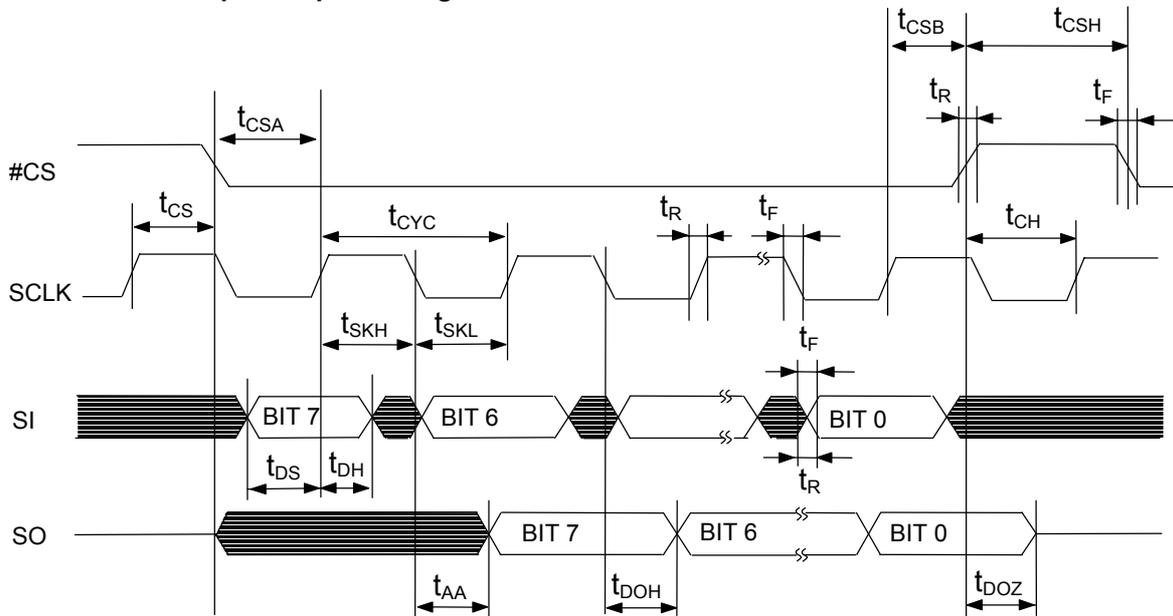
Standby Timing

1st byte = incorrect code
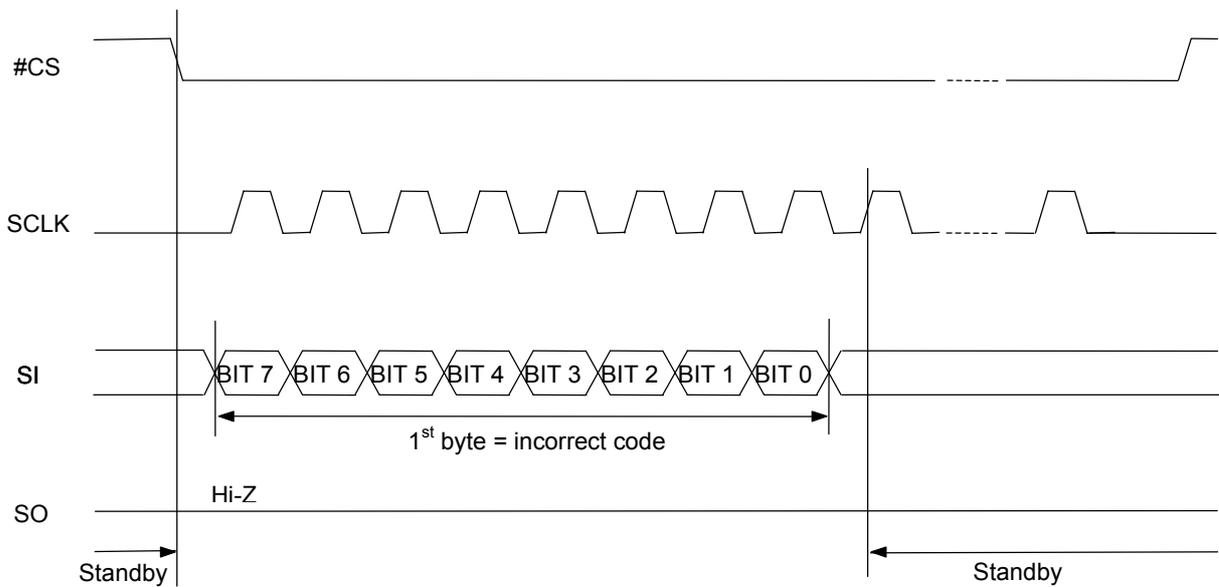
Incorrect command makes this LSI become and keep standby mode until next #CS rising edge. In standby mode, SO pin is High-Z.

Read Array Timing Waveform
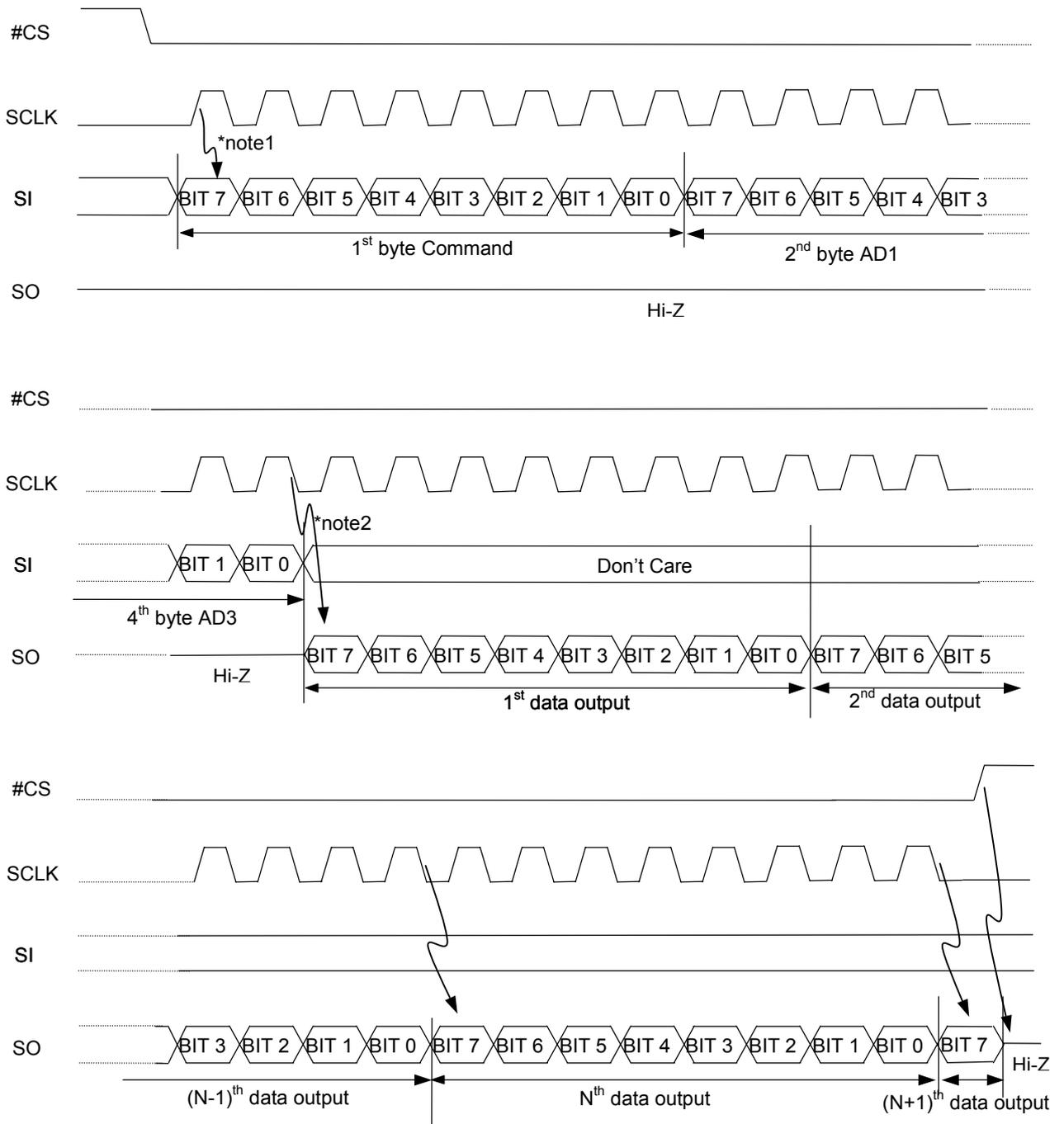
Note:
1. Input data are latched at SCLK-rising edge.
2. Data-output starts at SCLK-falling edge in bit0 of the 4th byte.

Fast Read Array Timing Waveform
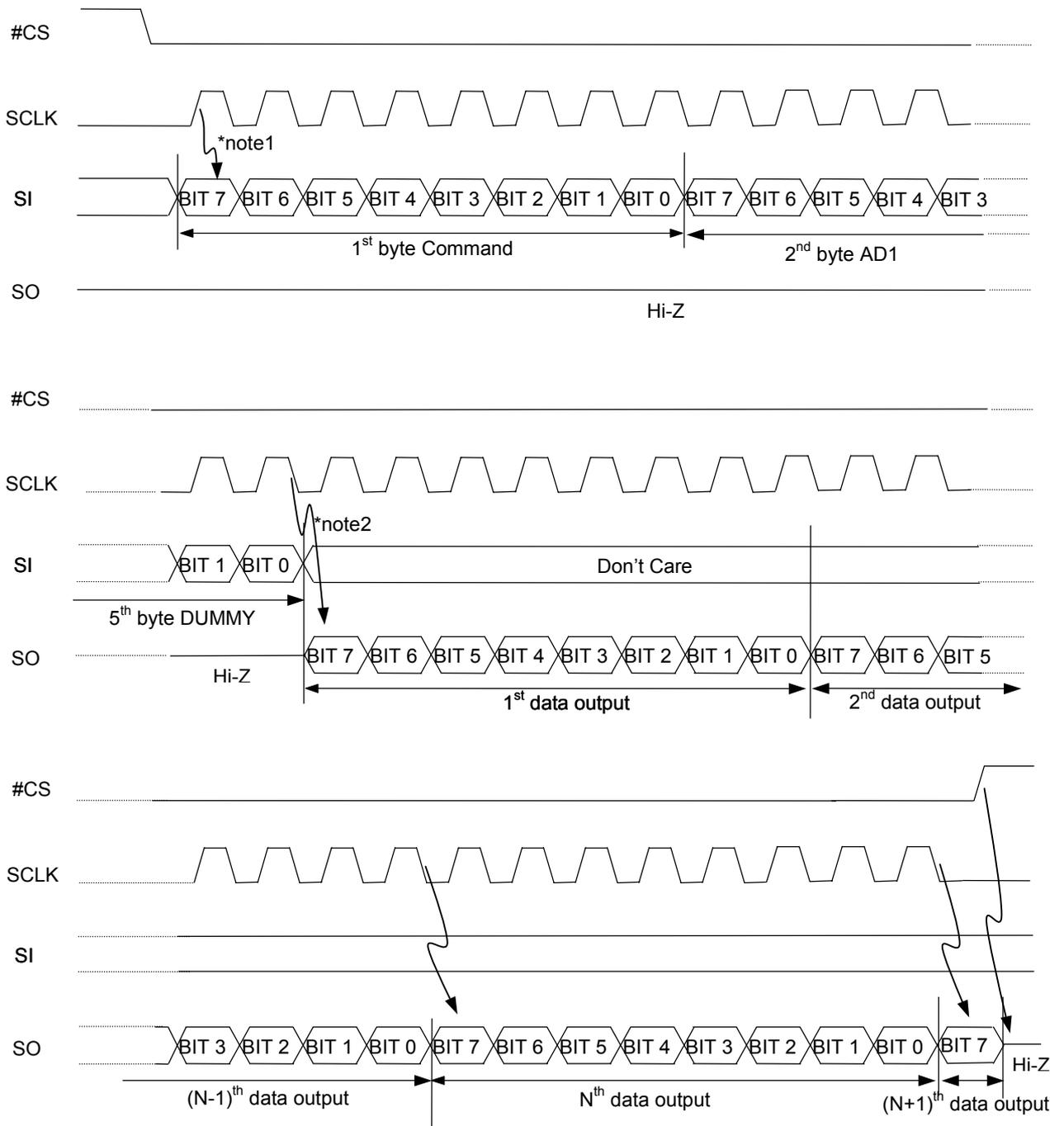
Note:
1. Input data are latched at SCLK-rising edge.
2. Data-output starts at SCLK-falling edge in bit0 of the 5th byte.

Read Identification Timing Waveform
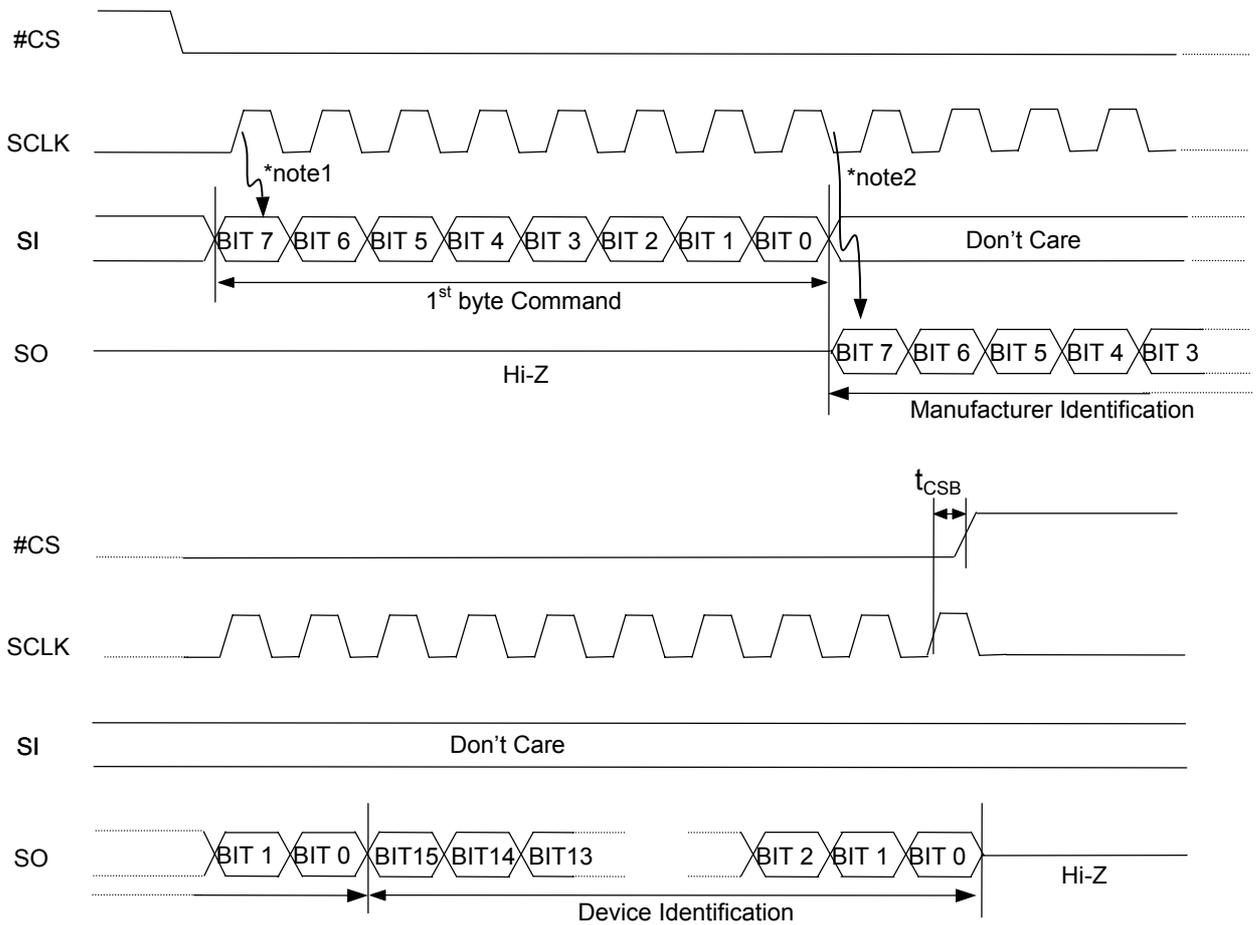

Note:
1. Input data are latched at SCLK-rising edge.
2. Data-output starts at SCLK-falling edge in bit0 of the 1st byte.

PACKAGE DIMENSIONS

(Unit: mm)

注記
1. リード幅にはダムバーカット残りを含まない。
2. パッケージ幅にはモールド樹脂バリ及びサポートカット残りを含まない。
   又モールドの上下のズレは含まない。
3. SEATING PLANEとは、パッケージを取り付ける面に対して、
   パッケージが接触し合う面である。

NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT
   PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE
   IS MOUNTED ON AND GETS IN CONTACT WITH.

沖電気工業株式会社 SiMC ATPビジネス本部 ATP品質保証部 Oki Electric Industry Co.,Ltd. SiMC ATP Business Division ATP Quality Assurance Department.			
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	42ALLOY	DWG No.	QSL-39475
LEAD FINISH	Sn/1~38i		
SOLDER THICKNESS	MORE THAN 5μm	TITLE	P-SOP16-375-1.27-K
PACKAGE MASS (g)	0.41TYP.	DESIGNED	S. Ohno	Sep/24/2004
REVISION	1	CHECKED	E. Yamada	Sep/24/2004
REVISED		CHECKED	Y. Ino	Sep/24/2004
ISSUED	Sep/24/2004	APPROVED	S. Ohno	Sep/24/2004

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDR27V1641L-02-H1	April 21, 2006	–	–	Final edition 1

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1. The information contained herein can change without notice owing to product and/or technical improvements. Before using the product, please make sure that the information being referred to is up-to-date.

2. The outline of action and examples for application circuits described herein have been chosen as an explanation for the standard action and performance of the product. When planning to use the product, please ensure that the external conditions are reflected in the actual circuit, assembly, and program designs.

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OKI NVM Code Information

MR XX X XXX XX X – XXX XX ZXXX

MR : NVM

Product Type
27   : Single chip
26   : MCP

Power Supply
V   : 3.0 to 3.6V
T   : 2.7 to 3.6V

Density (1-3 digits)
4 : 4M   64 : 64M
8 : 8M   128 : 128M
16 : 16M   256 : 256M
32 : 32M

Mode (2 digits)

0 : Standard Mode
5 : Page Mode   +

0: MROM pin
1: x8 (32pin)
2: x8/x16(Flash compatible)
3. X8/x16(Oki original)
4: x16
5: x16/x32

40 : MX interface SPI
41 : ST interface SPI
66 : Synchronous

Option
NA : Loose
Z060 : Tape&Reel (R1)
Z080 : Tape&Reel (R3)
Z03A : RoHS Compliant (Loose)
Z03B : RoHS Compliant (Tape&Reel, R1)
Z03D : RoHS Compliant (Tape&Reel, R3)
Z04A : High temp lead frame (Loose)
Z04B : High temp lead frame (Tape&Reel, R1)
Z04D : High temp lead frame (Tape&Reel, R3)

Note : " Z" will be deleted if P/N exceeds 20 digits

Package Type

JA : 42SOJ   TA : 32TSOPI, 48TSOP2
LA : 48BGA   56TSOPI, 70TSOP2
MA : 28SOP 32SOP 44SOP   86TSOP2
MB: 70SSOP   TM : 50TSOP2
MP : 40SOP, 16SOP   TN : 48TSOPI
RA : 42DIP 32DIP   TP : 44TSOP2
RP : 40DIP   WA : Chip

Customer Code (2-3 digits)

Die Generation