Compact Synchronous Buck Regulators

ISL8002, ISL8002A, ISL80019, ISL80019A

ISL8002, ISL8002A, ISL80019 and ISL80019A are highly efficient, monolithic, synchronous step-down DC/DC converters that can deliver up to 2A of continuous output current from a 2.7V to 5.5V input supply. They use peak current mode control architecture to allow very low duty cycle operation. They operate at either 1MHz or 2MHz switching frequency, thereby providing superior transient response and allowing for the use of small inductors. They also have excellent stability and provide both internal and external compensation options.

ISL8002, ISL8002A, ISL80019 and ISL80019A integrate very low $r_{DS(ON)}$ MOSFETs in order to maximize efficiency. In addition, since the high side MOSFET is a PMOS, the need for a Boot capacitor is eliminated, thereby reducing external component count. They can operate at 100% duty cycle (at 1MHz) with a dropout of 200mV at 2A output current.

These devices can be configured for either PFM (discontinuous conduction) or PWM (continuous conduction) operation at light load. PFM provides high efficiency by reducing switching losses at light loads and PWM reduces noise susceptibility and RF interference.

These devices are offered in a space saving 8 pin 2mmx2mm TDFN lead free package with exposed pad for improved thermal performance. The complete converter occupies less than $0.10in^2$ area.

Features

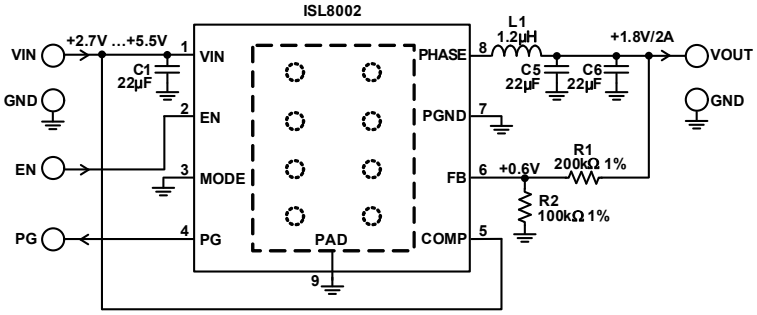
- V_{IN} range 2.7V to 5.5V
- V_{OUT} range is 0.6V to V_{IN}
- I_{OUT} maximum is 1.5A or 2A (see Table 1 on page 3)
- Switching frequency is 1MHz or 2MHz (see Table 1 on page 3)
- Internal or external compensation option
- Selectable PFM or PWM operation option
- Overcurrent and short circuit protection
- Over-temperature/thermal protection
- V_{IN} Undervoltage Lockout and V_{OUT} Overvoltage Protection
- Up to 95% peak efficiency

Applications

- General purpose point of load DC/DC
- Set-top boxes and cable modems
- FPGA power
- DVD, HDD drives, LCD panels, TV

Related Literature

- See AN1803, “1.5A/2A Low Quiescent Current High Efficiency Synchronous Buck Regulator”



$$R_1 = R_2\left(\frac{V_O}{VFB} - 1\right) \quad \text{(EQ. 1)}$$

FIGURE 1. TYPICAL APPLICATION CIRCUIT CONFIGURATION (INTERNAL COMPENSATION OPTION)

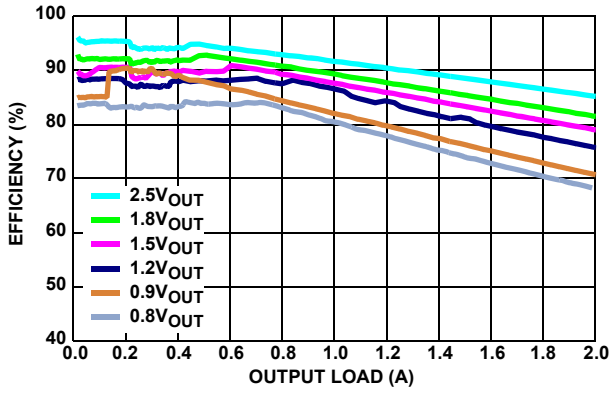


FIGURE 2. EFFICIENCY vs LOAD
F_{SW} = 1MHz, V_{IN} = 3.3V, MODE = PFM, T_A = +25°C

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TABLE 1. SUMMARY OF KEY DIFFERENCES

PART#	I_{OUT} (MAX) (A)	F_{SW} (MHz)	V_{IN} RANGE (V)	V_{OUT} RANGE (V)	PACKAGE SIZE
ISL80019	1.5	1	2.7 to 5.5	0.6 to 5.5	8 pin 2mmx2mm TDFN
ISL80019A	1.5	2			
ISL8002	2	1			
ISL8002A	2	2			

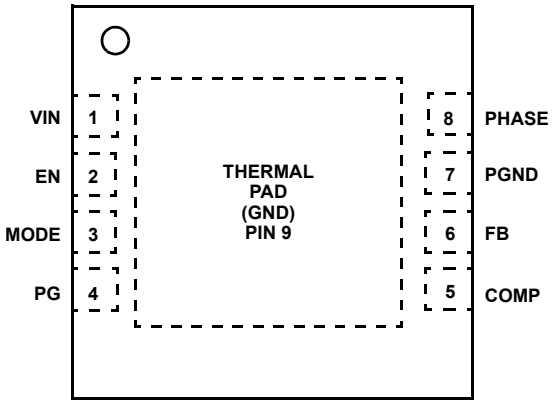
NOTE: In this datasheet, the parts in the table above are collectively called "device".

TABLE 2. COMPONENT VALUE SELECTION TABLE

V_{OUT} (V)	C1 (µF)	C5, C6 (µF)	C4 (pF)	L1 (µH)	R1 (kΩ)	R2 (kΩ)
0.8	22	22	22	1.0~2.2	33	100
1.2	22	22	22	1.0~2.2	100	100
1.5	22	22	22	1.0~2.2	150	100
1.8	22	22	22	1.0~3.3	200	100
2.5	22	22	22	1.5~3.3	316	100
3.3	22	22	22	1.5~4.7	450	100

Pin Configuration

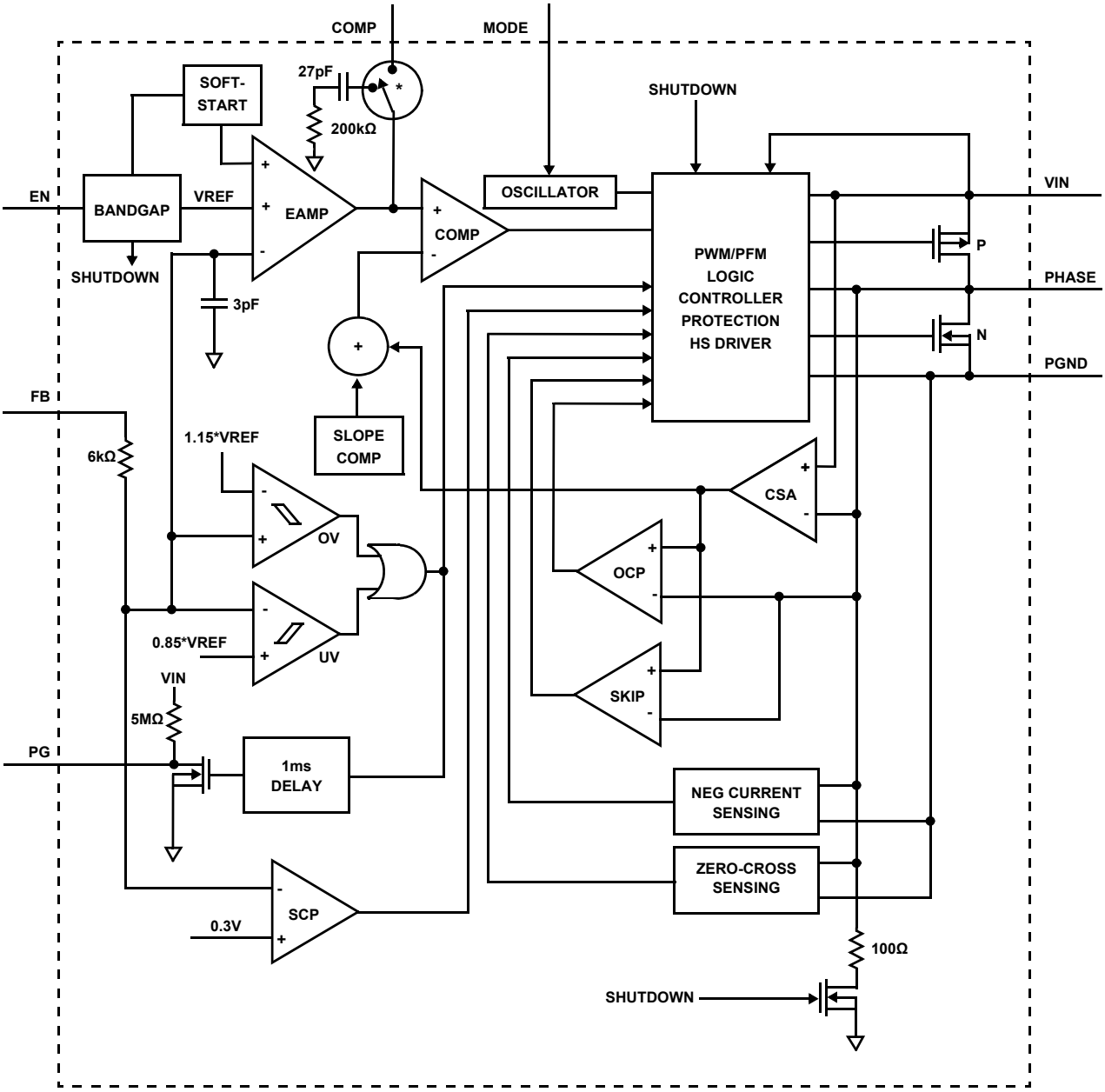
ISL8002, ISL8002A, ISL80019, ISL80019A
(8 LD 2x2 TDFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	PIN DESCRIPTION
1	VIN	The input supply for the power stage of the PWM regulator and the source for the internal linear regulator that provides bias for the IC. Place a minimum of 10µF ceramic capacitance from VIN to GND and as close as possible to the IC for decoupling.
2	EN	Device enable input. When the voltage on this pin rises above 1.4V, the device is enabled. The device is disabled when the pin is pulled to ground. When the device is disabled, a 100Ω resistor discharges the output through the PHASE pin. See Figure 3, “FUNCTIONAL BLOCK DIAGRAM” on page 5 for details.
3	MODE	Mode selection pin. Connect to logic high or input voltage VIN for PWM mode. Connect to logic low or ground for PFM mode. There is an internal 1MΩ pull-down resistor to prevent an undefined logic state in case the MODE pin is left floating, however, it is not recommended to leave this pin floating.
4	PG	Power Good output is pulled to ground during the soft-start interval and also when the output voltage is below regulation limits. There is an internal 5MΩ internal pull-up resistor on this pin.
5	COMP	COMP is the output of the error amplifier. When COMP is tied high to VIN, compensation is internal. When COMP is connected with a series resistor and capacitor to GND, compensation is external. See “Loop Compensation Design” on page 19 for more detail.
6	FB	Feedback pin for the regulator. FB is the negative input to the voltage loop error amplifier. The output voltage is set by an external resistor divider connected to FB. In addition, the Power Good PWM regulator’s power-good and undervoltage protection circuits use FB to monitor the output voltage.
7	PGND	Power and analog ground connections. Connect directly to the board GROUND plane.
8	PHASE	Power stage switching node for output voltage regulation. Connect to the output inductor. This pin is discharged by an 100Ω resistor when the device is disabled. See Figure 3, “FUNCTIONAL BLOCK DIAGRAM” on page 5 for details.
9	THERMAL PAD (T-PAD)	Power ground. This thermal pad provides a return path for the power stage and switching currents, as well as a thermal path for removing heat from the IC to the board. Place thermal vias to the PGND plane in this pad.

Functional Block Diagram



*** By default, when COMP is tied to VIN, the voltage loop is internally compensated with the 27pF and 200kΩ RC network. Please see "COMP" pin in the "Pin Descriptions" table on page 4 for more details.**

FIGURE 3. FUNCTIONAL BLOCK DIAGRAM

Ordering Information

PART NUMBER (Notes 1, 2, 3)	TAPE AND REEL QUANTITY	PART MARKING	TECHNICAL SPECIFICATIONS	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL8002IRZ-T	1000	002	2A, 1MHz	-40 to +85	8 Ld TDFN	L8.2x2C
ISL8002IRZ-T7A	250	002	2A, 1MHz	-40 to +85	8 Ld TDFN	L8.2x2C
ISL8002AIRZ-T	1000	02A	2A, 2MHz	-40 to +85	8 Ld TDFN	L8.2x2C
ISL8002AIRZ-T7A	250	02A	2A, 2MHz	-40 to +85	8 Ld TDFN	L8.2x2C
ISL80019IRZ-T	1000	019	1.5A, 1MHz	-40 to +85	8 Ld TDFN	L8.2x2C
ISL80019IRZ-T7A	250	019	1.5A, 1MHz	-40 to +85	8 Ld TDFN	L8.2x2C
ISL80019AIRZ-T	1000	19A	1.5A, 2MHz	-40 to +85	8 Ld TDFN	L8.2x2C
ISL80019AIRZ-T7A	250	19A	1.5A, 2MHz	-40 to +85	8 Ld TDFN	L8.2x2C
ISL8002FRZ-T	1000	02F	2A, 1MHz	-40 to +125	8 Ld TDFN	L8.2x2C
ISL8002FRZ-T7A	250	02F	2A, 1MHz	-40 to +125	8 Ld TDFN	L8.2x2C
ISL8002AFRZ-T	1000	2AF	2A, 2MHz	-40 to +125	8 Ld TDFN	L8.2x2C
ISL8002AFRZ-T7A	250	2AF	2A, 2MHz	-40 to +125	8 Ld TDFN	L8.2x2C
ISL80019FRZ-T	1000	19F	1.5A, 1MHz	-40 to +125	8 Ld TDFN	L8.2x2C
ISL80019FRZ-T7A	250	19F	1.5A, 1MHz	-40 to +125	8 Ld TDFN	L8.2x2C
ISL80019AFRZ-T	1000	9AF	1.5A, 2MHz	-40 to +125	8 Ld TDFN	L8.2x2C
ISL80019AFRZ-T7A	250	9AF	1.5A, 2MHz	-40 to +125	8 Ld TDFN	L8.2x2C

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL8002, ISL8002A, ISL80019, ISL80019A. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

VIN . . . . . -0.3V to 6V (DC) or 7V (20ms)
PHASE . . . . . -1.5V (100ns)/-0.3V (DC) to 6V (DC) or 7V (20ms)
EN, COMP, PG, MODE . . . . . -0.3V to VIN+0.3V
FB . . . . . -0.3V to 2.7V

Recommended Operating Conditions

VIN Supply Voltage Range . . . . . 2.7V to 5.5V
Load Current Range . . . . . 0A to 2A
Junction Temperature Range . . . . . -40°C to +125°C

Thermal Information

Thermal Resistance (Typical, Notes 4, 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
2x2 TDFN Package	71	7

Junction Temperature Range . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

T_J = -40°C to +125°C, V_{IN} = 2.7V to 5.5V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range , -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
INPUT SUPPLY						
V_{IN} Undervoltage Lockout Threshold	V_{UVLO}	Rising, no load		2.5	**2.7**	V
		Falling, no load	**2.2**	2.4		V
Quiescent Supply Current	I_{VIN}	MODE = PFM (GND), F_{SW} = 2MHz, no load at the output		35	**60**	µA
		MODE = PWM (VIN), F_{SW} = 1MHz, no load at the output		7	**15**	mA
		MODE = PWM (VIN), F_{SW} = 2MHz, no load at the output		10	**22**	mA
Shut Down Supply Current	I_{SD}	MODE = PFM (GND), V_{IN} = 5.5V, EN = low		5	**10**	µA
OUTPUT REGULATION						
Feedback Voltage	V_{FB}		**0.595**	0.600	**0.605**	V
		T_J = -40°C to +125°C	0.589		0.605	V
VFB Bias Current	I_{VFB}	V_{FB} = 2.7V. T_J = -40°C to +125°C	-120	50	350	nA
Line Regulation		V_{IN} = V_O + 0.5V to 5.5V (minimal 2.7V) T_J = -40°C to +125°C	-0.2	-0.05	0.1	%/V
Load Regulation		See Note 7		< -0.2		%/A
Soft-Start Ramp Time Cycle				1		ms
PROTECTIONS						
Positive Peak Current Limit	IPLIMIT	2A application	**3**	3.5	**4**	A
		1.5A application	**2.1**	2.5	**2.9**	A
Peak Skip Limit	I_{SKIP}	V_{IN} = 3.6, V_{OUT} = 1.8V (See "Applications Information" on page 19 for more detail)		450		mA
Zero Cross Threshold			**-170**	-70	**30**	mA
Negative Current Limit	INLIMIT		**-2.3**	-1.5	**-1**	A
Thermal Shutdown		Temperature rising		150		°C
Thermal Shutdown Hysteresis		Temperature falling		25		°C

Electrical Specifications T_J = -40°C to +125°C, V_{IN} = 2.7V to 5.5V, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range , -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
COMPENSATION						
Error Amplifier Trans-Conductance		COMP tied VIN		40		µA/V
		COMP with RC		120		µA/V
Trans-Resistance	RT		**0.24**	0.3	**0.40**	Ω
LX						
P-Channel MOSFET ON-Resistance		V_{IN} = 5V, I_O = 200mA		117		mΩ
N-Channel MOSFET ON-Resistance		V_{IN} = 5V, I_O = 200mA		86		mΩ
LX Maximum Duty Cycle				100		%
LX Minimum On-Time		MODE = PWM (High) 1MHz		60	**80**	ns
OSCILLATOR						
Nominal Switching Frequency	F_{SW}	ISL8002, ISL80019	**850**	1000	**1150**	kHz
		ISL8002A, ISL80019A	**1700**	2000	**2300**	kHz
PG						
Output Low Voltage		1mA sinking current			**0.3**	V
Delay Time (Rising Edge)			**0.5**	1	**2**	ms
PGOOD Delay Time (Falling Edge)				15		µs
PG Pin Leakage Current		PG = VIN		0.01	**0.1**	µA
OVP PG Rising Threshold			**110**	115	**120**	%
OVP PG Hysteresis				5		%
UVP PG Rising Threshold			**80**	85	**90**	%
UVP PG Hysteresis				5		%
EN AND MODE LOGIC						
Logic Input Low					**0.4**	V
Logic Input High			**1.4**			V
Logic Input Leakage Current	I_{MODE}	Pulled up to 5.5V		5.5	**8**	µA

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
7. Not tested in production. Characterized using evaluation board. Refer to Figures 12 through 14 load regulation diagrams. +105°C T_A represents near worst case operating point.

Typical Performance Curves

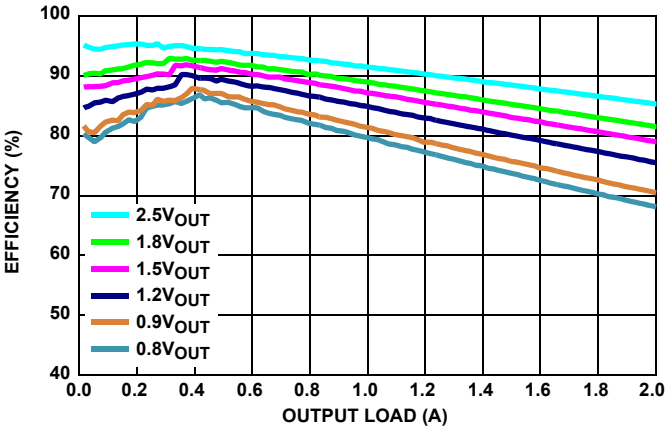


FIGURE 4. EFFICIENCY vs LOAD
F_{SW} = 2MHz, V_{IN} = 3.3V, MODE = PFM, T_A = +25°C

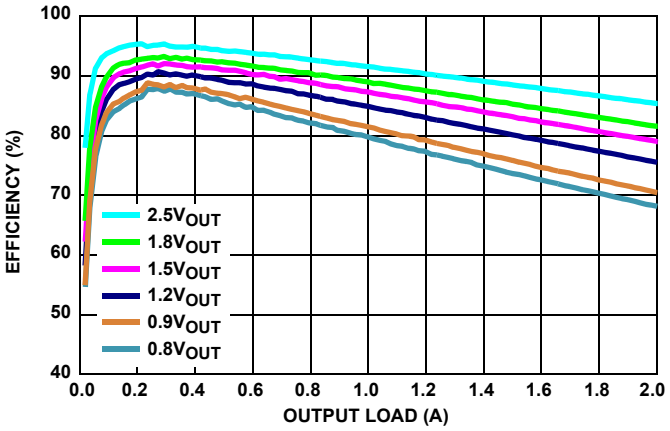


FIGURE 5. EFFICIENCY vs LOAD
F_{SW} = 2MHz, V_{IN} = 3.3V, MODE = PWM, T_A = +25°C

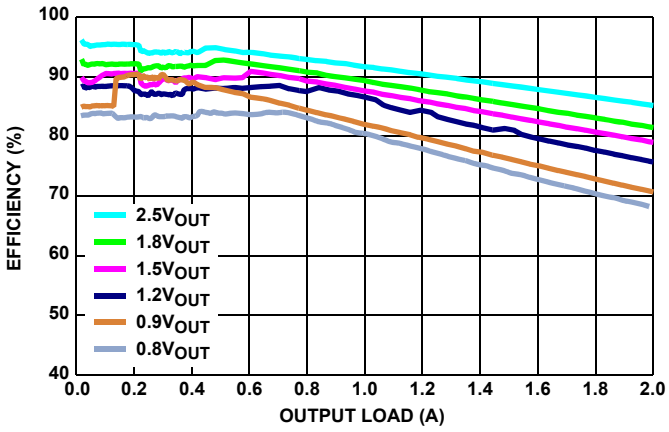


FIGURE 6. EFFICIENCY vs LOAD
F_{SW} = 1MHz, V_{IN} = 3.3V, MODE = PFM, T_A = +25°C

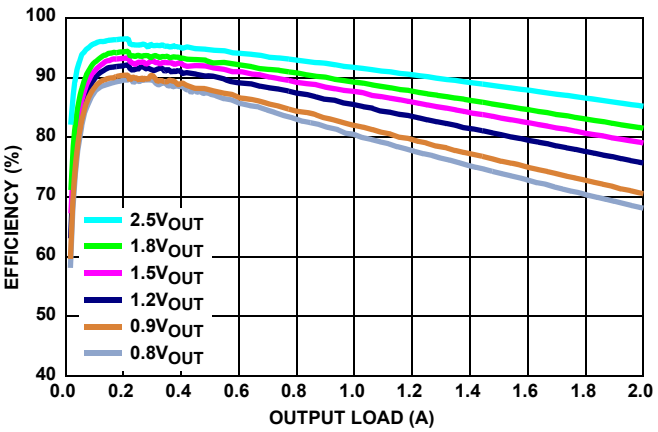


FIGURE 7. EFFICIENCY vs LOAD
F_{SW} = 1MHz, V_{IN} = 3.3V, MODE = PWM, T_A = +25°C

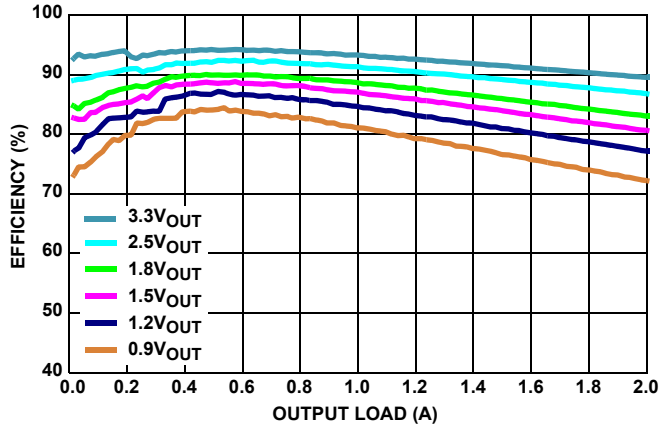


FIGURE 8. EFFICIENCY vs LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PFM, T_A = +25°C

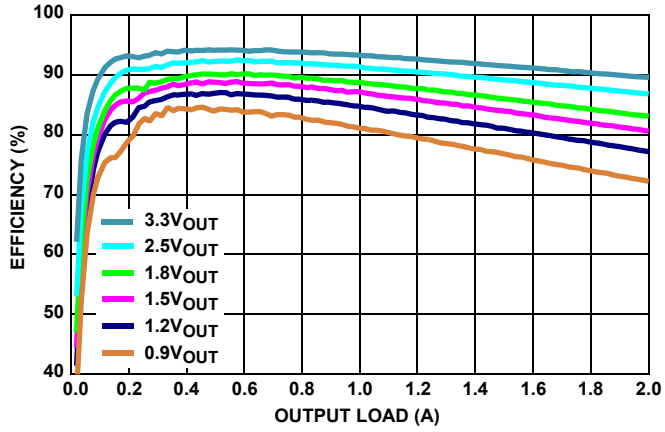


FIGURE 9. EFFICIENCY vs LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

Typical Performance Curves (Continued)

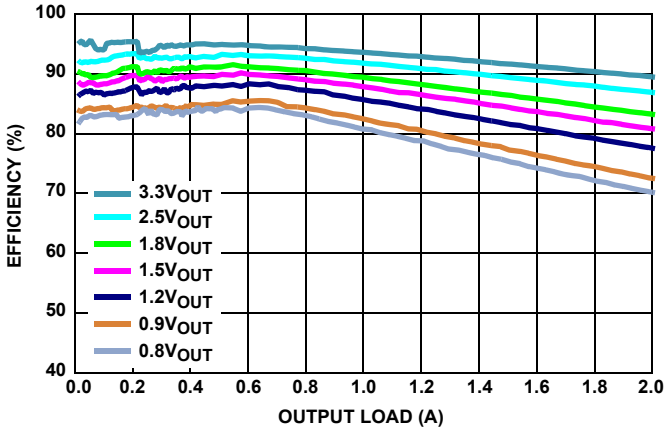


FIGURE 10. EFFICIENCY vs LOAD
F_{SW} = 1MHz, V_{IN} = 5V, MODE = PFM, T_A = +25°C

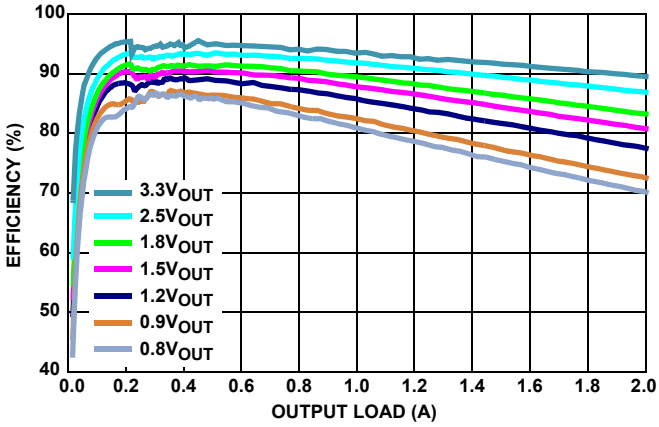


FIGURE 11. EFFICIENCY vs LOAD
F_{SW} = 1MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

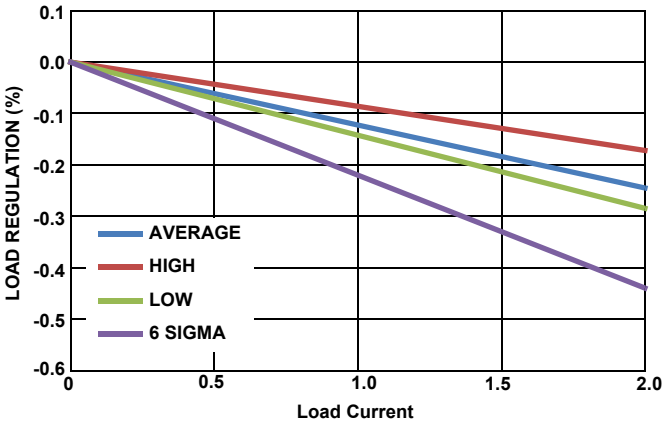


FIGURE 12. LOAD REGULATION, T_A = +105°C, 2.7V_{IN}, 0.6V_{OUT}, 1MHz

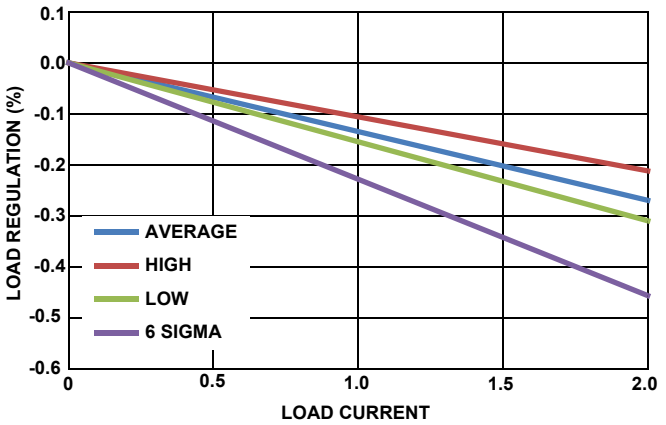


FIGURE 13. LOAD REGULATION, T_A = +105°C, 3.3V_{IN}, 0.6V_{OUT}, 1MHz

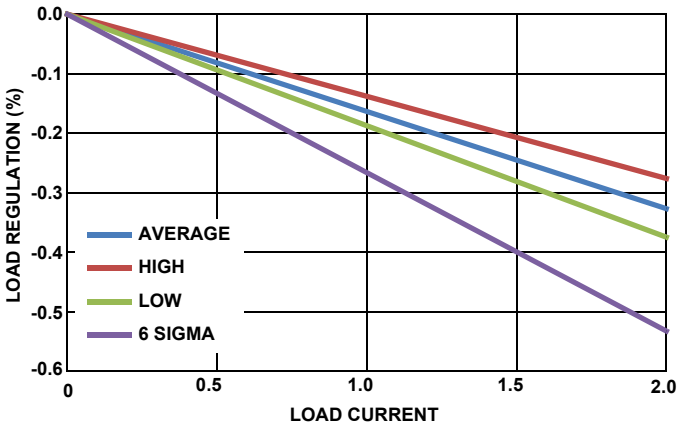


FIGURE 14. LOAD REGULATION, T_A = +105°, 5.5V_{IN}, 0.6V_{OUT}, 1MHz

Typical Performance Curves (Continued)

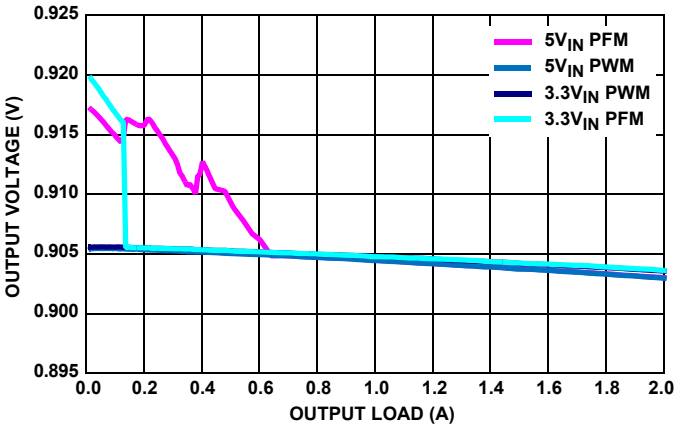


FIGURE 15. V_{OUT} REGULATION vs LOAD, F_{SW} = 2MHz, V_{OUT} = 0.9V, T_A = +25°C

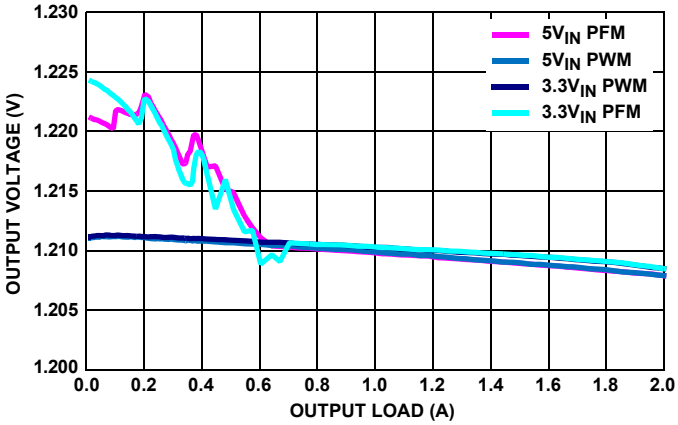


FIGURE 16. V_{OUT} REGULATION vs LOAD, F_{SW} = 2MHz, V_{OUT} = 1.2V, T_A = +25°C

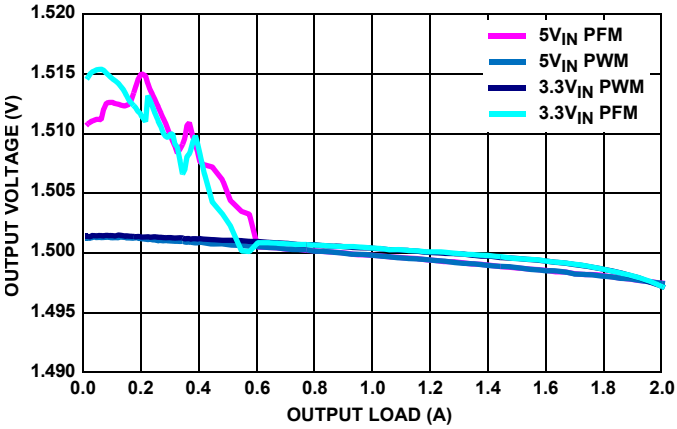


FIGURE 17. V_{OUT} REGULATION vs LOAD, F_{SW} = 2MHz, V_{OUT} = 1.5V, T_A = +25°C

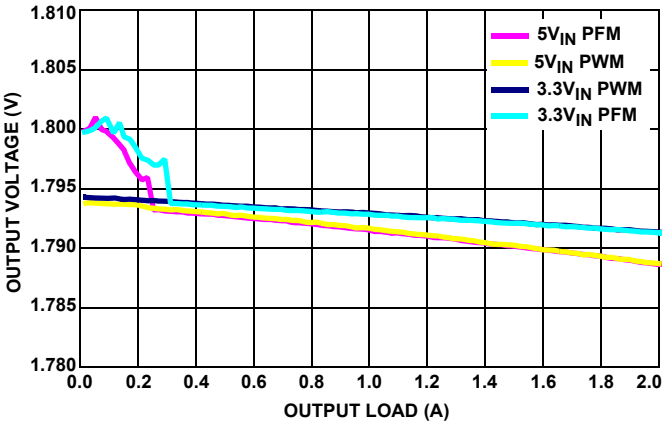


FIGURE 18. V_{OUT} REGULATION vs LOAD, F_{SW} = 2MHz, V_{OUT} = 1.8V, T_A = +25°C

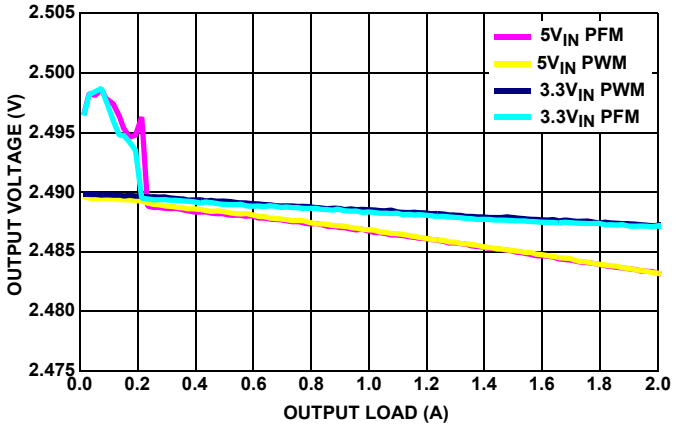


FIGURE 19. V_{OUT} REGULATION vs LOAD, F_{SW} = 2MHz, V_{OUT} = 2.5V, T_A = +25°C

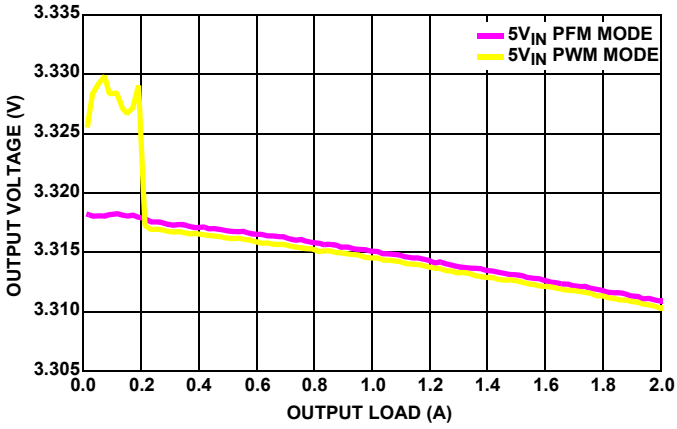


FIGURE 20. V_{OUT} REGULATION vs LOAD, F_{SW} = 2MHz, V_{OUT} = 3.3V, T_A = +25°C

Typical Performance Curves (Continued)

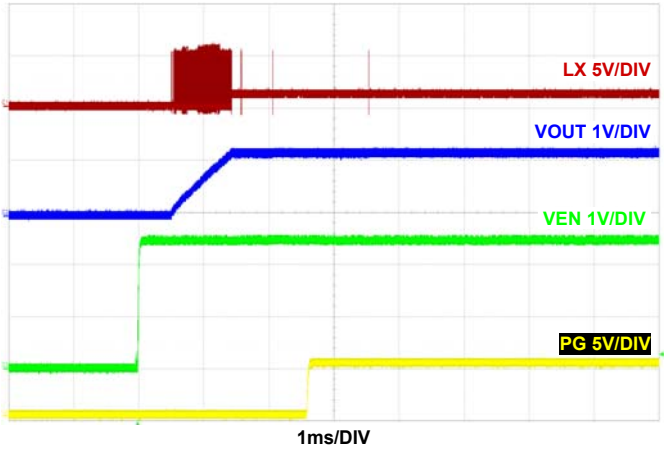


FIGURE 21. START-UP AT NO LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PFM, T_A = +25°C

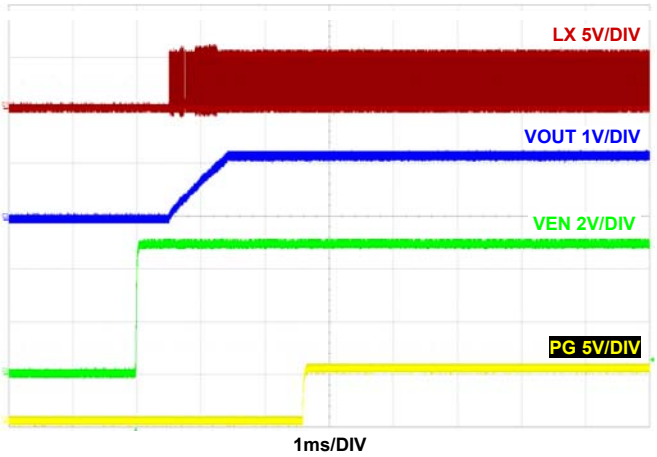


FIGURE 22. START-UP AT NO LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

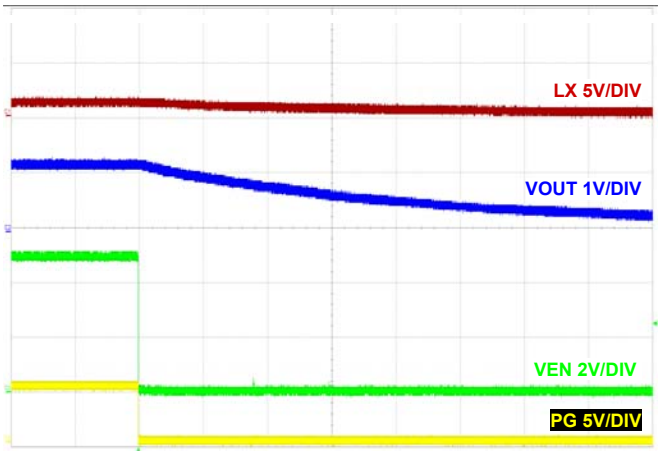


FIGURE 23. SHUTDOWN AT NO LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PFM, T_A = +25°C

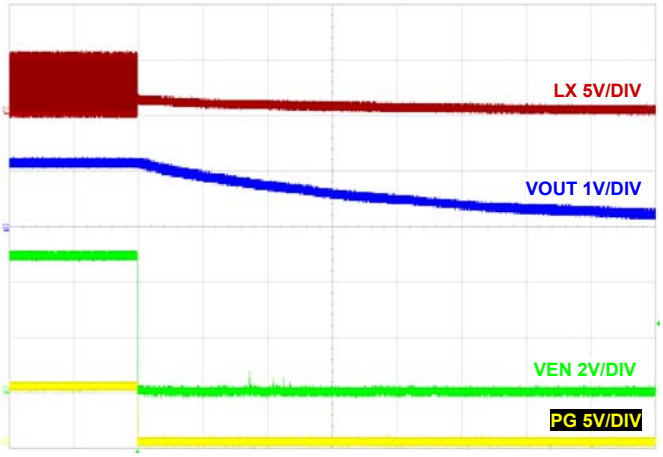


FIGURE 24. SHUTDOWN AT NO LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

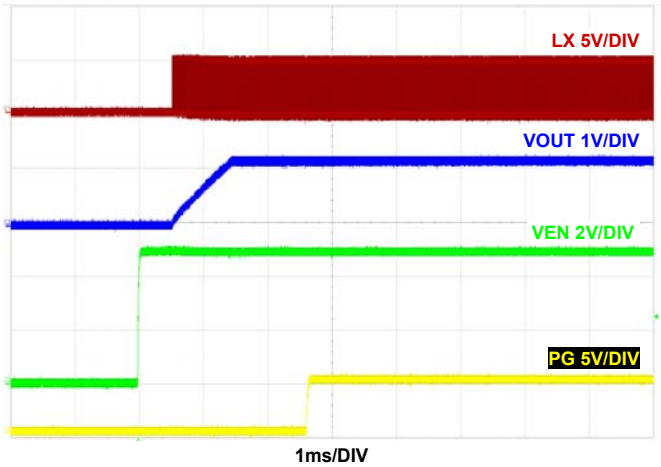


FIGURE 25. START-UP AT 2A LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

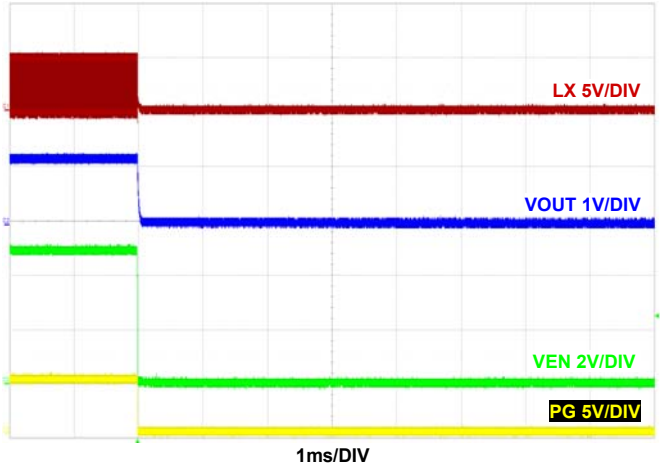


FIGURE 26. SHUTDOWN AT 2A LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

Typical Performance Curves (Continued)

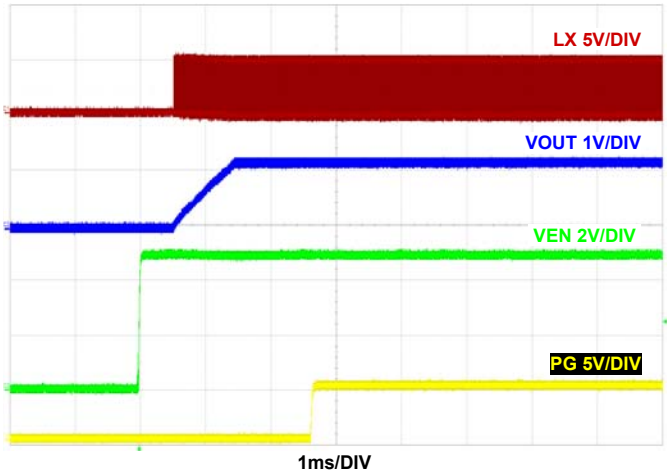


FIGURE 27. START-UP AT 2A LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PFM, T_A = +25°C

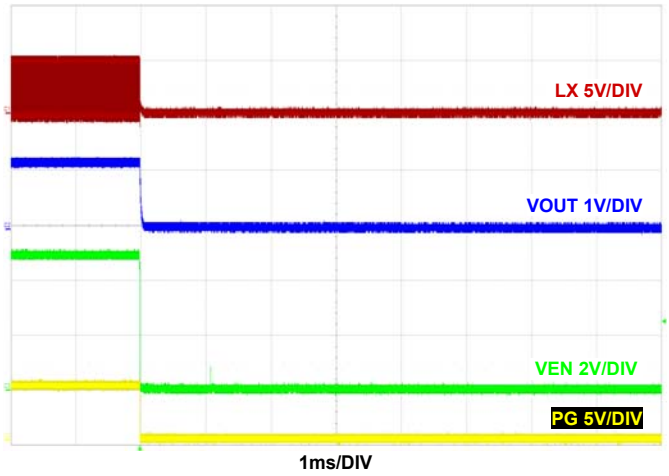


FIGURE 28. SHUTDOWN AT 2A LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PFM, T_A = +25°C

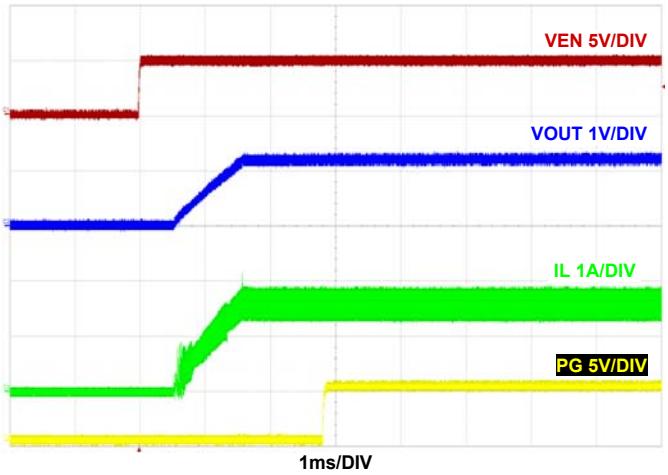


FIGURE 29. START-UP AT 1.5A LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

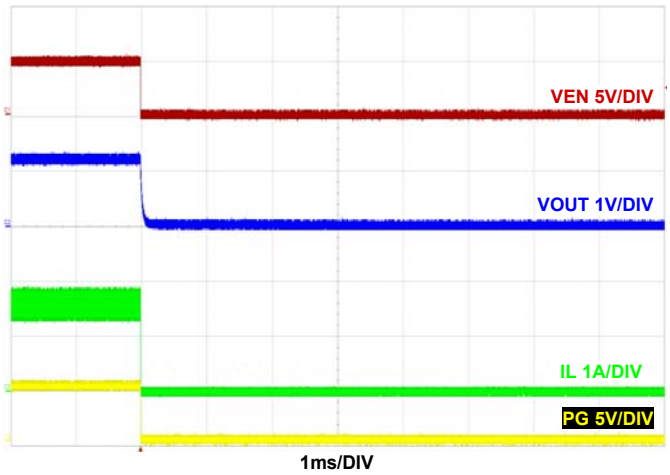


FIGURE 30. SHUTDOWN AT 1.5A LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

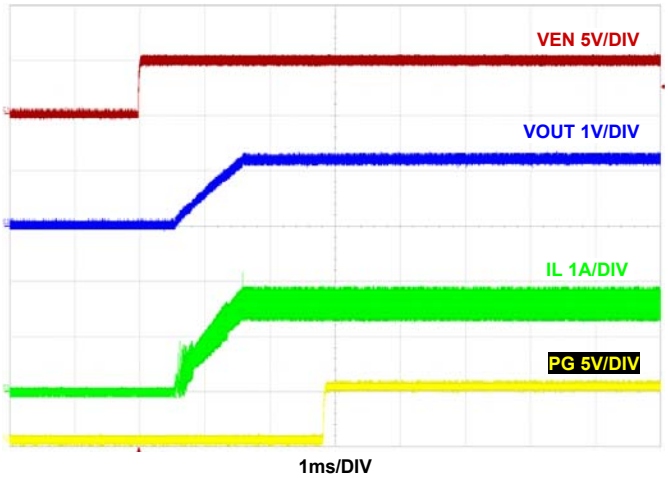


FIGURE 31. START-UP AT 1.5A LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PFM, T_A = +25°C

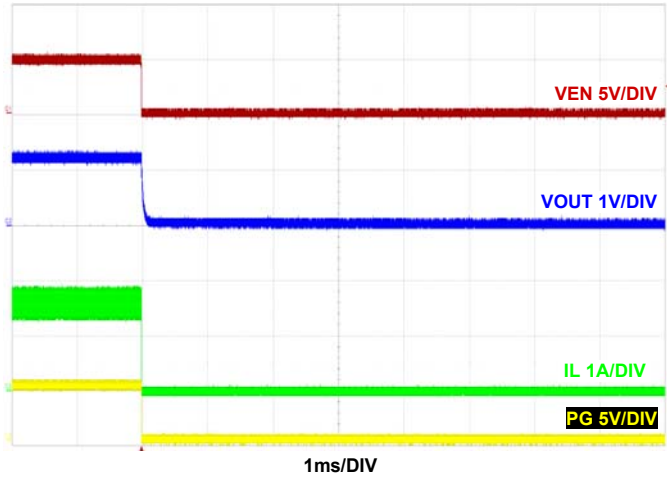


FIGURE 32. SHUTDOWN AT 1.5A LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PFM, T_A = +25°C

Typical Performance Curves (Continued)

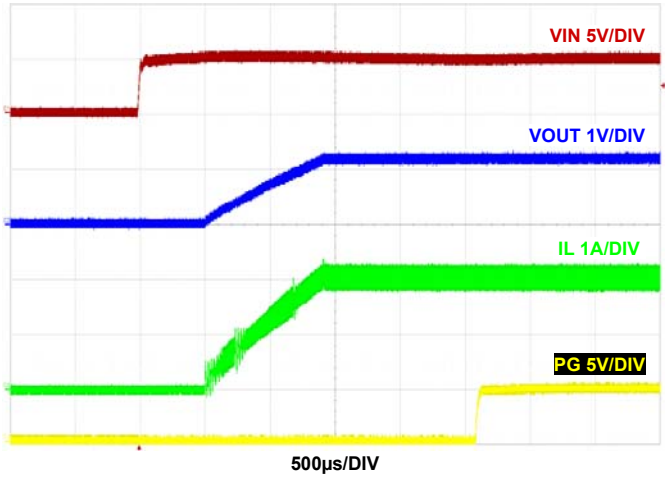


FIGURE 33. START-UP V_{IN} AT 2A LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PFM, T_A = +25°C

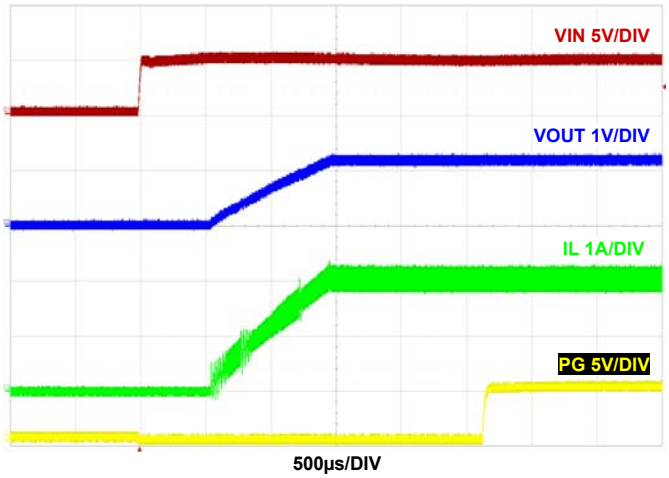


FIGURE 34. START-UP V_{IN} AT 2A LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

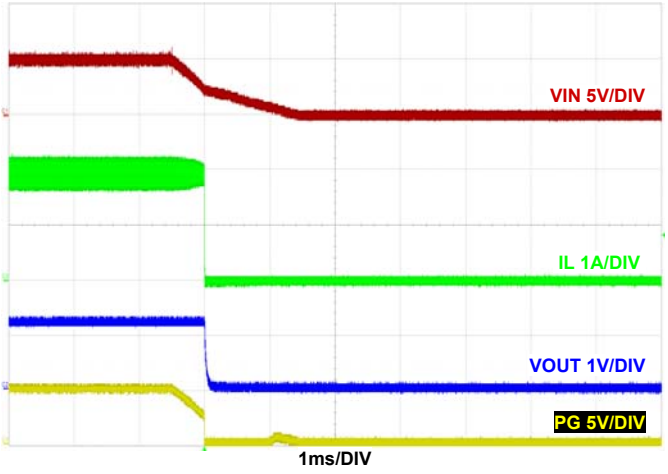


FIGURE 35. SHUTDOWN V_{IN} AT 2A LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PFM, T_A = +25°C

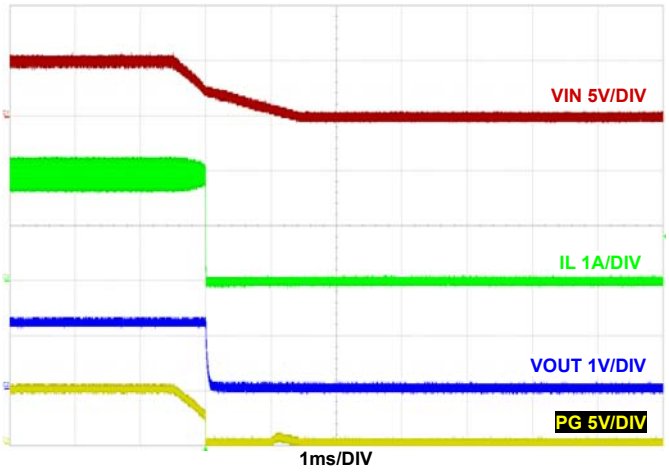


FIGURE 36. SHUTDOWN V_{IN} AT 2A LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

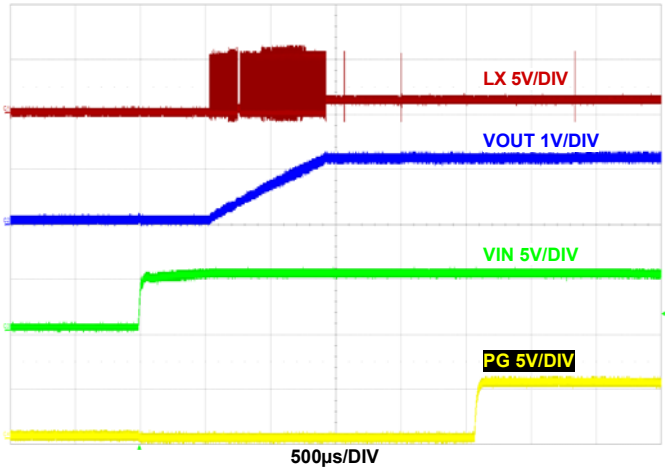


FIGURE 37. START-UP V_{IN} AT NO LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PFM, T_A = +25°C

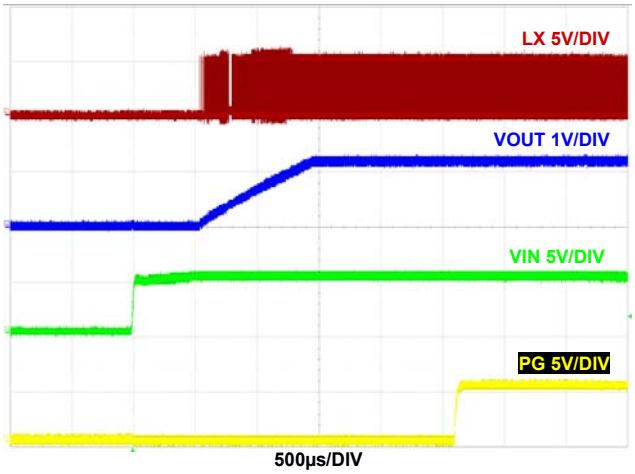


FIGURE 38. START-UP V_{IN} AT NO LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PFM, T_A = +25°C

Typical Performance Curves (Continued)

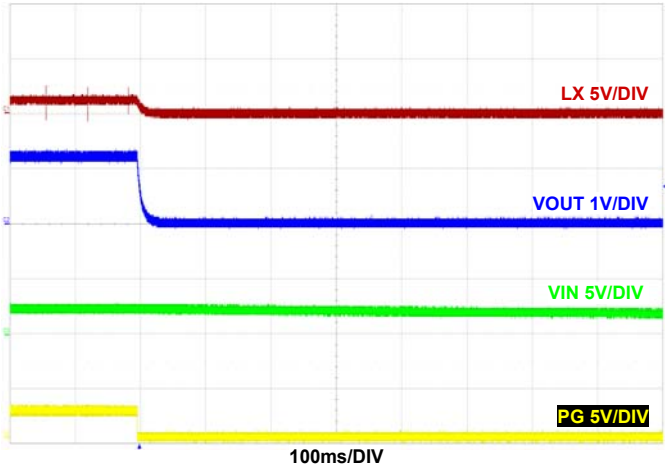


FIGURE 39. SHUTDOWN V_{IN} AT NO LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PFM, T_A = +25°C

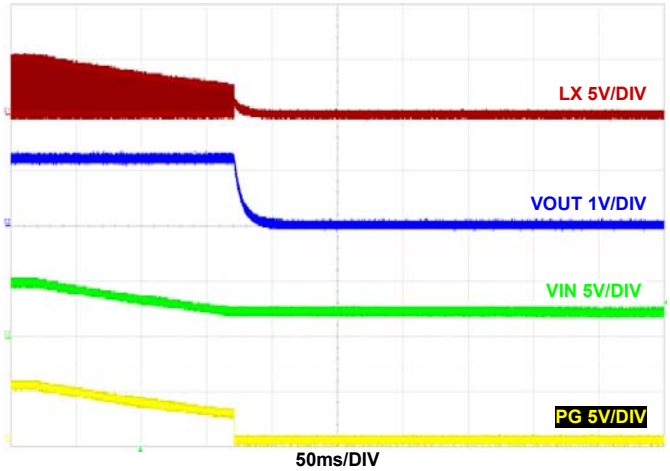


FIGURE 40. SHUTDOWN V_{IN} AT NO LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

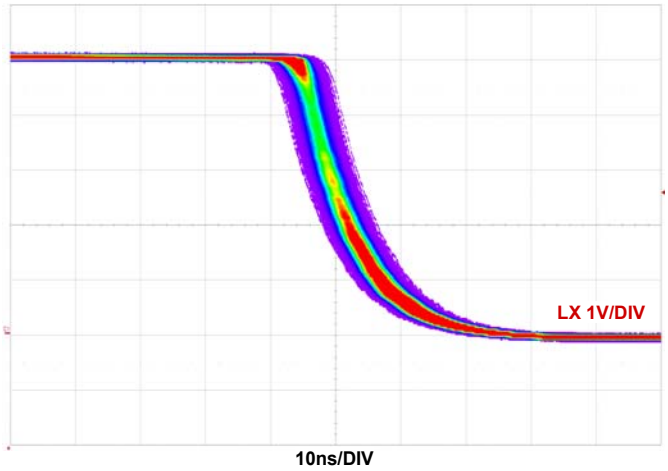


FIGURE 41. JITTER AT NO LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

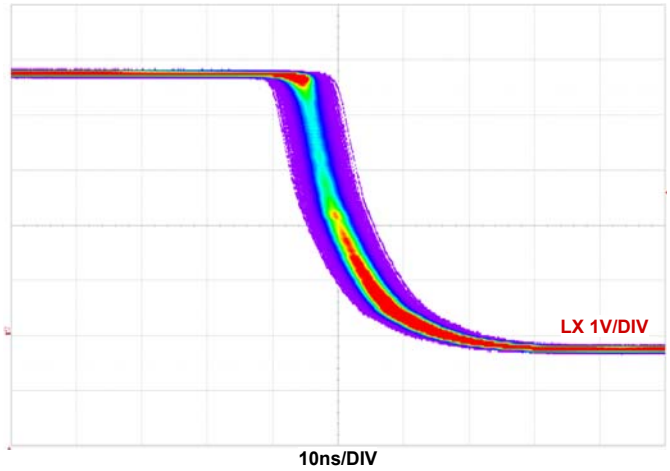


FIGURE 42. JITTER AT FULL LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

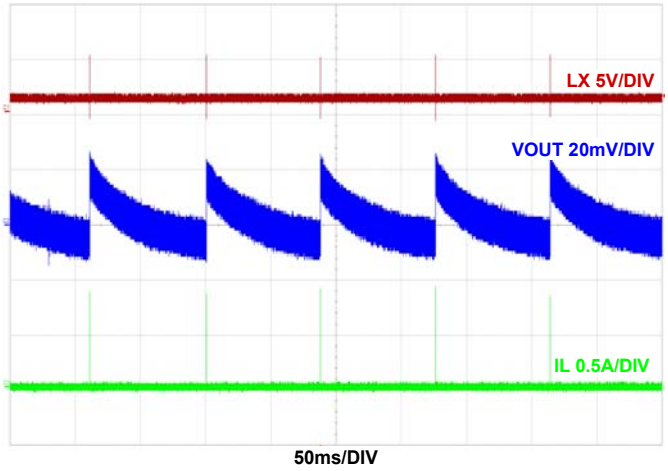


FIGURE 43. STEADY STATE AT NO LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PFM, T_A = +25°C

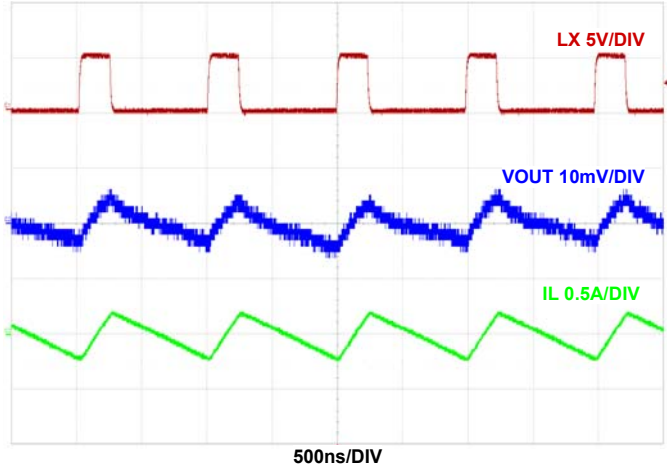


FIGURE 44. STEADY STATE AT NO LOAD
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

Typical Performance Curves (Continued)

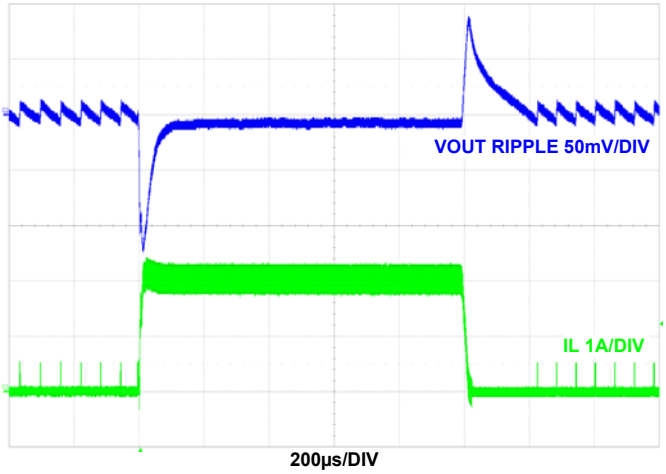


FIGURE 45. LOAD TRANSIENT
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PFM, T_A = +25°C

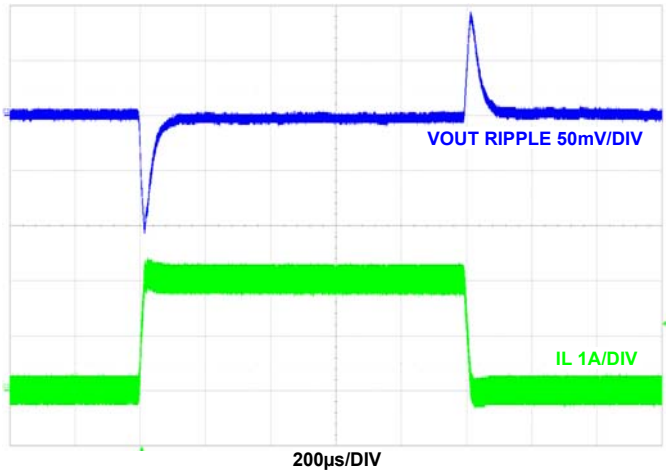


FIGURE 46. LOAD TRANSIENT
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

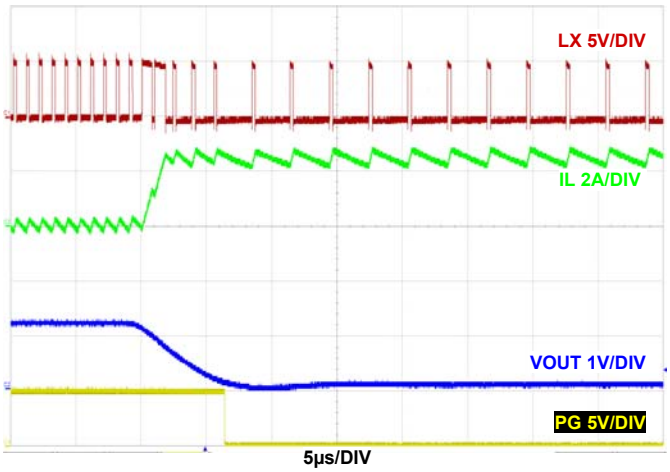


FIGURE 47. OUTPUT SHORT-CIRCUIT
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PFM, T_A = +25°C

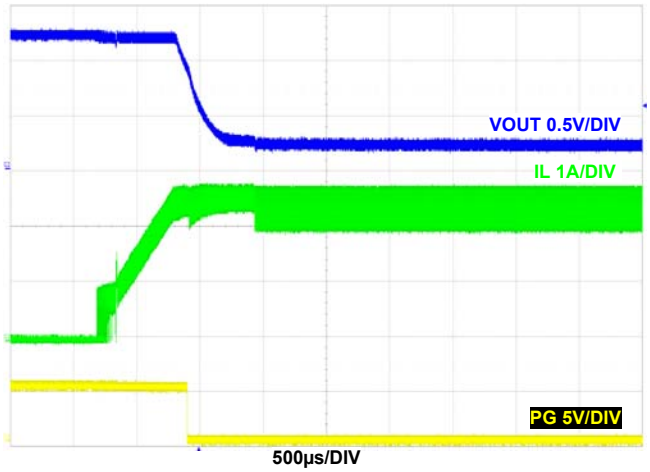


FIGURE 48. OVERCURRENT PROTECTION
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

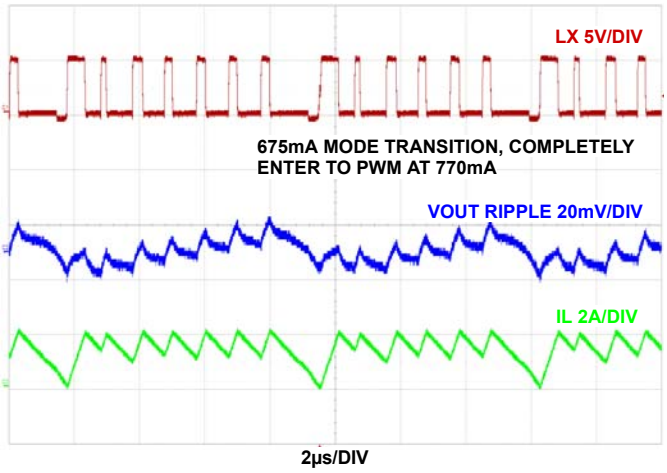


FIGURE 49. PFM TO PWM TRANSITION
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PFM, T_A = +25°C

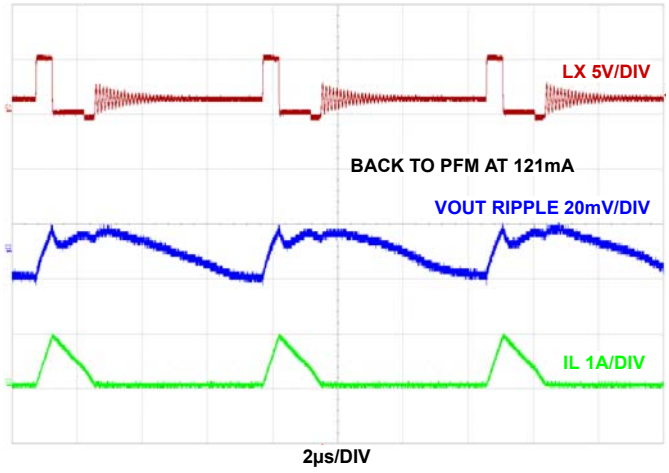


FIGURE 50. PWM TO PFM TRANSITION
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +25°C

Typical Performance Curves (Continued)

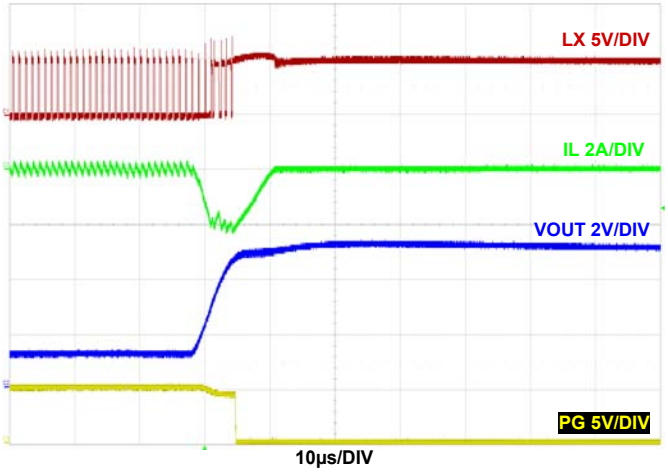


FIGURE 51. OVERVOLTAGE PROTECTION
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PFM, T_A = +25°C

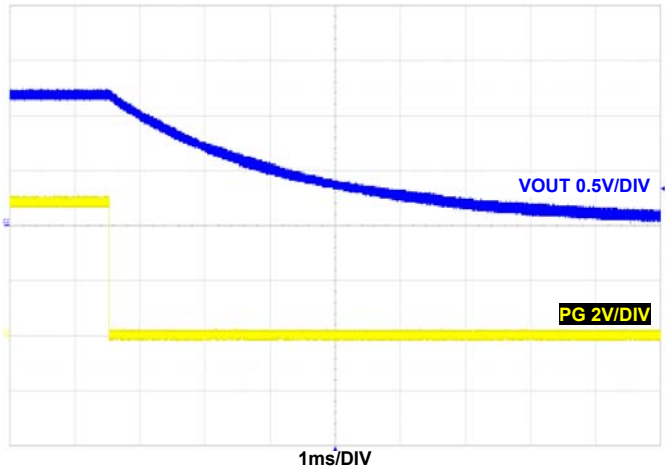


FIGURE 52. OVER-TEMPERATURE PROTECTION
F_{SW} = 2MHz, V_{IN} = 5V, MODE = PWM, T_A = +163°C

Theory of Operation

The device is a step-down switching regulator optimized for battery powered applications. It operates at high switching frequency (1MHz or 2MHz) which enables the use of smaller inductors resulting in small form factor, while also providing excellent efficiency. Further, at light loads while in PFM mode, the regulator reduces the switching frequency, thereby minimizing the switching loss and maximizing battery life. The quiescent current when the output is not loaded is typically only 35µA. The supply current is typically only 5µA when the regulator is shut down.

PWM Control Scheme

Pulling the MODE pin HI (>2.5V) forces the converter into PWM mode, regardless of output current. The device employs the current-mode pulse-width modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. Page 5 shows the “Functional Block Diagram”. The current loop consists of the oscillator, the PWM comparator, current sensing circuit and the slope compensation for the current loop stability. The slope compensation is 900mV/Ts, which changes with frequency. The gain for the current sensing circuit is typically 300mV/A. The control reference for the current loops comes from the error amplifier's (EAMP) output.

The PWM operation is initialized by the clock from the oscillator. The P-Channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier CSA and the slope compensation reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-FET and turn on the N-Channel MOSFET. The N-FET stays on until the end of the PWM cycle. Figure 53 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the slope compensation ramp and the current-sense amplifier’s CSA output.

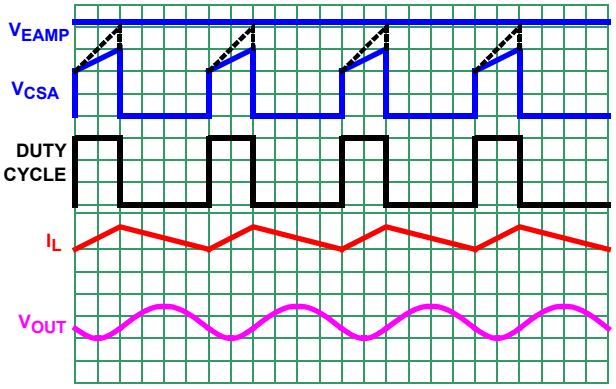


FIGURE 53. PWM OPERATION WAVEFORMS

The output voltage is regulated by controlling the V_{EAMP} voltage to the current loop. The bandgap circuit outputs a 0.6V reference voltage to the voltage loop. The feedback signal comes from the VFB pin. The soft-start block only affects the operation during the start-up and will be discussed separately. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 27pF and 200kΩ RC network. The maximum EAMP voltage output is precisely clamped to 1.6V.

PFM Mode

Pulling the MODE pin LO (<0.4V) forces the converter into PFM mode. The device enters a pulse-skipping mode at light load to minimize the switching loss by reducing the switching frequency. Figure 54 illustrates the skip-mode operation. A zero-cross sensing circuit shown in Figure 54 monitors the N-FET current for zero crossing. When 16 consecutive cycles of the inductor current crossing zero are detected, the regulator enters the skip mode. During the eight detecting cycles, the current in the inductor is allowed to become negative. The counter is reset to zero when the current in any cycle does not cross zero.

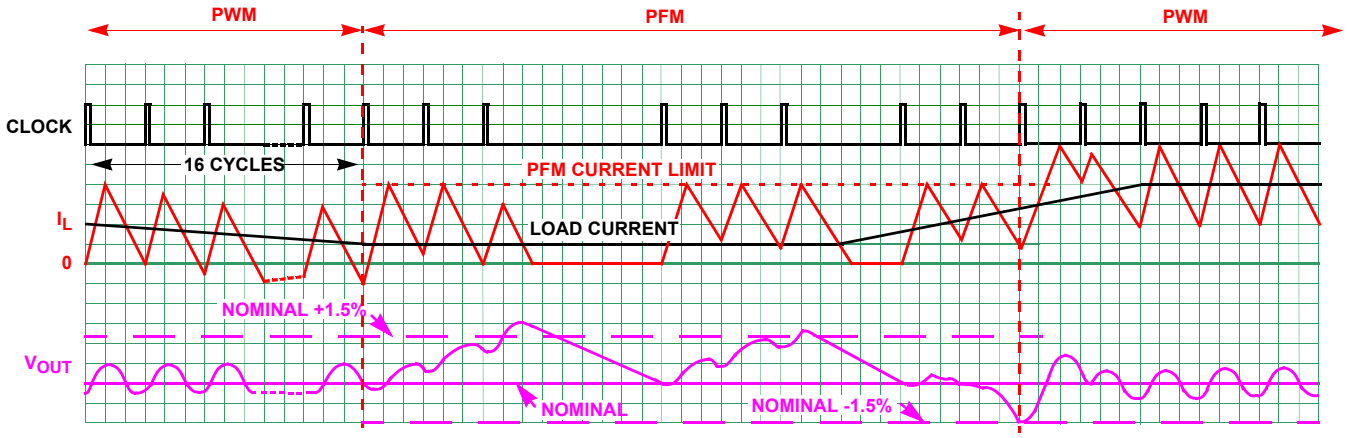


FIGURE 54. SKIP MODE OPERATION WAVEFORMS

Once the skip mode is entered, the pulse modulation starts being controlled by the SKIP comparator shown in the “Functional Block Diagram” on page 5. Each pulse cycle is still synchronized by the PWM clock. The P-FET is turned on at the clock's rising edge and turned off when the output is higher than 1.5% of the nominal regulation or when its current reaches the peak Skip current limit value. Then the inductor current is discharging to 0A and stays at zero. The internal clock is disabled. The output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the P-FET will be turned on again at the rising edge of the internal clock as it repeats the previous operations.

The regulator resumes normal PWM mode operation when the output voltage drops 1.5% below the nominal voltage.

Overcurrent Protection

The overcurrent protection is realized by monitoring the CSA output with the OCP comparator, as shown in the “Functional Block Diagram” on page 5. The current sensing circuit has a gain of 300mV/A, from the P-FET current to the CSA output. When the CSA output reaches a threshold, the OCP comparator is tripped to turn off the P-FET immediately. The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFET.

Upon detection of overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle. If the overcurrent condition goes away, the output will resume back into regulation point after the hiccup mode expires.

Short-Circuit Protection

The short-circuit protection (SCP) comparator monitors the VFB pin voltage for output short-circuit protection. When the VFB is lower than 0.3V, the SCP comparator forces the PWM oscillator frequency to drop to 1/3 of the normal operation value. This comparator is effective during start-up or an output short-circuit event.

Negative Current Protection

Similar to the overcurrent, the negative current protection is realized by monitoring the current across the low-side N-FET, as shown in the “Functional Block Diagram” on page 5. When the valley point of the inductor current reaches -1.5A for 2 consecutive cycles, both P-FET and N-FET shut off. The 100Ω in parallel to the N-FET will activate discharging the output into regulation. The control will begin to switch when output is within regulation. The regulator will be in PFM for 20µs before switching to PWM if necessary.

PG

PG is an output of a window comparator that continuously monitors the buck regulator output voltage. PG is actively held low when EN is low and during the buck regulator soft-start period. After 1ms delay of the soft-start period, PG becomes high impedance as long as the output voltage is within nominal regulation voltage set by VFB. When VFB drops 15% below or raises 15% above the nominal regulation voltage, the device pulls PG low. Any fault condition forces PG low until the fault condition is cleared by attempts to soft-start. There is an internal 5MΩ pull-up resistor to fit most applications. An external resistor can be added from PG to VIN for more pull-up strength.

UVLO

When the input voltage is below the undervoltage lock-out (UVLO) threshold, the regulator is disabled.

Enable, Disable, and Soft Start-Up

After the VIN pin exceeds its rising POR trip point (nominal 2.7V), the device begins operation. If the EN pin is held low externally, nothing happens until this pin is released. Once the EN is released and above the logic threshold, the internal default soft-start time is 1ms.

Discharge Mode (Soft-Stop)

When a transition to shutdown mode occurs or the VIN UVLO is set, the outputs discharge to GND through an internal 100Ω switch.

100% Duty Cycle (1MHz Version)

The device features 100% duty cycle operation to maximize the battery life. When the battery voltage drops to a level that the device can no longer maintain the regulation at the output, the regulator completely turns on the P-FET. The maximum dropout voltage under the 100% duty-cycle operation is the product of the load current and the ON-resistance of the P-FET.

Thermal Shut-Down

The device has built-in thermal protection. When the internal temperature reaches +150°C, the regulator is completely shut down. As the temperature drops to +125°C, the device resumes operation by stepping through the soft-start.

Applications Information

Output Inductor and Capacitor Selection

To consider steady state and transient operations, ISL8002A/ISL80019A typically requires a 1.2µH and ISL8002/ISL80019 typically requires a 2.2µH output inductor. Higher or lower inductor value can be used to optimize the total converter system performance. For example, for higher output voltage 3.3V application, in order to decrease the inductor ripple current and output voltage ripple, the output inductor value can be increased. It is recommended to set the inductor ripple current to be approximately 30% of the maximum output current for optimized performance. The inductor ripple current can be expressed as shown in Equation 2:

$$\Delta I = \frac{V_O \bullet \left(1 - \frac{V_O}{V_{IN}}\right)}{L \bullet F_{SW}} \quad \text{(EQ. 2)}$$

The inductor's saturation current rating needs to be at least larger than the peak current.

The device uses internal compensation network and the output capacitor value is dependent on the output voltage. The ceramic capacitor is recommended to be X5R or X7R.

Output Voltage Selection

The output voltage of the regulator can be programmed via an external resistor divider that is used to scale the output voltage relative to the internal reference voltage and feed it back to the inverting input of the error amplifier. Refer to Figure 35.

The output voltage programming resistor, R_2, will depend on the value chosen for the feedback resistor and the desired output voltage of the regulator. The value for the feedback resistor is typically between 10kΩ and 100kΩ, as shown in Equation 3.

$$R_1 = R_2\left(\frac{V_O}{VFB} - 1\right) \quad \text{(EQ. 3)}$$

If the output voltage desired is 0.6V, then R_2 is left unpopulated and R_1 is shorted. There is a leakage current from VIN to LX. It is recommended to preload the output with 10µA minimum. For better performance, add 22pF in parallel with R_1. Check loop analysis before use in application.

Input Capacitor Selection

The main functions for the input capacitor are to provide decoupling of the parasitic inductance and to provide filtering function to prevent the switching current flowing back to the battery rail. At least two 22µF X5R or X7R ceramic capacitors are a good starting point for the input capacitor selection.

Output Capacitor Selection

An output capacitor is required to filter the inductor current. Output ripple voltage and transient response are 2 critical factors when considering output capacitance choice. The current mode control loop allows for the usage of low ESR ceramic capacitors and thus smaller board layout. Electrolytic and polymer capacitors may also be used.

Additional consideration applies to ceramic capacitors. While they offer excellent overall performance and reliability, the actual in-circuit capacitance must be considered. Ceramic capacitors are rated using large peak-to-peak voltage swings and with no DC bias. In the DC/DC converter application, these conditions do not reflect reality. As a result, the actual capacitance may be considerably lower than the advertised value. Consult the manufacturers data sheet to determine the actual in-application capacitance. Most manufacturers publish capacitance vs DC bias so that this effect can be easily accommodated. The effects of AC voltage are not frequently published, but an assumption of ~20% further reduction will generally suffice. The result of these considerations can easily result in an effective capacitance 50% lower than the rated value. Nonetheless, they are a very good choice in many applications due to their reliability and extremely low ESR.

The following equations allow calculation of the required capacitance to meet a desired ripple voltage level. Additional capacitance may be used.

For the ceramic capacitors (low ESR) =

$$V_{OUTripple} = \frac{\Delta I}{8 * F_{SW} * C_{OUT}} \quad \text{(EQ. 4)}$$

where ΔI is the inductor's peak to peak ripple current, F_{SW} is the switching frequency and C_{OUT} is the output capacitor.

If using electrolytic capacitors then:

$$V_{OUTripple} = \Delta I * ESR \quad \text{(EQ. 5)}$$

Regarding transient response needs, a good starting point is to determine the allowable overshoot in V_{OUT} if the load is suddenly removed. In this case, energy stored in the inductor will be transferred to C_{OUT} causing its voltage to rise. After calculating capacitance required for both ripple and transient needs, choose the larger of the calculated values. The following equation determines the required output capacitor value in order to achieve a desired overshoot relative to the regulated voltage.

$$C_{OUT} = \frac{I_{OUT}^2 * L}{V_{OUT}^2 * (V_{OUTMAX}/V_{OUT})^2 - 1)} \quad \text{(EQ. 6)}$$

where V_{OUTMAX}/V_{OUT} is the relative maximum overshoot allowed during the removal of the load. For an overshoot of 5%, the equation becomes as follows:

$$C_{OUT} = \frac{I_{OUT}^2 * L}{V_{OUT}^2 * (1.05^2 - 1)} \quad \text{(EQ. 7)}$$

Loop Compensation Design

When COMP is not connected to VDD, the COMP pin is active for external loop compensation. The ISL8002, ISL8002A, ISL80019, and ISL80019A use constant frequency peak current mode control architecture to achieve fast loop transient response. An accurate current sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered as a state variable

since its peak current is constant, and the system becomes a single order system. It is much easier to design a type II compensator to stabilize the loop than to implement voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 55 shows the small signal model of the synchronous buck regulator.

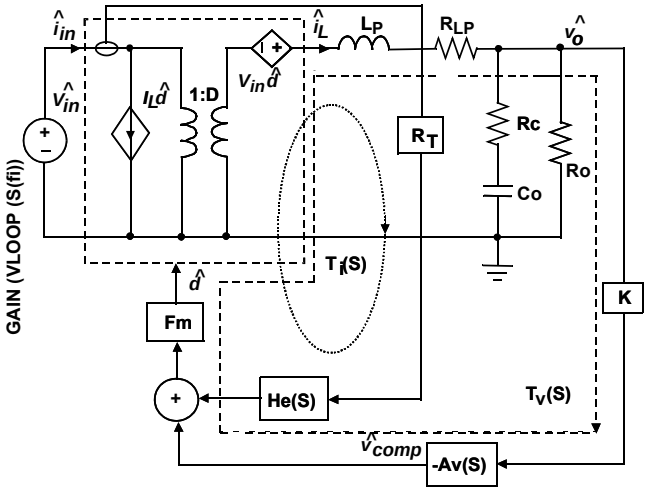


FIGURE 55. SMALL SIGNAL MODEL OF SYNCHRONOUS BUCK REGULATOR

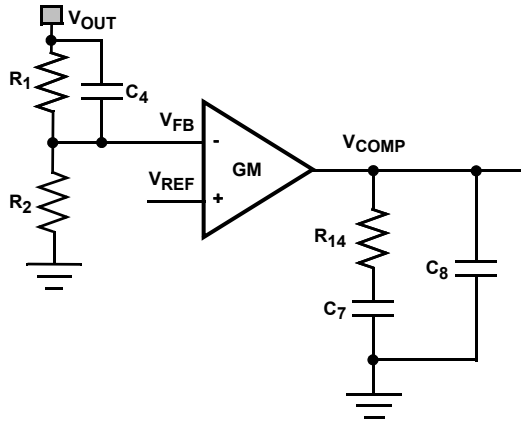


FIGURE 56. TYPE II COMPENSATOR

Figure 56 shows the type II compensator and its transfer function is expressed as Equation 8:

$$A_V(S) = \frac{\hat{v}_{comp}}{\hat{v}_{FB}} = \frac{GM \cdot R_2}{(C_7 + C_8)\cdot(R_1 + R_2)} \cdot \frac{\left(1 + \frac{S}{\omega_{cz1}}\right)\left(1 + \frac{S}{\omega_{cz2}}\right)}{S\left(1 + \frac{S}{\omega_{cp1}}\right)\left(1 + \frac{S}{\omega_{cp2}}\right)} \quad \text{(EQ. 8)}$$

where,

$$\omega_{cz1} = \frac{1}{R_{14}C_7},\ \omega_{cz2} = \frac{1}{R_1C_4},\ \omega_{cp1} = \frac{C_7 + C_8}{R_{14}C_7C_8},\ \omega_{cp2} = \frac{R_1 + R_2}{C_4R_1R_2}$$

COMPENSATOR DESIGN GOAL

- High DC gain
- Choose Loop bandwidth f_c less than 100kHz
- Gain margin: >10dB
- Phase margin: >50°

The compensator design procedure is as follows:

The loop gain at crossover frequency of f_c has unity gain. Therefore, the compensator resistance R_{14} is determined by Equation 9.

$$R_{14} = \frac{2\pi f_c V_o C_o R_t}{GM \cdot V_{FB}} = 26\times10^3 \cdot f_c V_o C_o \quad \text{(EQ. 9)}$$

Where GM is the trans-conductance of the voltage error amplifier.

Compensator capacitors C_7 and C_8 are then given by Equations 10 and 11.

$$C_7 = \frac{R_oC_o}{R_{14}} = \frac{V_oC_o}{I_oR_{14}} \quad \text{(EQ. 10)}$$

$$C_8 = \max\left(\frac{R_cC_o}{R_{14}}, \frac{1}{\pi f_s R_{14}}\right) \quad \text{(EQ. 11)}$$

An optional zero can boost the phase margin. ω_{CZ2} is a zero due to R_1 and C_4.

Put compensator zero 2 to 5 times f_c:

$$C_4 = \frac{1}{\pi f_c R_1} \quad \text{(EQ. 12)}$$

Example: V_{IN} = 5V, V_{OUT} = 1.8V, I_O = 2A, F_{SW} = 1MHz, R_1 = 200kΩ, R_2 = 100kΩ, C_{OUT} = 2x22µF/3mΩ, L = 2.2µH, f_c = 100kHz, then compensator resistance R_{14}:

$$R_{14} = 26\times10^3 \cdot 100kHz \cdot 1.8V \cdot 44\mu F = 205k\Omega \quad \text{(EQ. 13)}$$

Using the closest standard value for R_{14} value is fine (200kΩ).

$$C_7 = \frac{1.8V \cdot 44\mu F}{2A \cdot 200k\Omega} = 198pF \quad \text{(EQ. 14)}$$

$$C_8 = \max\left(\frac{3m\Omega \cdot 44\mu F}{200k\Omega}, \frac{1}{\pi \cdot 1MHz(200k\Omega)}\right) = (1pF, 2.3pF) \quad \text{(EQ. 15)}$$

The closest standard values for C_7 and C_8 are also fine. There is approximately 3pF parasitic capacitance from V_{COMP} to GND; Therefore, C_8 is optional. Use C_7 = 220pF and C_8 = OPEN.

$$C_4 = \frac{1}{\pi 100kHz \cdot 200k\Omega} = 16pF \quad \text{(EQ. 16)}$$

Use C_4 = 15pF. Note that C_4 may increase the loop bandwidth from previously estimated value. Figure 57 shows the simulated voltage loop gain. It is shown that it has 114kHz loop bandwidth with 52° phase margin and 10dB gain margin. It may be more desirable to achieve more phase margin. This can be accomplished by lowering R_{14} by 20% to 50%.

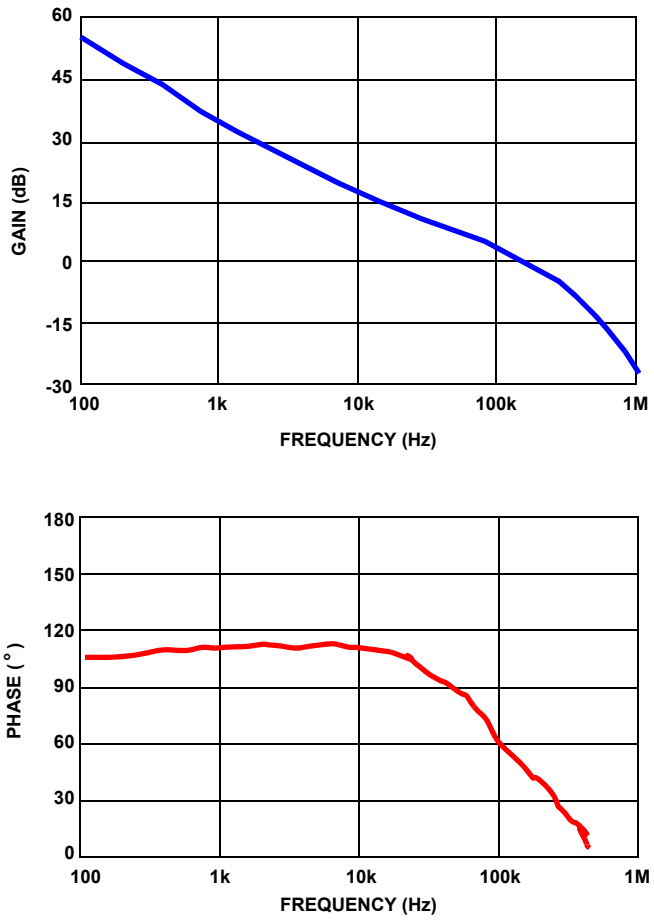


FIGURE 57. SIMULATED LOOP GAIN

Layout Considerations

The PCB layout is a very important converter design step to make sure the designed converter works well. The power loop is composed of the output inductor L's, the output capacitor C_{OUT}, the PHASE's pins, and the PGND pin. It is necessary to make the power loop as small as possible and the connecting traces among them should be direct, short and wide. The switching node of the converter, the PHASE pins, and the traces connected to the node are very noisy, so keep the voltage feedback trace away from these noisy traces. The input capacitor should be placed as closely as possible to the VIN pin and the ground of the input and output capacitors should be connected as closely as possible. The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for better EMI performance. It is recommended to add at least 4 vias ground connection within the pad for the best thermal relief.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
July 30, 2013	FN7888.2	Updated ordering information table on page 6. Added Figures 12, 13 and 14 to “Typical Performance Curves” on page 9. Electrical Specifications on page 7 under output regulation section removed duplicate of "TJ = -40°C to +125°C" from VFB Bias Current to in place Line Regulation.
June 13, 2013		Functional Block Diagram on page 5 - changed VFB to VREF Changed part number in ordering information on page 6 from ISL80019FRZ-T TO ISL80019FZ-T Changed on page 7 Recommend Operating Conditions the word "Ambient" to "Junction" Changed in Electrical Spec on page 7 conditions from TA -40 to +85 to TJ -40 to +125 VFB Bias Current under Output Regulation Test condition from 0.75V and TYP from 0.1 to 2.7V MIN -120 TYP 50 MAX 350 Type II Compensator graphic on page 20 - changed VFB to VREF
May 10, 2013		Pin Descriptions on page 4: EN section, changed pin rises from 0.6V to 1.4V.
January 7, 2013	FN7888.1	Initial release.

About Intersil

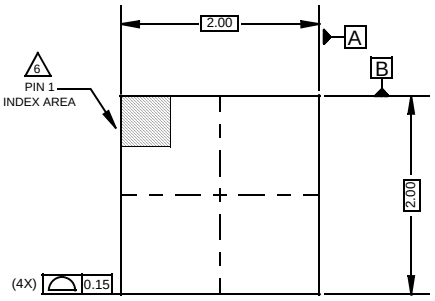
Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

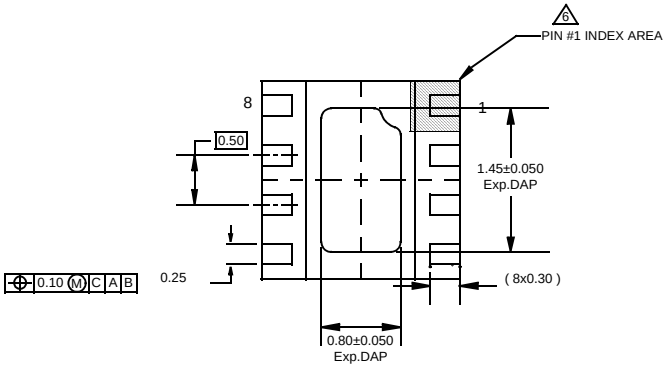
Package Outline Drawing

L8.2x2C

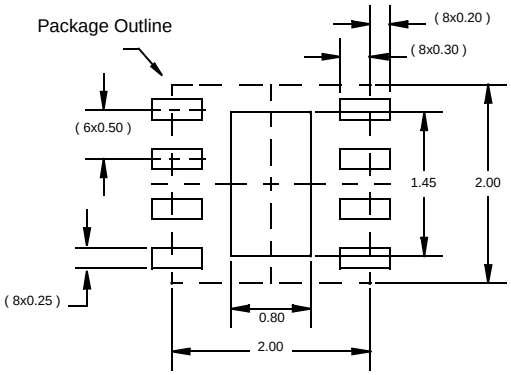
8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE (TDFN) WITH E-PAD
Rev 0, 07/08



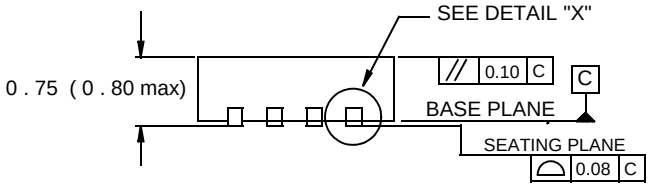
TOP VIEW



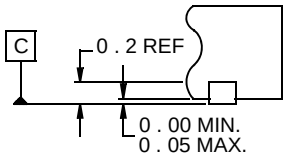
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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