cellergy Ltd

Super Capacitors To Improve Power Performance.

Low ESR
High Capacitance
Wide Range of Operating Temperatures
Wide Packaging Capability
Wide Footprint Selection
High Power
Safe
Environmentally Friendly RoHS Compliant

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Revision History

No.	Documentation	Check	Description of Revision	Approval	Date
1		Semion Simma	Soldering temperature changed from 245 °C to 360 °C.		20/07/08
2		Semion Simma	CLP serias are applied.		20/07/08
3		Semion Simma	Polarity signs are applied also different leads' length.		20/07/08
4		Semion Simma	CLP04P070L28 changed to CLP04P040L28		20/07/08
5		Semion Simma	Tolerance of ESR/Cap is added		20/11/08
6		Semion Simma	SC weights were added		24/05/09
7		Semion Simma	1.4V supercapacitors were added		04/06/09
8		Semion Simma	CLG05P008L12, CLG05P016L12 were added		17/06/09
9		Semion Simma	CLC03P012L12,CLC04P010L12 were added		17/09/09
10		Semion Simma	CLK,CLX, CLP were added, Temperature Cycling test was updated		16/11/09
11		Semion Simma	Leakage current changed for 12x12, 17x17 SC families		20/12/09
12		Semion Simma	CLX04P007L12 details were changed		29/12/09
13		Semion Simma	1) CLX04P007L12 height changed from 2.2 mm to 2.9mm 2) Packing weight and dimensions were added		7/2/10
14		Semion Simma	1) CLG01P030L12, CLG01P060L12, CLG01P060L17, CLG01P120L17 were added. 2) CLG01P150L28 and CLG01P300L12 parameters were changed.		21/3/10

Ordering Information

1	2	3	4	5	6
CLG	02	P	080	L	17

1_ Series Name

CLG : Standard
CLP : Low Profile (PRELIMINARY)
CLK : Extra Capacitance (PRELIMINARY)
CLC : Low Leakage (PRELIMINARY)
CLX : Low ESR (PRELIMINARY)

2_ Nominal Voltage:01 (1.4V); 02 (2.1V); 03 (3.5V); 04 (4.2V); 05 (5.5V); 06 (6.3V); 09 (9V); 12 (12V)

3_ Case Types: P - Prismatic

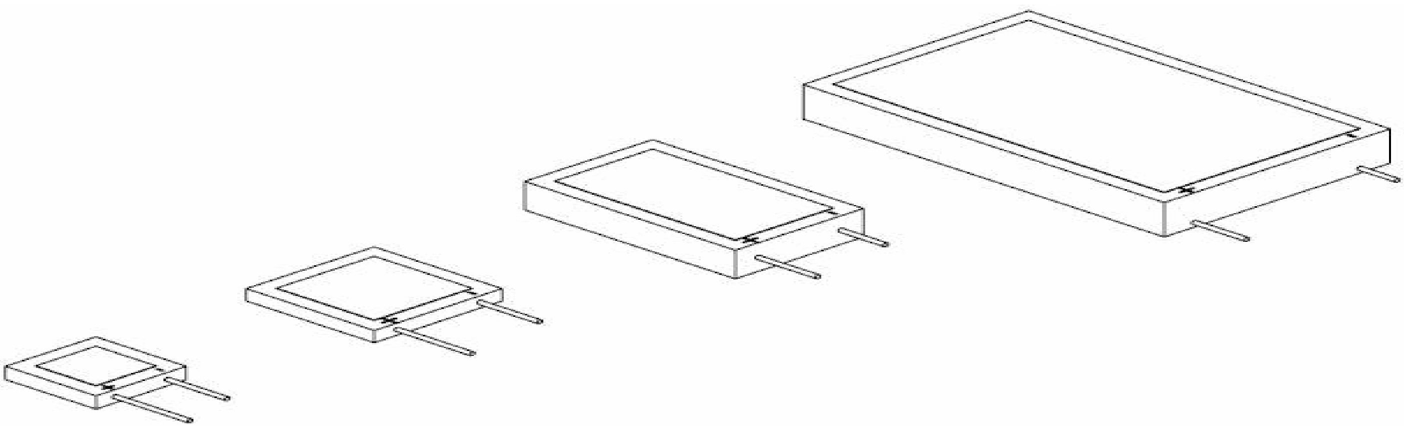
4_ Capacitance: 080 (80 mF)

5_ Leads: L-Trough Hole, F-Flat (PRELIMINARY)

6_ Case Size: 12 (12X12.5mm), 17(17x17.5 mm), 28(28x17.5mm), 48(48X30.5mm)

Product Schematics (by Case Size)

L12	L17	L28	L48



PRELIMINARY— **New prototype , not qualified yet**

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Line Card

Foot Print	P/N	V	ESR [mΩ]	Cap. [mF]	L.C[μA]	Length	Width [mm]	Height	Pitch	Weight [g]
12x12	CLG03P012L12	3.5	600	12	3	12	12.5	2.4	8.0	1.3
	CLG04P010L12	4.2	720	10	3	12	12.5	2.6	8.0	1.3
	CLG05P008L12	5.5	1000	8	3	12	12.5	3.1	8.0	
	CLG06P007L12	6.3	1200	7	3	12	12.5	3.4	8.0	1.6
	CLG03P025L12	3.5	300	25	6	12	12.5	3.4	8.0	1.6
	CLG04P020L12	4.2	360	20	6	12	12.5	3.9	8.0	1.6
	CLG05P016L12	5.5	500	16	6	12	12	4.8	8.0	
	CLG06P012L12	6.3	600	12	6	12	12.5	5.3	8.0	1.9
preliminary	CLX04P007L12	4.2	300	7	12	12	12.5	2.9	8.0	
preliminary	CLG01P030L12	1.4	240	30	3	12	12.5	1.7	8.0	
preliminary	CLG01P060L12	1.4	120	60	6	12	12.5	2.0	8.0	
preliminary	CLK01P080L12	1.4	240	80	3	12	12.5	1.7	8.0	
preliminary	CLK01P160L12	1.4	120	160	6	12	12.5	2.0	8.0	
preliminary	CLC03P012L12	3.5	1000	12	1	12	12.5	2.4	8.0	
preliminary	CLC04P010L12	4.2	1200	10	1	12	12.5	2.6	8.0	
17x17	CLG02P040L17	2.1	180	40	6	17	17.5		11.0	
	CLG03P025L17	3.5	300	25	6	17	17.5		11.0	
	CLG04P020L17	4.2	360	20	6	17	17.5		11.0	
	CLG05P015L17	5.5	560	15	6	17	17.5		11.0	
	CLG02P080L17	2.1	90	80	12	17	17.5	2.5	11.0	3.2
	CLG03P050L17	3.5	150	50	12	17	17.5	3.4	11.0	3.3
	CLG04P040L17	4.2	180	40	12	17	17.5	3.9	11.0	3.3
	CLG05P030L17	5.5	280	30	12	17	17.5	4.8	11.0	3.4
preliminary	CLG01P60L17	1.4	120	60	6	17	17.5	1.7	11.0	
preliminary	CLG01P120L17	1.4	60	120	12	17	17.5	2.0	11.0	

PRELIMINARY — New prototype , not qualified yet

Line Card

Foot Print	P/N	V	ESR [mΩ]	Cap. [mF]	L.C[μA]	Length	Width [mm]	Height	Pitch [mm]	Weight [g]
preliminary	CLP04P040L28	4.2	150	40	12	28	17.5	2.0	11.0	
preliminary	CLG01P150L28	1.4	50	150	10	28	17.5	1.7	11.0	
preliminary	CLG01P300L28	1.4	25	300	20	28	17.5	2.0	11.0	
28x17	CLG03P060L28	3.5	130	60	10	28	17.5	2.4	11.0	4.3
	CLG04P050L28	4.2	150	50	10	28	17.5	2.6	11.0	4.5
	CLG05P040L28	5.5	200	40	10	28	17.5	3.1	11.0	4.8
	CLG06P035L28	6.3	230	35	10	28	17.5	3.4	11.0	5.3
	CLG12P015L28	12	445	15	10	28	17.5	5.4	11.0	6.4
	CLG03P120L28	3.5	65	120	20	28	17.5	3.4	11.0	5.3
	CLG04P100L28	4.2	75	100	20	28	17.5	3.9	11.0	5.4
	CLG05P080L28	5.5	100	80	20	28	17.5	4.8	11.0	5.7
	CLG06P070L28	6.3	115	70	20	28	17.5	5.4	11.0	6.3
48x30	CLG02P700L48	2.1	11	700	65	48	30.5	2.5	22.3	18.5
	CLG03P420L48	3.5	20	420	65	48	30.5	3.4	22.3	19.5
	CLG04P350L48	4.2	25	350	65	48	30.5	3.9	22.3	20.0
	CLG05P280L48	5.5	30	280	65	48	30.5	4.8	22.3	21.2
	CLG06P245L48	6.3	35	245	65	48	30.5	5.3	22.3	21.7
	CLG09P165L48	9	50	165	65	48	30.5	7.2	22.3	25.2
	CLG12P120L48	12	70	120	65	48	30.5	9.2	22.3	31.1

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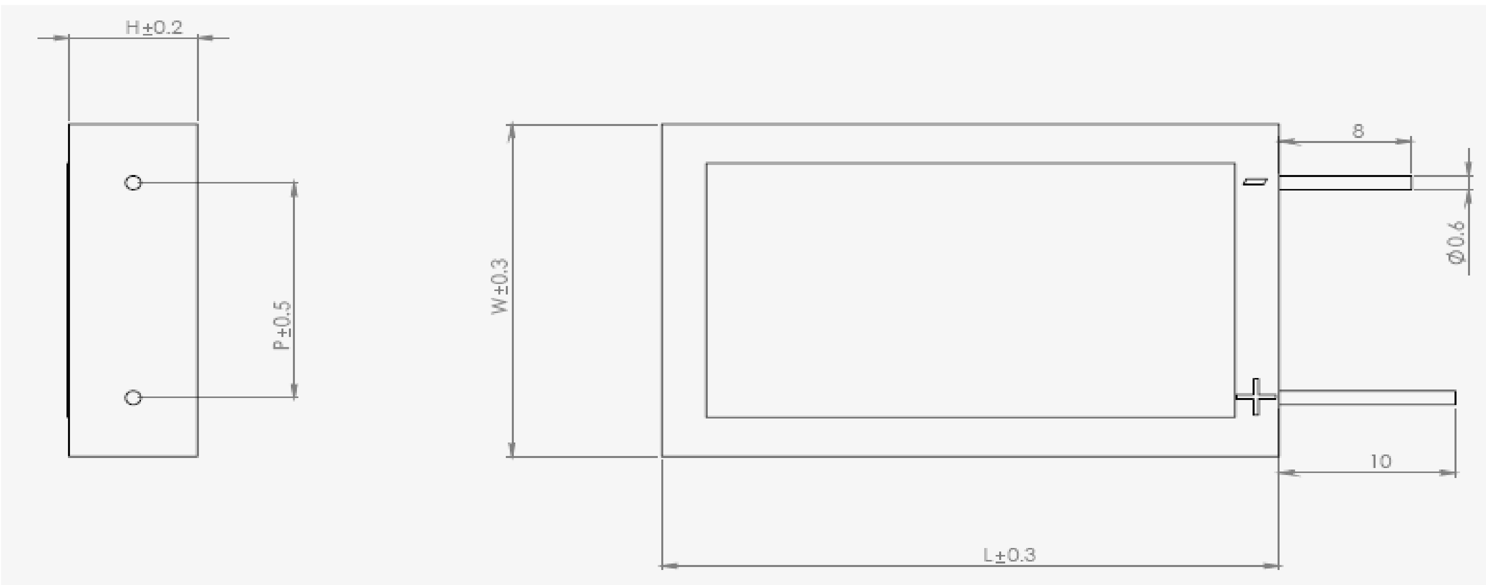
Electrical Rating Table

CLG Ratings	Nominal	Minimum	Maximum
Capacitance tolerance		-20%	+80%
Operating Temp.	25°C	-40°C	+70°C
Storage Temp.	25°C	-40°C	+70°C
Surge voltage			+25%
ESR change with Temp.	150% of nominal @ 70°C		200% of nominal @-20°C
Pulse current			No limit

Mechanical Dimensions



L, W, H – appear at LINE CARD (Page 5) for each Supercapacitor configuration.

Cellergy's products typically do not have polarity as the electrodes are symmetrical.

Voltage is applied to the capacitors during Cellergy's qualification tests and the capacitor may be sent to the customer with residual voltages remaining after shorting the cells. Accordingly plus / minus signs are designated in accordance with Cellergy Q&R procedures.

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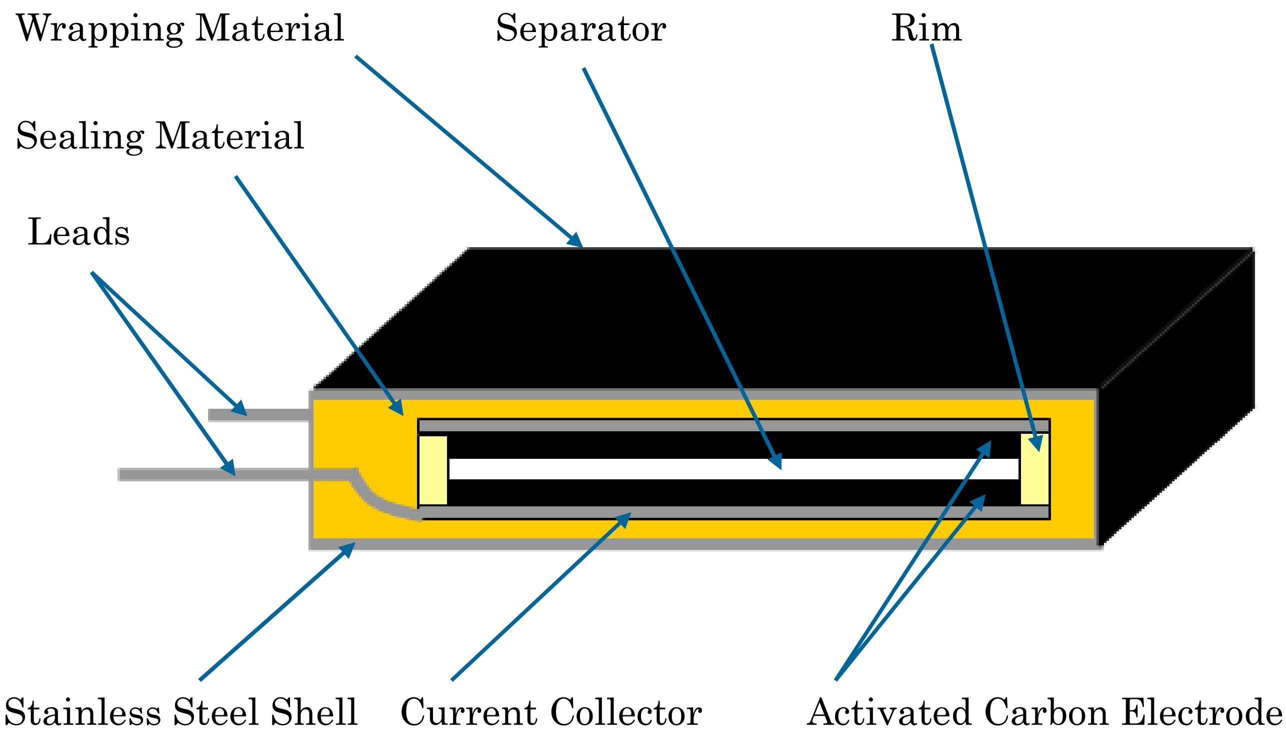
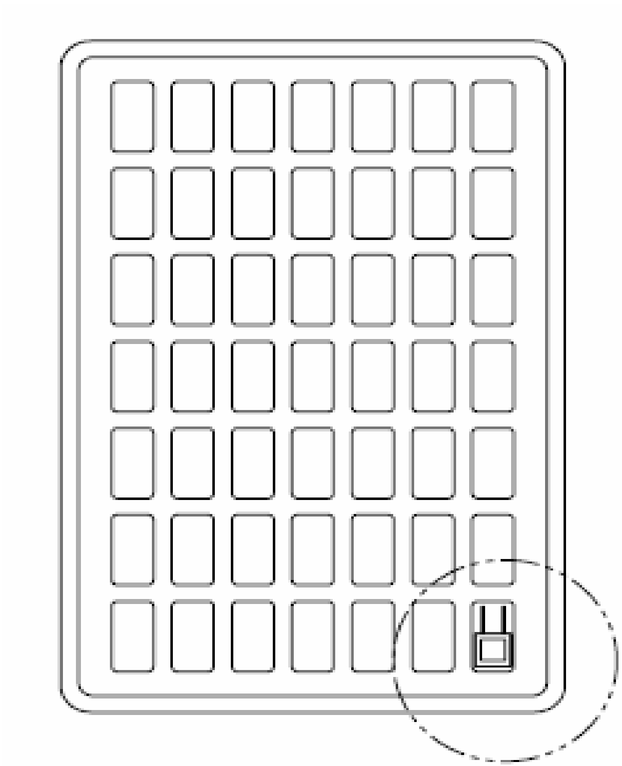
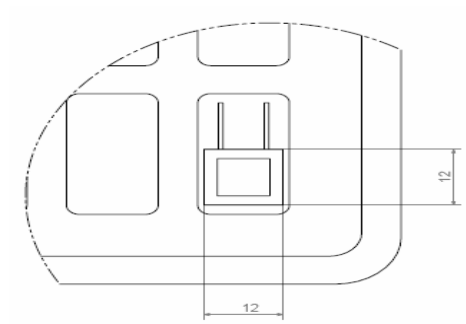
Cell Structure

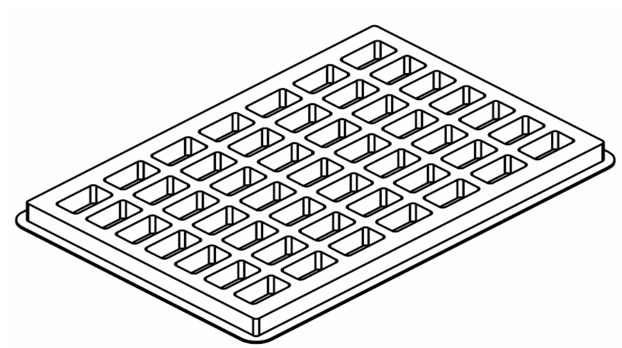


Packing (CL...12)



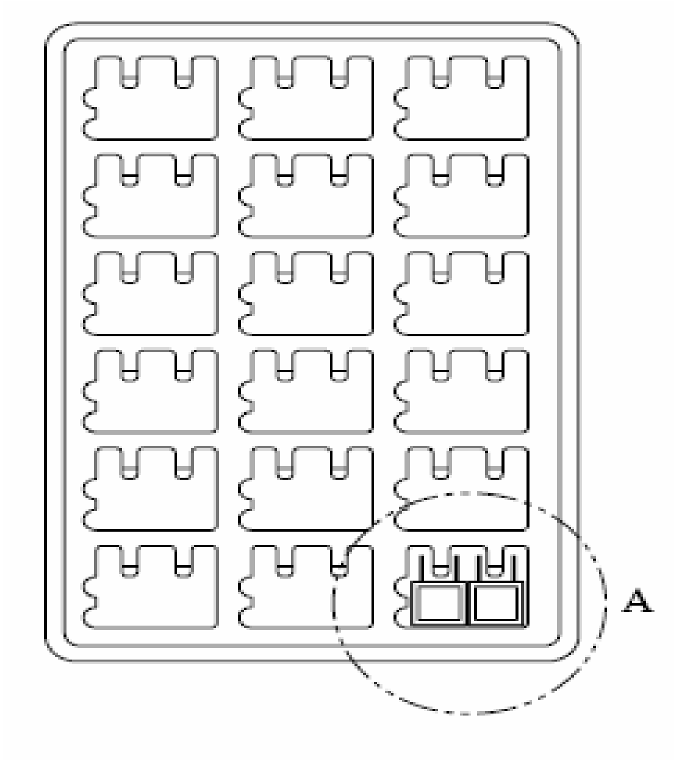
Weight = 33 gram
Dimension = 24.6mm x 16.8mm



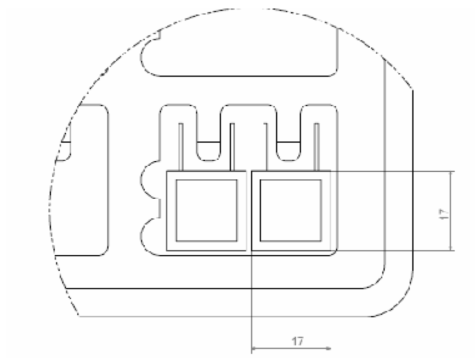


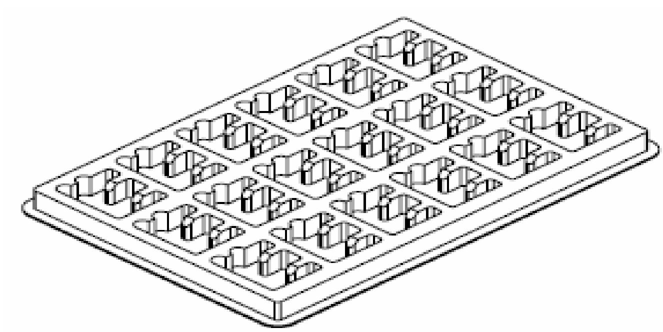
Supercapacitors per tray	Part Number
196	CLG03P012L12,CLG04P010L12,CLX04P007L12
147	CLG06P007L12,CLG03P025L12,CLG04P020L12
98	CLG06P012L12

Packing (CL...17)



Weight = 31 gram
Dimension = 24.6mm x 16.8mm





Supercapacitors per tray	Part Number
144	CLG02P080L17
108	CLG03P050L17,CLG04P040L17
72	CLG05P030L17

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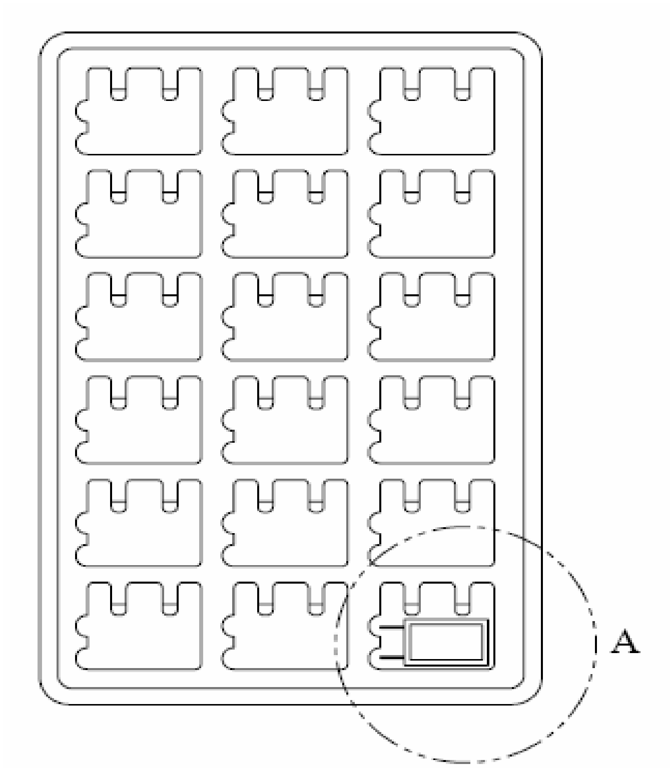
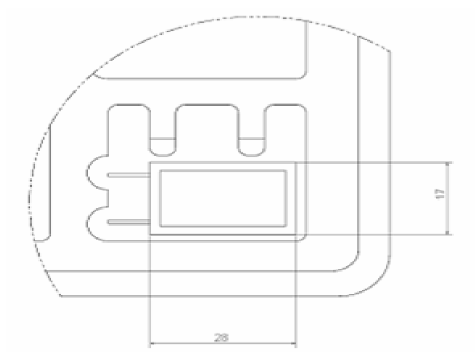
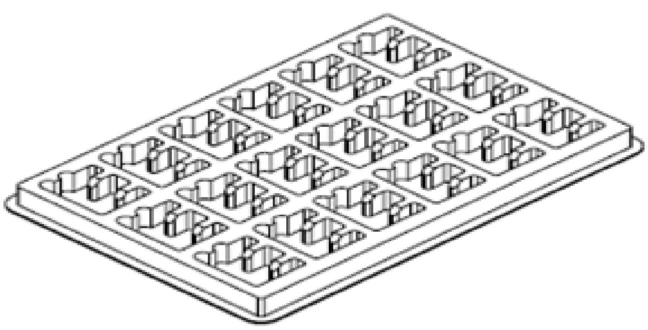
Packing (CL…28)



Weight = 31 gram
Dimension = 24.6mm x 16.8mm



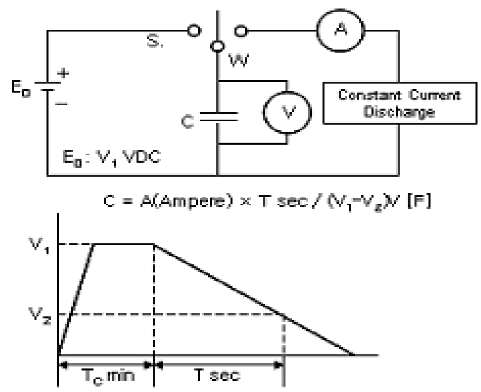


Supercapacitors per tray	Part Number
72	CLP04P040L28,CLG03P060L28,CLG04P050L28,
54	CLG05P040L28,CLG06P035L28,CLG03P120L28,CLG04P100L28
36	CLG12P015L28,CLG05P080L28,CLG06P070L28

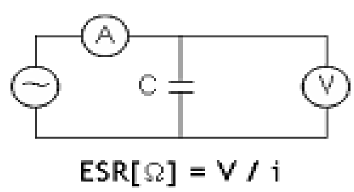
Qualification Test Summary

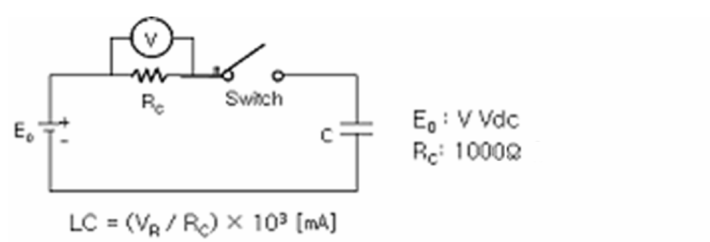
Test	Cellergy Qualification	Limits
Capacitance	Charge to rated voltage for 10min. discharge at constant current, C=Idt/dv	+80% / -20% of rated value
Leakage current	Charge to rated voltage 12 hr measure current	Within Limit
ESR	1 KHz, measure Voltage @20mV amplitude	+20% / -50% of rated value
Load Life	1000 hrs at 70°C at rated voltage Cool to RT measure: ESR,LC,C	LC <200% of initial rating Cap ±30% of initial rating ESR <200% of initial rating
Shelf life	1000 hrs at 70°C no voltage Cool to RT measure: ESR,LC,C	LC <200% of initial rating Cap ±30% of initial rating ESR <200% of initial rating
Humidity life	1000 hrs at 70°C 90-95% humidity no voltage Cool to RT measure: ESR,LC,C	LC <150% of initial rating Cap ±10% of initial rating ESR <150% of initial rating
Leg pull strength	In accordance with JIS-C5102,8.1	No change
Surge voltage	Apply 15% voltage above rated voltage for 10 sec short cells 10 seconds repeat procedure 1000 times measure ESR,LC,C	LC : <200% of initial rating Cap : ±30% of initial rating ESR <200% of initial rating
Temperature cycling	Each cycle consist of following steps: 1) Place supercapacitor in cold chamber (–40C) hold for 30 min 2) Transfer supercapacitor to hot chamber (+70C) in 2 to 3 minutes. 3) Hold supercapacitor in hot chamber for 30 min Number of cycles: 5	LC : <150% of initial rating Cap: ±10% of initial rating ESR: <150% of initial rating
Vibration	JIS-C5102,8.25-7 Hz displacement 25.4 mm 5 min 7-30 Hz Constant acceleration 1.5 gr. 10 min 30-50 Hz displacement 8.0 mm 5 min 50-500 Hz Constant acceleration 4.2 gr. 10 min sine pulse along 3 axis 300grs of 1.4mS (6 shocks)	LC : initial rating Cap : ±10% of initial rating ESR : initial rating
Solder ability	3/4 or more of pin should covered with new solder temp 360°, immersion time 8+/- 0.3 sec	LC : initial rating Cap : initial rating ESR : initial rating

Measuring Method of Characteristics

<table>
<tr><td>Capacitance</td><td>
1) Charge the capacitor at constant current to nominal voltage(V1) and hold the nominal voltage for 10 minutes.
2) Discharge the capacitor with constant current (A) to the voltage of (V2) while measure discharge time (T).
3) Calculate capacitance using following formula


</td></tr>
<tr><td>Equivalent Series Resistance

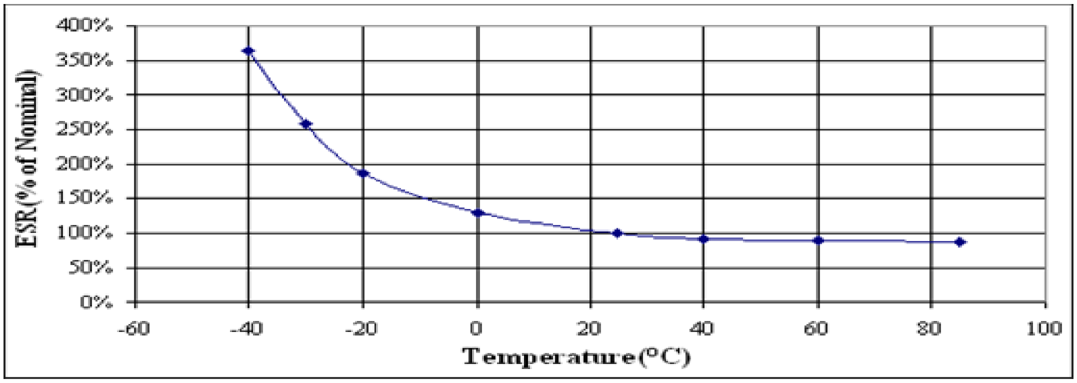
(ESR @1Khz)</td><td>
1) Measure ESR by HIOKI Model 3560 AC Low Ohmmeter


</td></tr>
<tr><td>Leakage Current</td><td>
1) Apply Nominal voltage to the capacitor.
2) Measure Vr after 12±1 hours.
3) Calculate current using following formula.


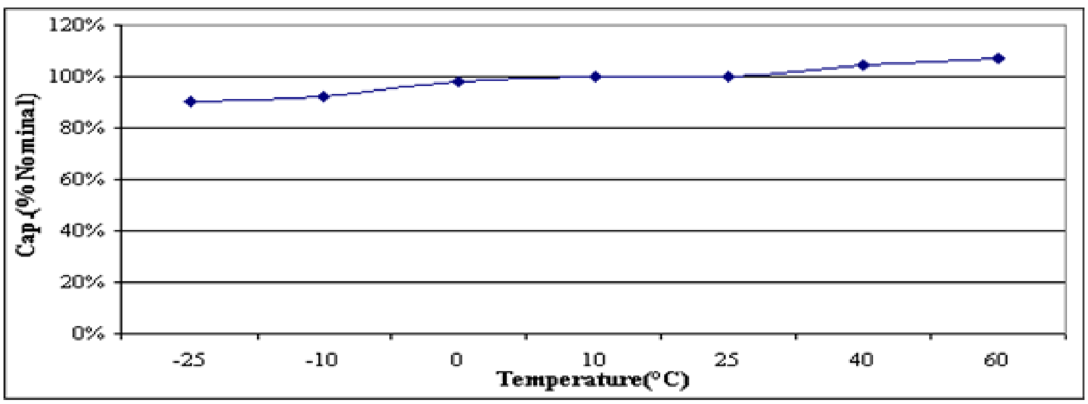
</td></tr>
<tr><td colspan="2">Supercapacitor should be shorted before each measurement as follows:
Capacitance:60 min., ESR: 15 min., LC: 12 hours</td></tr>
</table>

Typical Capacitor Characteristics

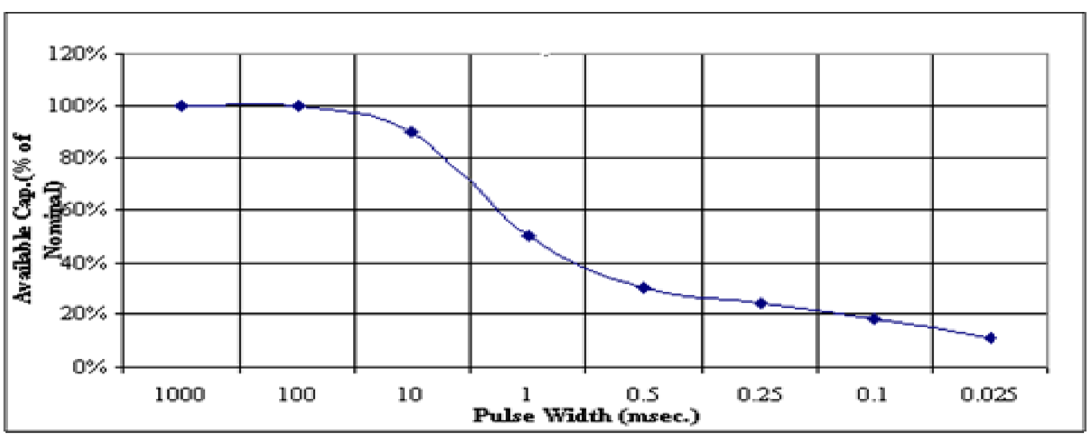
ESR vs. Temperature



Capacitance vs. Temperature



Capacitance vs. Pulse Width



Part 2: User Manual

1. Background

Film capacitors store charge by means of two layers of conductive film that are separated by a dielectric material. The charge accumulates on both conductive film layers, yet remains separated due to the dielectric between the conductive films.
Electrolytic capacitors are composed of metal to which is added a thin layer of non-conductive metal oxide which serves as the dielectric.
These capacitors have an inherently larger capacitance than that of standard film capacitors.
In both cases the capacitance is generated by electronic charge and therefore the power capability of these types of capacitors is relatively high while the energy density is much lower.
The Electrochemical Double Layer Capacitor (EDLC) or Super Capacitor is a form of hybrid between conventional capacitors and the battery.
The electrochemical capacitor is based on the double layer phenomena occurring between a conductive solid and a solution interphase.
The capacitance, coined the "double layer capacitance", is the result of charge separation in the interphase. On the solid electrode, electronic charge is accumulated and in the solution counter charge is accumulated in the form of ionic charge.
The EDLC embodies high power and high energy density (Fig. 1).

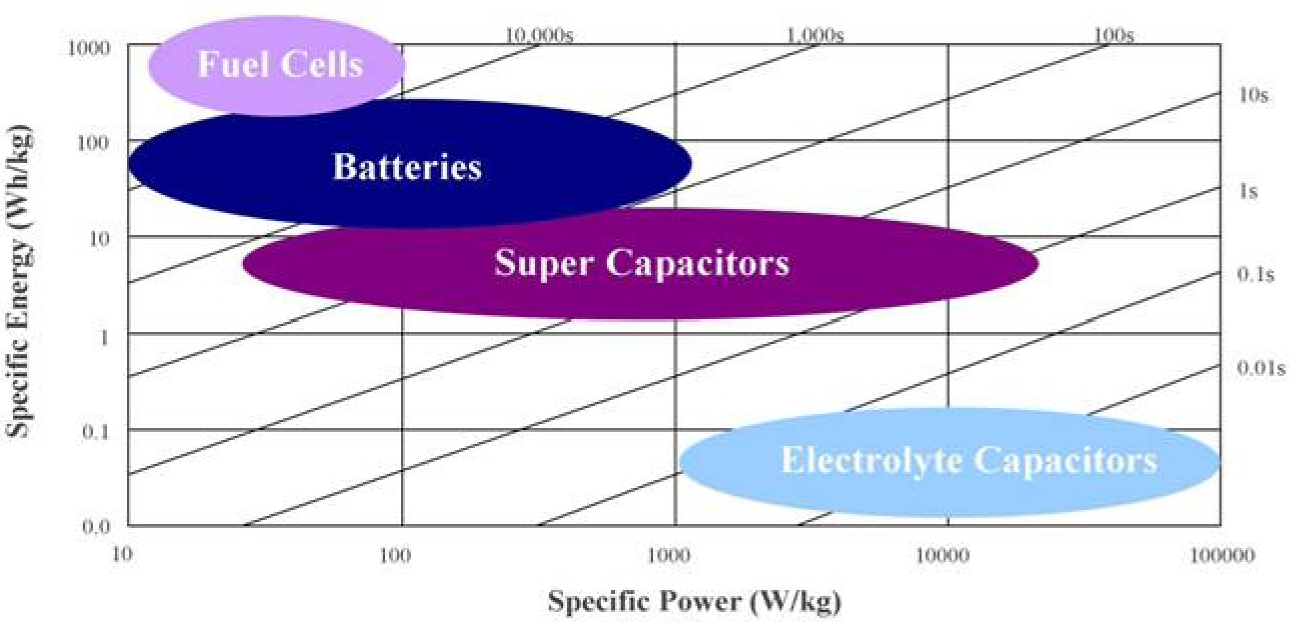


Fig. 1

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Electrochemical Capacitors

The operating principle of the super capacitor is similar to that of a battery. Pairs of electrodes are separated by an ionic conductive, yet electrically insulating, separator (Fig. 2). When a super capacitor is charged, electronic charge accumulates on the electrodes (conductive carbon) and ions (from the electrolyte) of opposite charge approach the electronic charge.

This phenomenon is coined "the double layer phenomenon".

The distance between the electronic and the ionic charges is very small, roughly 1 nanometer, yet electronic tunneling does not occur.

Between charging and discharging, ions and electrons shift locations.

In the charged state a high concentration of ions will be located along the electronically charged carbon surface (electrodes).

As the electrons flow through an external discharge circuit, slower moving ions will shift away from the double layer. During EDLC cycling electrons and ions constantly move in the capacitor, yet no chemical reaction occurs.

Therefore electrochemical capacitors can undergo millions of charge and discharge cycles. This phenomenon which occurs with carbon electrodes of very high surface area and a three-dimensional structure, leads to incredibly high capacitance as compared to standard capacitors.

One can envision the model of the EDLC as two capacitors formed by the solid (carbon) liquid (electrolyte) interphase separated by a conductive ionic membrane. An equivalent electronic model is two capacitors in a series connection (Fig. 3) where C_{dl} is the capacitance of each electrode; R_p is the parallel resistance to the electrode, R_s is the resistance of the separator.

We conclude that the energy density of electrochemical capacitors is higher than that of electrolytic capacitors, and therefore they have applicability for systems with lower frequency requirements.

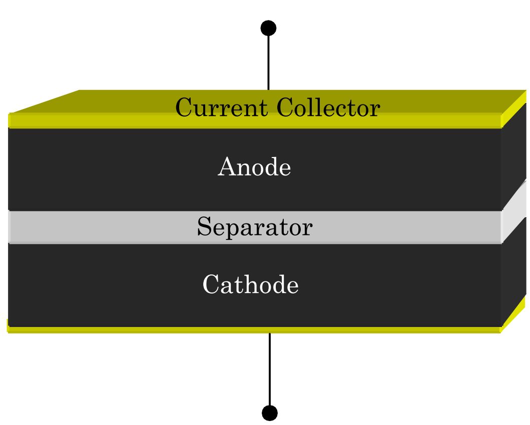

Fig. 2

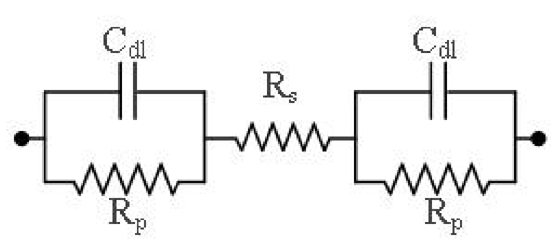

Fig. 3

Cellergy's Technology

By use of a unique patented production and manufacturing process, Cellergy has developed a small footprint, low Equivalent Series Resistance (ESR), high frequency EDLC capable of storing relatively large amounts of energy.
The development is based on an innovative printing technology allowing the production of EDLC's in many different sizes with varied dimensions and shapes.
In fact, Cellergy produces one of the smallest low ESR footprint EDLC's on the market today.
Since the patented printing technology is based on conventional printing techniques, the manufacturing process is simple and unique, and it is possible to manufacture large wafers of EDLC's.
The basis of the technology is a printable aqueous electrode paste based on a high surface area carbon paste that is printed in an electrode matrix structure on an electronically conductive film.
The electrodes are then encapsulated with a porous ionic conducting separator and another electrode matrix is then printed on the separator.
This bipolar printing process is repeated as many times as required enabling us to tailor our product to the specifications of the end user.
The finished wafer is then cut into individual EDLC's that are then packaged.
Cellergy's EDLC's boasts low equivalent series resistance as well as a low leakage current due to our unique encapsulation technology and electrode composition.
Cellergy's EDLC's require no cell balancing or de-rating.
The combination of the separator and carbon paste lead to the capability of very high power bursts within low milli-second pulse widths.
Cellergy's technology is based on aqueous components that are all environmentally friendly and non-toxic. Though the system is water based, the capacitor can work at temperatures between -40°C and 70°C.
This working temperature range is achieved by the unique water based electrolyte that impregnates the high surface carbon.
Because the chemistry of the system is based on water, the performance of Cellergy's EDLC's is not affected by humidity.

Application Notes for EDLC

Cellergy's super capacitors offer high power and high energy.
This characteristic coupled with a battery offer the designer a unique opportunity to solve power related issues.
The following table lists the characteristics of the EDLC (Table 1):

Characteristics	
Working Voltage	1-12 volts
De-rating	Not required
Capacitance	10-100's of mF
Foot print	Selectable down to 17mm by 17 mm
Operating Temperatures	-40°C to +70°C
SMT	Under development.
ESR	10's-100's mΩ
Expected life	50,000 hours
Safety	Environmentally friendly materials, No toxic fumes upon burning
Power	10's of amps, short pulse widths
Polarity	No polarity
Number of cycles	Not limited

Table 1

Voltage Drop

Two main factors affect the voltage drop of all capacitors including EDLC's.
The first voltage drop is defined as the ***Ohmic voltage drop***.
The capacitor has an internal resistance defined as ESR (Equivalent Series Resistance).
As current flows through the capacitor, a voltage drop occurs that obeys Ohms law. This voltage drop is instantaneous and will diminish the moment that no current is drawn.
The second voltage drop (***capacitance related voltage drop***) is due to capacitor discharge.
The voltage of the capacitor is directly proportional to the charge accumulated in the capacitor. During current discharge, capacitance is consumed (current emitting from the capacitor) thus causing a linear voltage decrease in the capacitor. When the current is stopped, the voltage of the capacitor indicates the charge left in the capacitor. The combination of the Ohmic related voltage drop and the capacitance related voltage drop determine the actual ***working voltage window*** of an EDLC under drain conditions (Fig. 4).

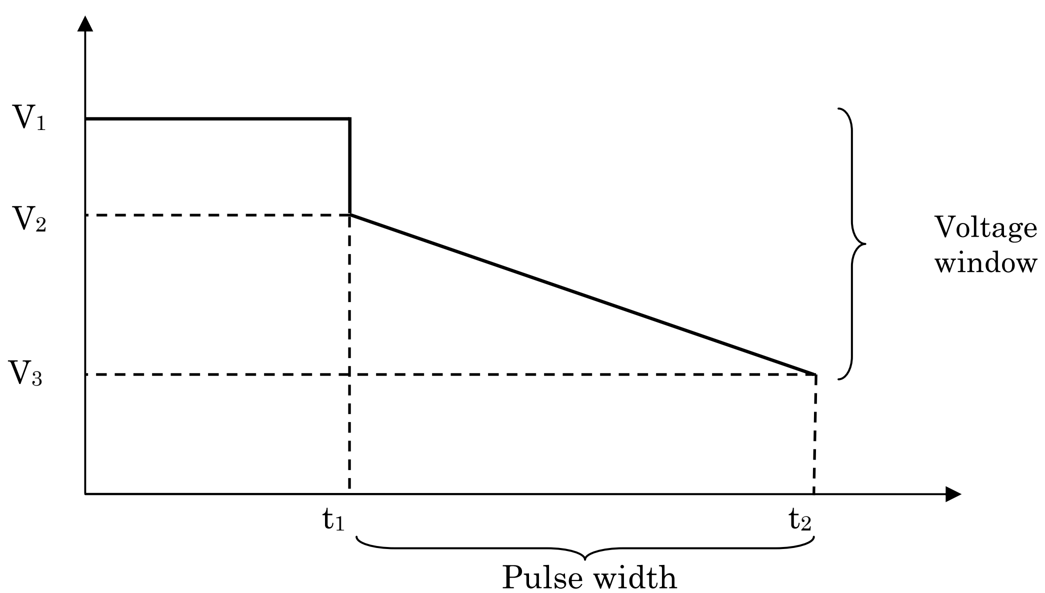

Fig. 4

Ohmic voltage drop $= V_1 - V_2 = I_{pulse} * ESR$
Capacitance related voltage drop $= V_2 - V_3 = I_{pulse} * (t_2 - t_1)/C$
Working voltage window $= V_1 - V_3 = I_{pulse} * ESR + I_{pulse} * (t_2 - t_1)/C$

*Where C is Capacitance

EDLC and Battery Coupling

Under drain conditions, a battery undergoes a voltage drop similarly to the EDLC. Because of many physical and chemical constraints, the battery often cannot supply the power required while still retaining its open circuit voltage.
The working voltage of the battery reflects the load on the battery, thus the larger the voltage drop of the battery the larger the load on the battery.
Many difficulties are encountered by the designer planning the online power demand of a system, mainly because the power of the batteries is limited.
If the battery must supply high power at short pulse widths, the voltage drop may be too great to supply the power and voltage required by the end product (cutoff voltage).
The large load on the battery may decrease the useful energy stored in the battery and even may harm the battery and shorten its work life.
This problem may be resolved by connecting the battery in parallel to an EDLC (Fig. 5).

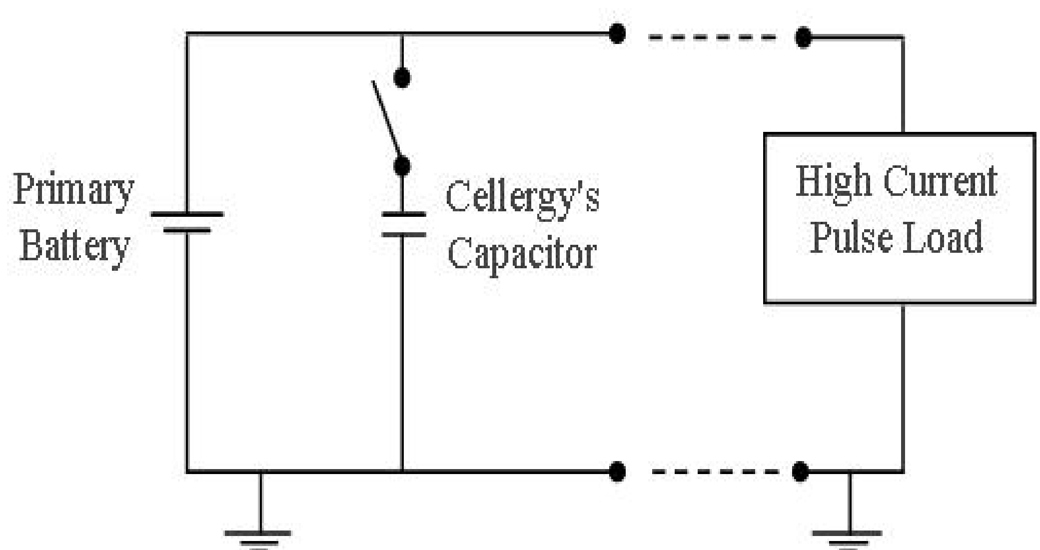

Fig. 5

EDLC and Battery Coupling (Continued)

Under conditions of high power and short duration current pulses, a ***voltage damping effect*** will be achieved. The voltage drop of the battery will be decreased resulting in better energy management and superior energy density of the battery (Fig. 6).

The power supplied will be produced by both the EDLC and the battery, and each will supply the relative power inversely to its own ESR.

The inefficiency of batteries at lower temperatures is well known.

The capacitance of most batteries decreases with decreasing temperatures.

This decrease is due to the slow kinetics of the chemical reaction in the battery which increases the internal resistance of the battery.

At low temperatures, the voltage drop of the battery increases and reduces the usefulness of the battery. This voltage drop can be reduced greatly by coupling of the battery and the EDLC.

In conclusion, coupling the battery and EDLC results in superior power management for many short interval and high power applications.

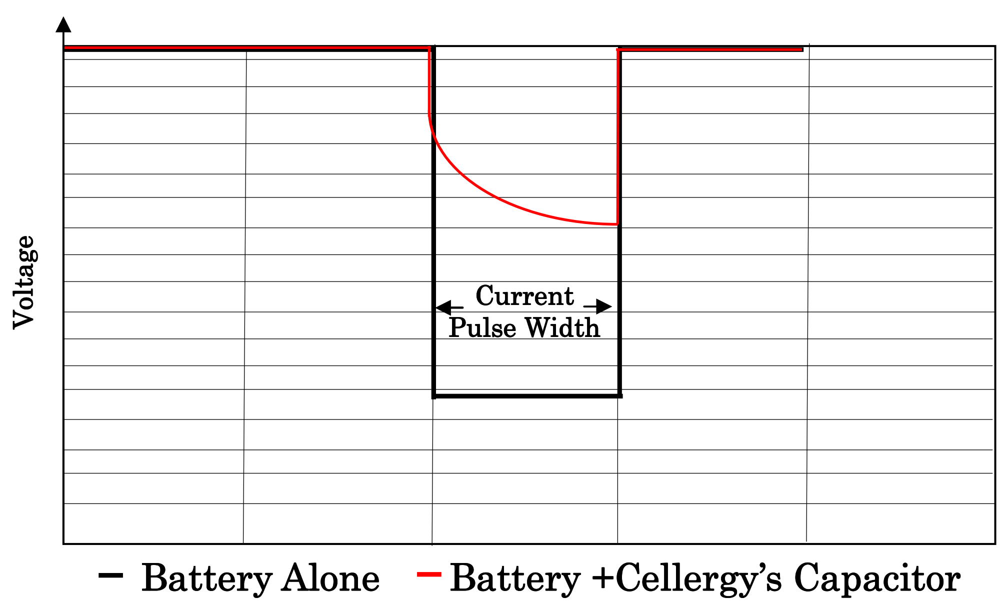

Fig. 6

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Distinct Applications for Cellergy's Super Capacitors

- Extending battery lifetimes – by connecting a primary battery in parallel to Cellergy's capacitor, the designer can reduce the voltage drop during a high current pulse.
- Extending secondary battery operation - Reducing voltage drop at low temperatures (-40°C).
- CF, PCMCIA Cards - Cellergy's EDLC overcome the current limitation encountered when connecting boards in an application utilizing batteries.
- Backup or current booster for mechanical applications such as a DC motor.
- Extending the battery lifetime of digital cameras.
- Rechargeable backup power source for microprocessors, static RAM's and DAT.
- AMR – Automatic Meter Readings.
- GPS-GSM Modules.

Manual Soldering

Upon using a soldering iron, it should not touch the cell body.

Temperature of the soldering iron should be less than 360±5℃.

Soldering time for terminals should be less than 8 ± 0.3 seconds.

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Handling Cautions

1) Do not apply more than rated voltage.
   If you apply more than rated voltage, Cellergy electrolyte will be electrolyzed and the super capacitors ESR may increase.

2) Do not use Cellergy for ripple absorption.

3) Operating temperature and life
   Generally, Cellergy has a lower leakage current, longer back-up time and longer life in the low temperature range i.e. the room temperature. It will have a higher leakage current and a shorter life at elevated temperatures.
   Please design the Cellergy such that is not adjacent to heat emitting elements.

4) Short-circuit Cellergy
   You can short-circuit between terminals of Cellergy without a resistor. However when you short-circuit frequently, please consult us.

5) Storage
   In long term storage, please store Cellergy in following condition;
   1) TEMP. : 15 ~ 25 °C
   2) HUMIDITY: 45 ~ 75 %RH
   3) NON-DUST

6) Do not disassemble Cellergy. It contains electrolyte.

7) The tips of Cellergy terminals are very sharp. Please handle with care.

8) Reflow process is not recommended for Cellergy capacitors.

Note
The Cellergy EDLC is a water based component. Extended use of the EDLC at elevated temperatures may cause evaporation of water leading to ESR increase.