MB86953

PC BUS INTERFACE UNIT

FUJITSU

T-75-49

DATA SHEET

JANUARY 1992

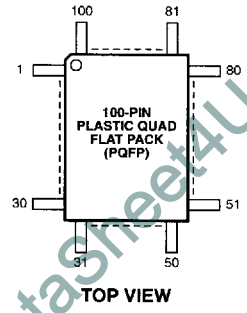
FEATURES

- Companion chip for MB86950 EtherStar™ and MB86960 NICE™ Ethernet LAN Controllers
- Provides interface between controller and IBM® PC, XT™ or AT® bus
- Substantially reduces parts count for LAN adapter
- 8- and 16-bit bus capability
- Supports 8 and 16 Kbyte static RAM and 16, 32 and 64 Kbyte DRAM buffer memory implementations
- Provides decoding for Ethernet node ID PROM
- Programmable adapter I/O address
- Programmable boot PROM address
- 100-pin plastic quad flat pack
- Low-power, high-speed CMOS technology

GENERAL DESCRIPTION

The MB86953 PC Bus Interface Unit (PCBIU) is a single-chip implementation of the logic necessary to interface a LAN adapter utilizing Fujitsu's MB86950 EtherStar or MB86960 NICE controllers to the bus of IBM or compatible PC, XT and AT computers. Implemented in CMOS technology, the PCBIU eliminates external SSI or MSI 'glue' logic for 8-bit adapters, and requires only one or two external parts for 16-bit adapters, depending on buffer memory configuration. Buffer memory may be implemented with static RAM for minimum cost, or with DRAM for larger buffer requirements. The PCBIU allows selection of eight different I/O port addresses and seven different boot EPROM base addresses via external switches or jumpers. Address decoding for an external Ethernet node ID PROM is also provided.

PIN CONFIGURATION



TOP VIEW

(For pin assignment, see pin assignment table)

T-75-49

PIN ASSIGNMENT – PQFP

PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE
1	SADR4	I	26	SDATA1	B24	51	N.C.	-	76	LSADR1	O3
2	SADR5	I	27	N.C.	-	52	SDATA7	B24	77	LSADR0	O3
3	VCC	-	28	VCC	-	53	VCC	-	78	VCC	-
4	GND	-	29	GND	-	54	GND	-	79	GND	-
5	IRQ	OD24	30	AEN	I	55	LBA6/–ROUT	O3	80	–DSEL	O3
6	SADR6	I	31	CHRESET	IS	56	LBA1/–WEH	O3	81	–RSEL/–ECS	O3
7	SADR7	I	32	SDATA2	B24	57	LBA0/–WEL	O3	82	–RINT	IP
8	SADR8	I	33	N.C.	-	58	LBA2/LADR	O3	83	–TINT/–INT	I
9	SADR9	I	34	SDATA3	B24	59	LBA5	O3	84	–READY	I
10	SYSCLK	IS	35	N.C.	-	60	LBA3/–SHE	O3	85	RESET	O3
11	–DMACK	IP	36	SDATA4	B24	61	LBA4/–TOE	O3	86	–ROMSEL	O3
12	SADR14	I	37	N.C.	-	62	BA6	IP	87	IDATA7	B3
13	IOCHRDY1	OD12	38	MODE0	IP	63	BA5	IP	88	IDATA6	B3
14	IOCHRDY2	OD12	39	MODE1	IP	64	–SMEMR	I	89	IDATA5	B3
15	GND	-	40	GND	-	65	GND	-	90	GND	-
16	SADR15	I	41	MSEL2	IP	66	BA4	IP	91	IDATA4	B3
17	SADR16	I	42	MSEL1	IP	67	BA3/–SBHE	I	92	IDATA3	B3
18	–IOR	I	43	MSEL0	IP	68	BA2/–WE	I	93	IDATA2	B3
19	SADR17	I	44	IOSEL2	IP	69	BA1/–CAS	I	94	IDATA1	B3
20	–IOW	I	45	IOSEL1	IP	70	BA0/–RAS1	I	95	IDATA0	B3
21	SADR18	I	46	IOSEL0	IP	71	–WRITE	O3	96	–IDROMSEL	O3
22	–ZWS/–IO16	OD24	47	N.C.	-	72	–READ	O3	97	SADR0	I
23	SADR19	I	48	SDATA5	B24	73	–RAS0	IP	98	SADR1	I
24	SDATA0	B24	49	N.C.	-	74	LSADR3	O3	99	SADR2	I
25	N.C.	-	50	SDATA6	B24	75	LSADR2	O3	100	SADR3	I

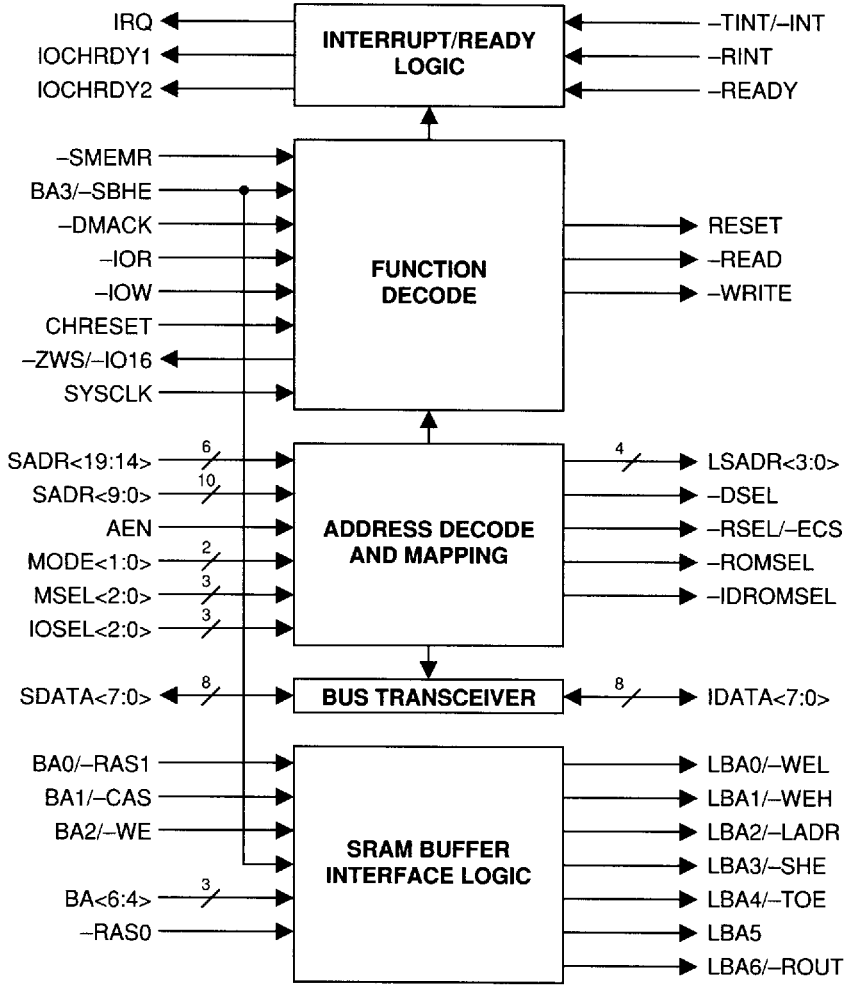
NOTE: I = Standard input
IS = Schmitt trigger input
IP = Input with pull-up resistor
B3 = 3.2mA bidirectional I/O
B24 = 24mA bidirectional I/O
O3 = 3.2mA totem pole output
OD12 = 12mA open drain output
OD24 = 24mA open drain output
N.C. = No connect

ORDERING CODE

PACKAGE STYLE	PACKAGE CODE	V_{CC} = +5V ± 5%, T_A = 0 to +70°C
100-Pin Plastic Quad Flat Pack	FPT-100P-M01	MB86953PF-G

BLOCK DIAGRAM

T-75-49



T-75-49

PIN DESCRIPTIONS[1]

PIN NO.	SYMBOL	TYPE	DESCRIPTION
23, 21, 19, 17, 16, 12	SADR<19:14>	I	**HIGH ORDER SYSTEM ADDRESS:** These inputs are connected to the corresponding signals from the system bus.
9 - 6, 2, 1, 100 - 97	SADR<9:0>	I	**LOW ORDER SYSTEM ADDRESS:** These inputs are connected to the corresponding signals from the system bus.
30	AEN	I	**ADDRESS ENABLE:** Input signal from the system bus. When low, indicates that an I/O slave may respond to addresses and I/O commands on the system bus.
39, 38	MODE<1:0>	IP	**MODE CONTROL:** These inputs set the operation mode of the MB86953. See Functional Description for additional information.
41 - 43	MSEL<2:0>	IP	**MEMORY ADDRESS:** These inputs set the base address at which the –ROMSEL output is asserted. See Functional Description for additional information.
44 - 46	IOSEL<2:0>	IP	**I/O ADDRESS:** These inputs set the base address at which the controller is located, and control the assertion of the –DSEL and –RSEL/–ECS outputs. See Functional Description for additional information.
74 - 77	LSADR<3:0>	O3	**LATCHED SYSTEM ADDRESS:** Latched outputs used as address inputs for the controller. These outputs may be modified as described in the Functional Description section.
80	–DSEL	O3	**DATA SELECT:** When operating in the MB86950 (EtherStar) mode, an active low output indicating that the current I/O access is to the BMP register set.
81	–RSEL/–ECS	O3	**REGISTER SELECT:** When operating in the MB86950 (EtherStar) mode, an active low output indicating that the current I/O access is to the DLC register set. When operating in the MB86960 (NICE) mode, an active low output indicating that the current I/O access is for the controller.
86	–ROMSEL	O3	**BOOT ROM SELECT:** Active low enable output indicating that the current memory access is in the range defined by the MSEL<2:0> inputs.
96	–IDROMSEL	O3	**ID ROM SELECT:** Active low enable output indicating that the current I/O access is in the space assigned for the ID ROM.
64	–SMEMR	I	**SYSTEM MEMORY READ:** Active low signal from the system bus which indicates that the current bus cycle is a memory read operation.
20	–IOW	I	**I/O WRITE:** Active low signal from the system bus which indicates that the current bus cycle is an I/O write operation.
18	–IOR	I	**I/O READ:** Active low signal from the system bus which indicates that the current bus cycle is an I/O read operation.
11	–DMACK	IP	**DMA ACKNOWLEDGE:** Active low signal from the system bus indicating that a DMA acknowledge cycle is in progress.
31	CHRESET	IS	**CHANNEL RESET:** Reset signal from the system bus used to generate a reset to the controller chip and other logic on the board.
22	–ZWS/–IO16	OD24	**ZERO WAIT STATE/IO CHANNEL SIZE 16:** In 8-bit mode this active low output is used to shorten the timing of the I/O cycle. In 16-bit mode this active low output indicates that the channel size is 16 bits.
10	SYSCLK	IS	**SYSTEM CLOCK:** Clock from the system bus which controls the timing of several signals from the PCBIU.

1. In the following descriptions, signal names preceded by a minus sign (–) indicate an active low state. Dual function pins have two names separated by a slash (/).

PIN DESCRIPTIONS (continued)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
85	RESET	O3	**RESET:** Reset output to the controller and other board logic. Produced in response to receipt of CHRESET.
72	–READ	O3	**READ STROBE:** Active low output to the controller which indicates that the current I/O operation is a read cycle.
71	–WRITE	O3	**WRITE STROBE:** Active low output to the controller which indicates that the current I/O operation is a write cycle.
52, 50, 48, 36, 34, 32, 26, 24	SDATA<7:0>	B24	**SYSTEM DATA BUS:** Bidirectional bus for the least significant byte of system data. In 8-bit mode, all data transactions take place over this bus. In 16-bit mode, an external transceiver is required for the upper byte of data.
87 - 89, 91 - 95	IDATA<7:0>	B3	**INTERNAL DATA BUS:** Internal, isolated, 8-bit bidirectional data bus corresponding to SDATA<7:0>.
13, 14	IOCHRDY1, 2	OD12	**I/O CHANNEL READY:** Active high outputs to the system bus indicating that the addressed I/O device is ready for the bus transaction. The outputs can be connected together for increased current sink capability.
5	IRQ	OD24	**INTERRUPT REQUEST:** This output to the system bus indicates that the controller chip is requesting an interrupt.
83	–TINT/–INT	I	**TRANSMIT INTERRUPT / INTERRUPT:** In MB86950 mode, an active low transmit interrupt request input from the controller. In MB86960 mode, an active low interrupt request input from the controller.
82	–RINT	IP	**RECEIVE INTERRUPT:** In MB86950 mode, an active low receive interrupt request input from the controller.
84	–READY	I	**READY:** An active low input from the controller indicating that it is ready to complete the requested bus transaction.
73	–RAS0	IP	**ROW ADDRESS STROBE 0:** In 8-bit MB86950 mode, an input for the RAS0 signal from the controller. Used to latch the buffer address BA<6:0> into the internal address latch to allow operation with static RAM.
70	BA0/–RAS1	I	**BUFFER ADDRESS 0 / ROW ADDRESS STROBE 1:** In 8-bit MB86950 mode, an input for the BA0 signal from the controller. In 16-bit MB86950 mode, an input for the –RAS1 signal from the controller.
69	BA1/–CAS	I	**BUFFER ADDRESS 1 / COLUMN ADDRESS STROBE:** In 8-bit MB86950 mode, an input for the BA1 signal from the controller. In 16-bit MB86950 mode, an input for the –CAS signal from the controller.
68	BA2/–WE	I	**BUFFER ADDRESS 2 / WRITE ENABLE:** In 8-bit MB86950 mode, an input for the BA2 signal from the controller. In 16-bit MB86950 mode, an input for the write enable signal from the controller.
67	BA3/–SBHE	I	**BUFFER ADDRESS 3 / SOURCE BYTE HIGH ENABLE:** In 8-bit MB86950 mode, an input for the BA3 signal from the controller. In 16-bit mode, an input for the active low –SBHE signal from the system bus.
62, 63, 66	BA<6:4>	IP	**BUFFER ADDRESS <6:4>:** In 8-bit MB86950 mode, inputs for the corresponding signals from the controller.
57	LBA0/–WEL	O3	**LATCHED BUFFER ADDRESS 0 / WRITE ENABLE LOW:** In 8-bit MB86950 mode, the latched BA0 output for the SRAM. In 16-bit MB86950 mode, the active low write enable output for the low byte of the buffer SRAM.

T-75-49

PIN DESCRIPTIONS (continued)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
56	LBA1/–WEH	O3	**LATCHED BUFFER ADDRESS 1 / WRITE ENABLE HIGH:** In 8-bit MB86950 mode, the latched BA1 output for the SRAM. In 16-bit MB86950 mode, the active low write enable output for the high byte of the buffer SRAM.
58	LBA2/LADR	O3	**LATCHED BUFFER ADDRESS 2 / LATCH ADDRESS STROBE:** In 8-bit MB86950 mode, the latched BA2 output for the SRAM. In 16-bit MB86950 mode, the control signal used to strobe the row address from the controller into an external latch to address the SRAM.
60	LBA3/–SHE	O3	**LATCHED BUFFER ADDRESS 3 / LATCHED SOURCE BYTE HIGH ENABLE:** In 8-bit MB86950 mode, the latched BA3 output for the SRAM. In 16-bit mode, the active low output to the controller corresponding to the –SBHE signal from the system bus. This signal is latched by the –READY input.
61	LBA4/–TOE	O3	**LATCHED BUFFER ADDRESS 4 / TRANSCEIVER OUTPUT ENABLE:** In 8-bit MB86950 mode, the latched BA4 output for the SRAM. In 16-bit mode, an active low output enable for the external transceiver for the high byte of data.
59	LBA5	O3	**LATCHED BUFFER ADDRESS 5:** In 8-bit MB86950 mode, the latched BA5 output for the SRAM.
55	LBA6/–ROUT	O3	**LATCHED BUFFER ADDRESS 6 / RAS OUT:** In 8-bit MB86950 mode, the latched BA6 output for the SRAM. In 16-bit mode, an active low output which is asserted whenever the –RAS0 or –RAS1 inputs are asserted.
3, 28, 53, 78	V_{CC}	–	**+5 VOLT POWER INPUT**
4, 15, 29, 40, 54, 65, 79, 90	GND	–	**POWER AND SYSTEM GROUND**

NOTE: I = Standard input
IS = Schmitt trigger input
IP = Input with pull-up resistor
B3 = 3.2mA bidirectional I/O
B24 = 24mA bidirectional I/O
O3 = 3.2mA totem pole output
OD12 = 12mA open drain output
OD24 = 24mA open drain output

FUNCTIONAL DESCRIPTION

This section provides a detailed description of the operation of the MB86953 PCBIU. Reference should also be made to the timing diagrams in the Electrical Characteristics section of this data sheet for additional information.

The block diagram illustrates the major functional blocks of the MB86953. These are:

- Function decode
- Bus transceiver
- Address decode and mapping
- Interrupt and ready logic
- SRAM buffer interface logic

FUNCTION DECODE

This block converts system bus control and timing signals to appropriate signals to control read and write operations for the adapter logic. The –READ output is asserted whenever the system performs a valid read of the boot ROM, the ID ROM or the controller, and the –WRITE output is asserted whenever the system performs a valid write to the controller. This block also generates a RESET signal in response to a system write to any address in the range 0x18 - 0x1F or assertion of the CHRESET input by the system, and asserts the –ZWS and –IO16 signals with appropriate timing during 8- and 16-bit modes respectively.

BUS TRANSCEIVER

The PCBIU incorporates an 8-bit bus transceiver for the lower eight data bits of the system bus (SDATA<7:0>). This transceiver is capable of sinking 24mA on the system bus side and 3.2mA on the adapter logic side (IDATA<7:0>). The transceiver drives the system bus side when a read cycle is made to the boot ROM, the ID ROM or the controller, and drives the adapter logic side when a write cycle to the controller is performed. The enable timing for the transceiver is controlled by the –IOW and –IOR system bus inputs.

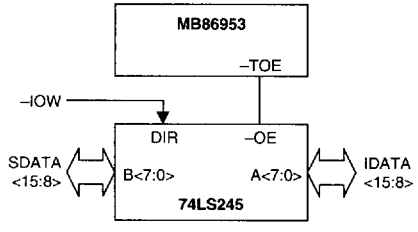


Figure 1. External Transceiver for Upper Data Bus

For 16-bit operation, an external transceiver for the upper eight data bits is required. The –TOE output, which is active in 16-bit mode, is used to control the enabling of the external transceiver, and –IOW from the system bus controls its data direction. See Figure 1.

INTERRUPT AND READY LOGIC

The IRQ output to the system is asserted whenever the controller requests an interrupt, as indicated by assertion of the –RINT or –TINT/–INT inputs from the adapter logic. Assertion of the IOCHRDY1 and IOCHRDY2 outputs to the system indicates that the controller has responded with its –READY output and is ready to complete the requested read or write cycle. The two IOCHRDY outputs may be tied together to provide 24mA sink capability.

ADDRESS DECODE AND MAPPING

This functional block receives address inputs from the system bus and select inputs from switches or jumpers on the adapter board and generates the appropriate signals to select the boot ROM, the ID ROM or the controller. It also latches and outputs the four least significant bits of the system address for use by the controller. These outputs are remapped when certain registers of the controller are accessed to permit use of additional types of processor instructions, thus allowing greater flexibility in writing the driver for the controller.

The MODE<1:0> inputs select 8- or 16-bit operation with either the MB86950 (EtherStar) or MB86960 (NICE) LAN controllers. Decoding for these inputs, which contain internal pullup resistors, is shown in Table 1.

The MB86953 provides for an optional boot ROM of up to 16 Kbytes on the adapter board. Address selection for this ROM is performed by the MSEL<2:0> inputs. Decoding for these inputs, which contain internal pullup resistors, is shown in Table 2.

I/O address selection of the 32-byte address block for the controller and ID ROM is performed by the IOSEL<2:0> inputs. Decoding for these inputs, which contain internal pullup resistors, is shown in Table 3. Table 4 shows the select output which is asserted and the address output at LSADR<3:0> whenever the

system address lies within the address block selected by IOSEL<2:0>.

SRAM BUFFER INTERFACE LOGIC

The PCBIU provides interface logic to allow implementation of an 8 Kbyte or 8 Kword buffer memory with low-cost SRAM when using the MB86950 controller. In 8-bit mode, the PCBIU latches the upper 7 bits of the buffer memory address from the multiplexed buffer address lines (BA<6:0>) from the controller. The latched outputs are provided on LBA<6:0>. In 16-bit mode, the PCBIU generates

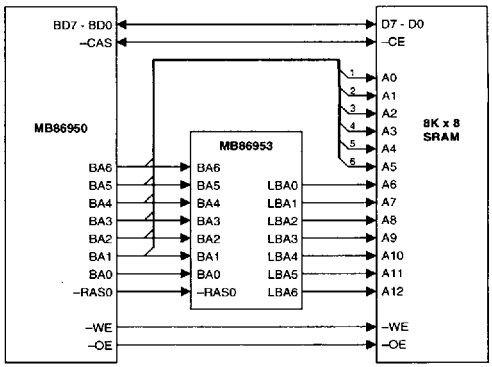


Figure 2. 8-Bit SRAM Buffer for MB86950 EtherStar

TABLE 1. Operating Mode Decoding

MODE 1	MODE 0	OPERATION MODE
0	0	8-bit NICE (MB86960)
0	1	16-bit NICE (MB86960)
1	0	8-bit EtherStar (MB86950)
1	1	16-bit EtherStar (MB86950)

TABLE 2. Boot ROM Address Decoding

MSEL2	MSEL1	MSEL0	ROM ADDRESS
0	0	0	0xC4000 - 0xC7FFF
0	0	1	0xC8000 - 0xCBFFF
0	1	0	0xCC000 - 0xCFFFF
0	1	1	0xD0000 - 0xD3FFF
1	0	0	0xD4000 - 0xD7FFF
1	0	1	0xD8000 - 0xDBFFF
1	1	0	0xDC000 - 0xDFFFF
1	1	1	Decode Disabled

TABLE 3. I/O Addressing

MSEL2	MSEL1	MSEL0	I/O ADDRESS
0	0	0	0x260 - 0x27F
0	0	1	0x280 - 0x29F
0	1	0	0x2A0 - 0x2BF
0	1	1	0x2E0 - 0x2FF
1	0	0	0x300 - 0x31F
1	0	1	0x320 - 0x33F
1	1	0	0x380 - 0x39F
1	1	1	0x3E0 - 0x3FF

TABLE 4. System Address Translation to Select Outputs and Latched Address

SYSTEM ADDRESS	MODE = 00 (NICE 8)		MODE = 01 (NICE 16)		MODE = 10 (ES 8)		MODE = 11 (ES 16)	
	LSADR	SELECT	LSADR	SELECT	LSADR	SELECT	LSADR	SELECT
0x00[1]	0	-ECS	0	-ECS	0	-RSEL	0	-RSEL
|	|	|	|	|	|	|	|	|
0x0F	F	-ECS	F	-ECS	F	-RSEL	F	-RSEL
0x10	8	-ECS	8	-ECS	0	-DSEL	0	-DSEL
0x11	9	|	9	|	0	|	1	|
0x12	A	|	A	|	2	|	2	|
0x13	B	|	B	|	3	|	3	|
0x14	8	|	8	|	4	|	0	|
0x15	9	|	9	|	5	|	1	|
0x16	8	|	8	|	6	|	0	|
0x17	9	-ECS	9	-ECS	7	-DSEL	1	-DSEL
0x18[2]	8	-IDROM	8	-IDROM	8	-IDROM	8	-IDROM
|	|	|	|	|	|	|	|	|
0x1F	F	-IDROM	F	-IDROM	F	-IDROM	F	-IDROM

1. System address is relative to base I/O address selected by IOSEL<2:0>.
2. A write to any address in the range 0x18 - 0x1F will cause the PCBIU to reset the controller by asserting the reset pin. This feature provides a means for software resets.

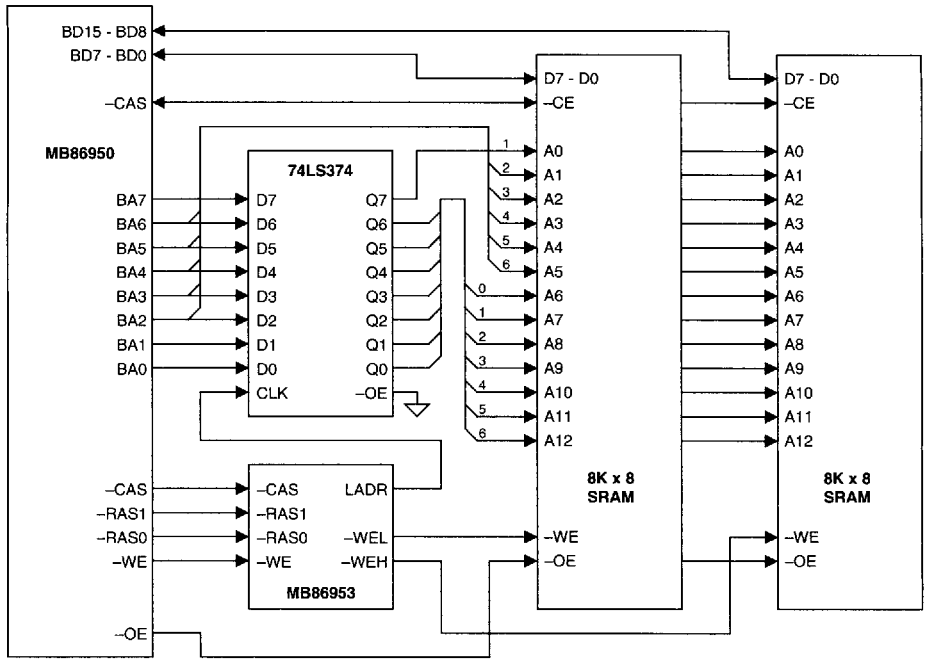


Figure 3. 16-Bit SRAM Buffer for MB86950 EtherStar

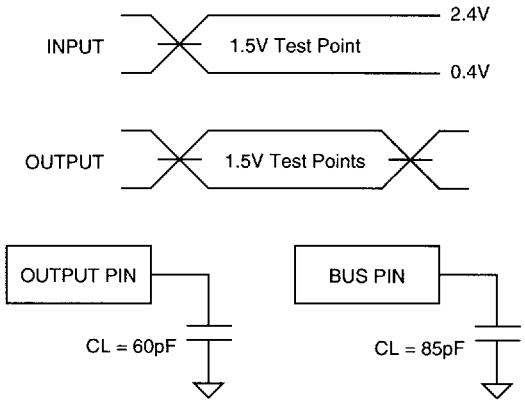


Figure 4. Test Conditions

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[1,4]

T-75-49

Symbol	Rating	Conditions	Min.	Max.	Units
V_{CC}	Supply voltage		-0.5	6	V
V_I	Input voltage[2]		-0.5	V_{CC} + 0.5	V
V_O	Output voltage		-0.5	V_{CC} + 0.5	V
T_{STG}	Storage temperature		-40	125	°C
T_{BIAS}	Temperature under bias		-25	85	°C
I_{OS}	Short circuit output current[5]	O3 output OD12 output OD24 output	-40 -60 -90	40 120 180	mA

DC SPECIFICATIONS[3,4] T_A = 0°C to +70°C, V_{CC} = 5V ± 5%

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{IL}	Input low voltage			0.8	V
V_{IH}	Input high voltage		2.2		V
V_{OL}	Output low voltage O3, B3 outputs OD12 outputs OD24, B24 outputs	 I_{OL} = 3.2mA I_{OL} = 12mA I_{OL} = 24mA	 0 0 0	 0.4 0.4 0.5	 V V V
V_{OH}	Output high voltage O3, B3 outputs B24 outputs	 I_{OH} = -2mA I_{OH} = -8mA	 4.0 4.0	 V_{CC} V_{CC}	 V V
I_{LI}	Input leakage current	V_{IN} = 0 to V_{CC}	-10	10	µA
I_{LZ}	3-state leakage current	V_{IN} = 0 to V_{CC} 3-state condition	-10	10	µA
I_{CC}	Operating power supply current	V_{IN} = 0 or V_{CC} V_{IN} = 0.8V or 2.2V		6 75	mA mA
I_{CCS}	Steady state power supply current	V_{IN} = V_{CC}	0	500	µA
R_P	Input pull-up resistor, IP inputs	V_{IN} = 0 or V_{CC}	25	100	kΩ

CAPACITANCE

Symbol	Parameter	Conditions	Min.	Max.	Units
C_{IN}	Input pin capacitance	T_A = 25°C V_{CC} = 0 V_{IN} = 0 f = 1 MHz		16	pF
C_{OUT}	Output pin capacitance O3, OD12 outputs OD24 outputs			 16 18	 pF pF
$C_{I/O}$	I/O pin capacitance B3 outputs B24 outputs			 16 23	 pF pF

AC CHARACTERISTICS[3,4,6] T_A = 0°C to +70°C, V_{CC} = 5V ± 5%

T-75-49

Write Cycle Timing - Reference Figure 5.

Symbol	Parameter	Parameter Description	Min.	Typ.	Max.	Units
t1	t_{ADVIOH}	SADR, AEN valid to –IO16 high			53	ns
t2	t_{ADVLAV}	SADR, AEN valid to LSADR<3:0> valid			22	ns
t3	t_{WRLCRL}	–IOW low to IOCHRDY1, 2 low			22	ns
t4	t_{WRLIDV}	–IOW low to IDATA<7:0> active and valid			36	ns
t5	t_{WRLDSL}	–IOW low to –DSEL low			29	ns
t6	t_{WRLRSL}	–IOW low to –RSEL/–ECS low			33	ns
t7	t_{WRLTEL}	–IOW low to –TOE low			29	ns
t8	t_{CKHWRL}	SYSCLK high to –WRITE low			29	ns
t9	t_{RYLCRH}	–READY low to IOCHRDY1, 2 high			34	ns
t10	t_{CKHZWL}	SYSCLK high to –ZWS low			35	ns
t11	t_{WRHZWH}	–IOW high to –ZWS high			47	ns
t12	t_{WRHIDF}	–IOW high to IDATA<7:0> three-state			38	ns
t13	t_{WRHWRH}	–IOW high to –WRITE high			19	ns
t14	t_{WRHDSH}	–IOW high to –DSEL high			23	ns
t15	t_{WRHRSH}	–IOW high to –RSEL/–ECS high			23	ns
t16	t_{WRHTEH}	–IOW high to –TOE high			21	ns
t17	t_{ADIIOL}	SADR, AEN to –IO16 low			58	ns
t18	t_{ADILAI}	SADR, AEN to LSADR<3:0> not valid			29	ns

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.
2. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is recommended that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
3. Parameters are valid over specified temperature range and supply voltage range unless otherwise noted.
4. All voltage measurements are referenced to ground. All time measurements are referenced at input and output levels of 1.5V. For testing, all inputs swing between 0.4V and 2.4V. See Figure 4.
5. Not more than one output may be shorted at a time for a maximum duration of one second.
6. See Figure 4 for test conditions for outputs.

T-75-49

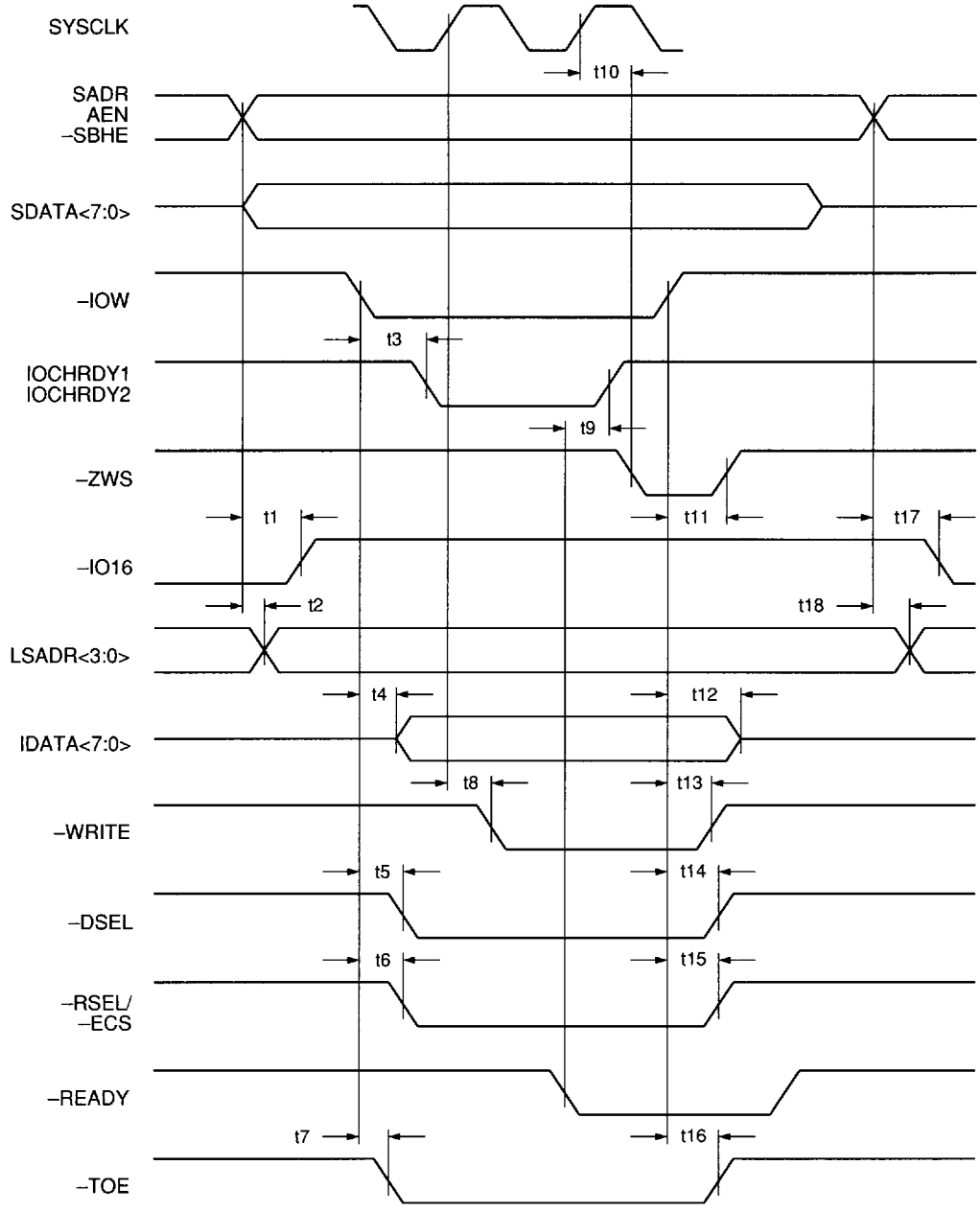


Figure 5. Write Cycle Timing

T-75-49

Read Cycle Timing - Reference Figure 6.

Symbol	Parameter	Parameter Description	Min.	Typ.	Max.	Units
t1	t_{ADVIOH}	SADR, AEN valid to –IO16 high			53	ns
t2	t_{ADVLAV}	SADR, AEN valid to LSADR<3:0> valid			22	ns
t3	t_{RDLSDA}	–IOR low to SDATA<7:0> enabled			39	ns
t4	t_{RDLCRL}	–IOR low to IOCHRDY1, 2 low			22	ns
t5	t_{RDLDSL}	–IOR low to –DSEL low			29	ns
t6	t_{RDLRSL}	–IOR low to –RSEL/–ECS low			33	ns
t7	t_{RDLTEL}	–IOR low to –TOE low			29	ns
t8	t_{CKHRDL}	SYSCLK high to –READ low			29	ns
t9	t_{RYLCRH}	–READY low to IOCHRDY1, 2 high			34	ns
t10	t_{CKHZWL}	SYSCLK high to –ZWS low			35	ns
t11	t_{RDHSDF}	–IOR high to SDATA<7:0> three-state			50	ns
t12	t_{RDHZWH}	–IOR high to –ZWS high			47	ns
t13	t_{RDHRDH}	–IOR high to –READ high			19	ns
t14	t_{RDHDSH}	–IOR high to –DSEL high			22	ns
t15	t_{RDHRSH}	–IOR high to –RSEL/–ECS high			25	ns
t16	t_{RDHTEH}	–IOR high to –TOE high			21	ns
t17	t_{ADIIOL}	SADR, AEN to –IO16 low			58	ns
t18	t_{ADILAI}	SADR, AEN to LSADR<3:0> not valid			29	ns
t19	t_{IDVSDV}	IDATA<7:0> valid to SDATA<7:0> valid			36	ns

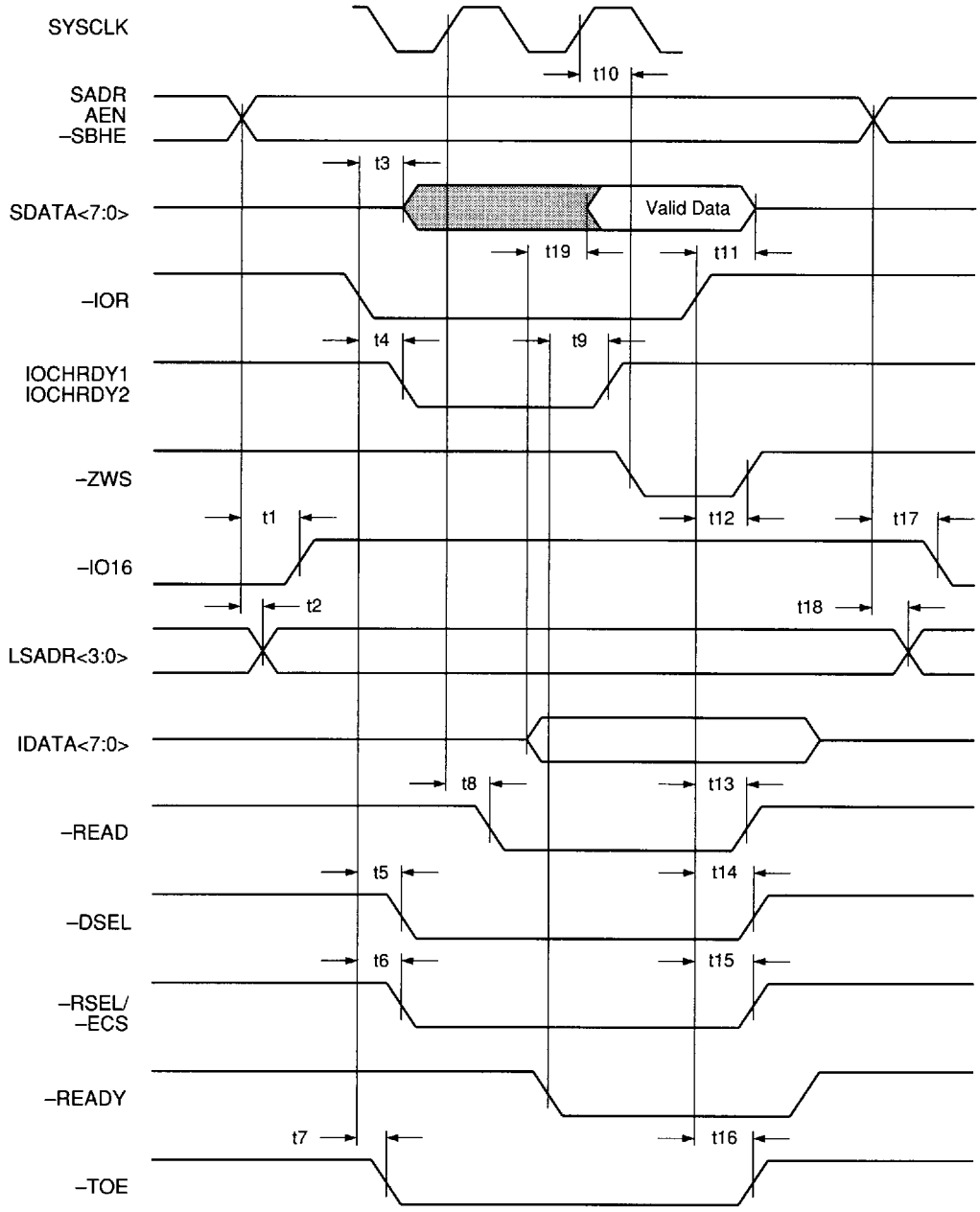


Figure 6. Read Cycle Timing

DMA Write Cycle Timing - Reference Figure 7.

Symbol	Parameter	Parameter Description	Min.	Typ.	Max.	Units
t1	t_{WRLIDV}	–IOW low to IDATA<7:0> active and valid			36	ns
t2	t_{WRLTEL}	–IOW low to –TOE low			29	ns
t3	t_{CKHWRL}	SYSCLK high to –WRITE low			29	ns
t4	t_{WRHIDF}	–IOW high to –IDATA<7:0> three-state			38	ns
t5	t_{WRHTEH}	–IOW high to –TOE high			21	ns
t6	t_{WRHWRH}	–IOW high to –WRITE high			19	ns

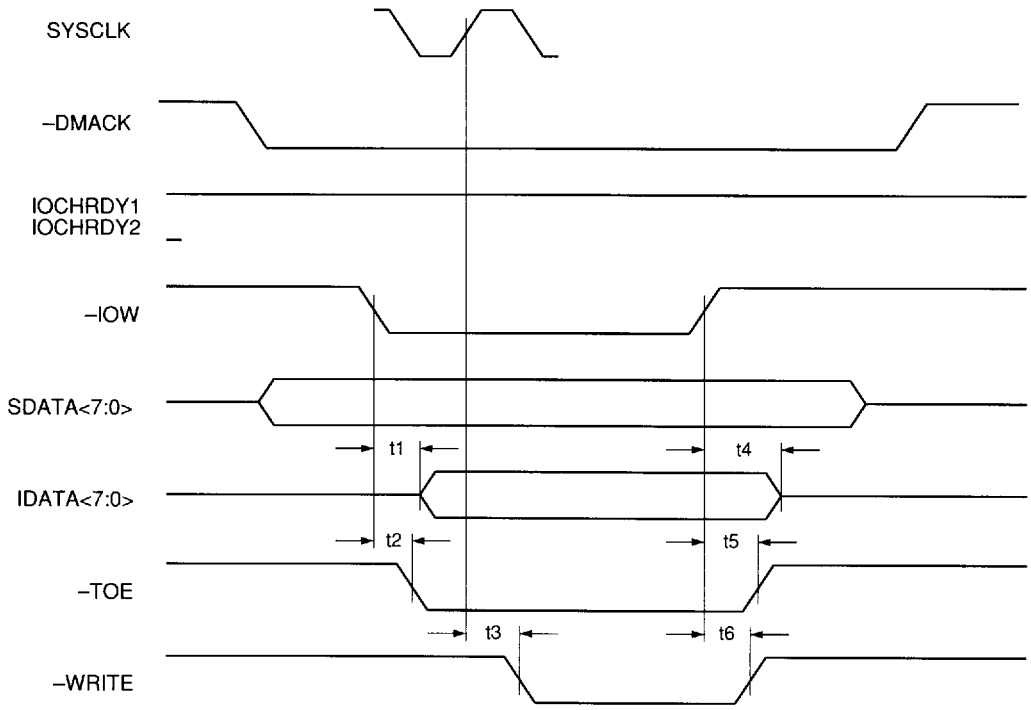


Figure 7. DMA Write Cycle Timing

DMA Read Cycle Timing - Reference Figure 8.

Symbol	Parameter	Parameter Description	Min.	Typ.	Max.	Units
t1	t_{RDLSDA}	–IOR low to SDATA<7:0> enabled			39	ns
t2	t_{RDLTEL}	–IOR low to –TOE low			29	ns
t3	t_{CKHRDL}	SYSCLK high to –READ low			29	ns
t4	t_{RDHSDF}	–IOR high to –SDATA<7:0> three-state			50	ns
t5	t_{RDHTEH}	–IOR high to –TOE high			21	ns
t6	t_{RDHRDH}	–IOR high to –READ high			19	ns
t7	t_{IDVSDV}	IDATA<7:0> valid to SDATA<7:0> valid			36	ns

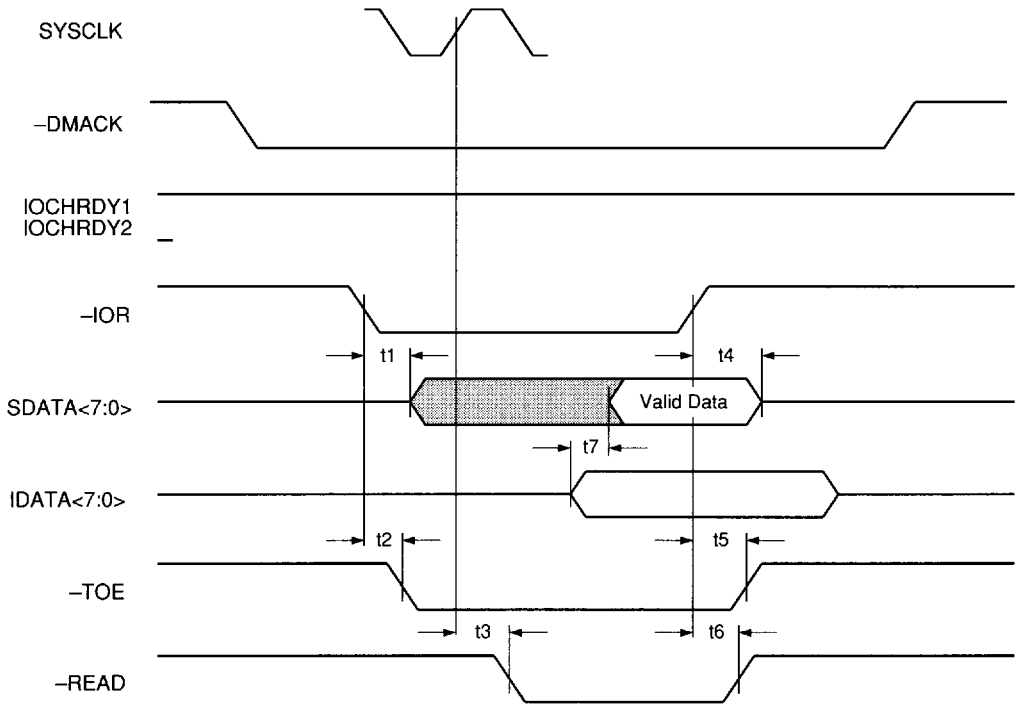


Figure 8. DMA Read Cycle Timing

DRAM to SRAM Signal Conversion Timing - Reference Figure 9.

Symbol	Parameter	Parameter Description	Min.	Typ.	Max.	Units
t1	t_{RALLAH}	–RAS0 or –RAS1 low to –LADR high			18	ns
t2	t_{BAVRAL}	BA<6:0> valid to –RAS0 low	45			ns
t3	t_{RALBAI}	–RAS0 low to BA<6:0> invalid	23			ns
t4	t_{CALWLL}	–CAS low to –WEL low			28	ns
t5	t_{CALWHL}	–CAS low to –WEH low			28	ns
t6	t_{WRHWLH}	–WE high to –WEL high			19	ns
t7	t_{WRHWHH}	–WE high to –WEH high			19	ns
t8	t_{RAHLAL}	–RAS0 and –RAS1 low to –ROUT low			24	ns
t9	t_{RALROL}	–RAS0 or –RAS1 low to –ROUT low			24	ns
t10	t_{RAHROH}	–RAS0 and –RAS1 high to –ROUT high			16	ns

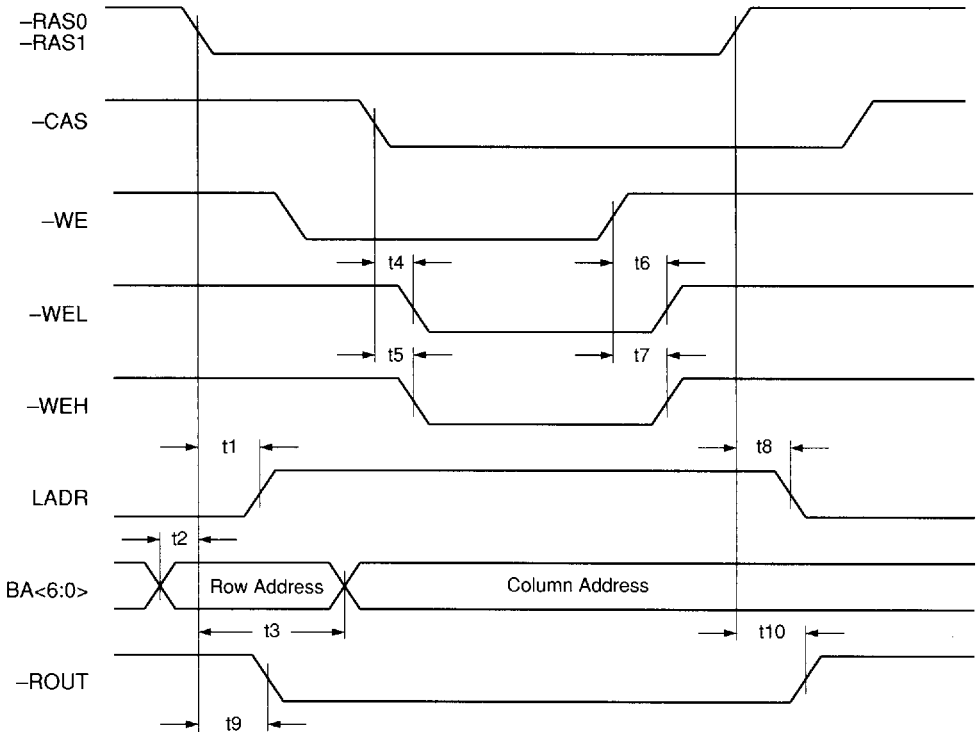


Figure 9. DRAM to SRAM Signal Conversion Timing