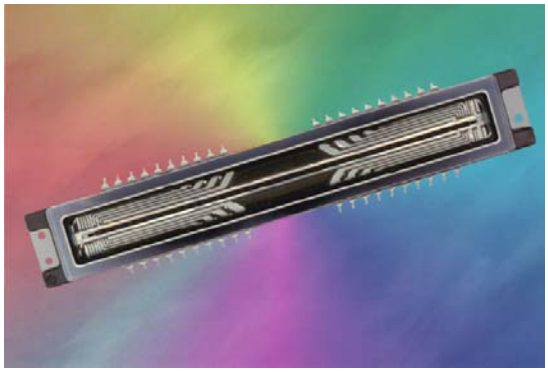
Kodak Digital Science KLI-14403 Image Sensor

Features

- Tri-Linear Color Array 3 x 14404 pixels
- 5um^2 pixels.
- 32 line spacing between color channels.
- Dual shift register per channel.
- Improved blue response filter
- Dark reference pixels provided.
- Antireflective glass standard.
- Wide dynamic range, low noise.
- No image lag.
- Electronic exposure control.
- High charge transfer efficiency.
- Two-phase register clocking.
- Clocks are 74ACT logic compatible.
- 10 MHz maximum data rate.

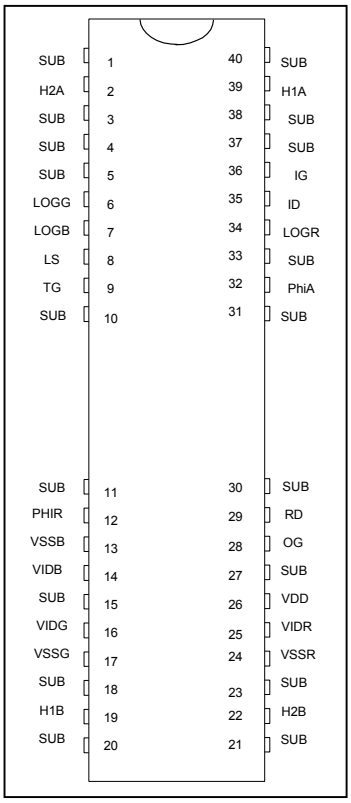


Typical Key Specifications

- Dynamic Range >12 bits
- Output Signal 2.7V
- Saturation Signal 250K electrons
- PRNU(med) 5%
- Lag (first field) 0.06%
- Dark Current 0.002pA/pixel (max.)
- CTE per transfer 0.999998
- No darkfield defects allowed
- No brightfield defects allowed

Pin Description

Symbol	Description	Pin
PhiA	Accumulation Phase Clock	32
TG	Transfer Gate Clock	9
LOGn	Exposure Control for Channel (R,G,B)	34,6,7
H1A,B	Phase 1 CCD Clock	19,39
H2A,B	Phase 2 CCD Clock	2,22
PHIR	Reset Clock	12
VIDn	Blue Output Video (R,G,B)	25,16,14
VDD	Amplifier Supply	26
VSSn	Ground Reference (R,G,B)	24,17,13
LS	Light Shield / Exposure Drain	8
OG	Output Gate	28
RD	Reset Drain	29
SUB	Substrate / Ground	1,3,4,5,10,11,15,18,20, 21,23,27,30,31,33,37, 38,40
ID	Test Input - Input Diode	35
IG	Test Input - Input Gate	36



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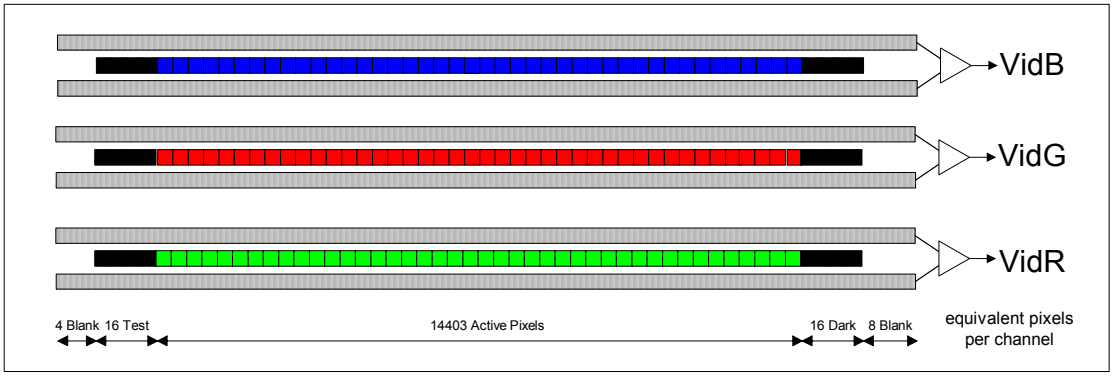
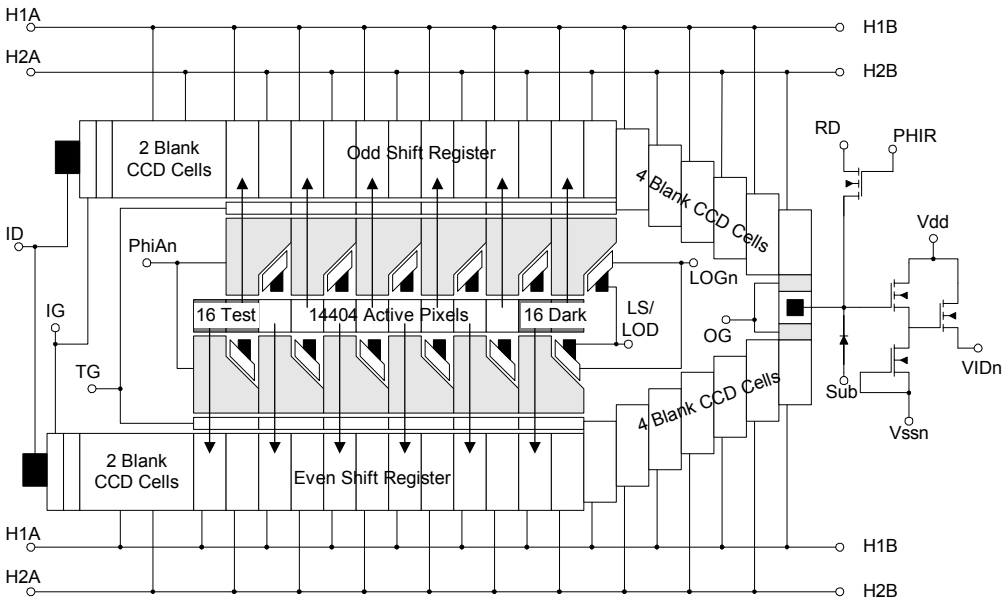
Block Diagram



Single Channel Schematic



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General Description

The KLI-14403 is a high resolution, tri-linear array designed for high resolution color scanning applications. Each device contains 3 rows of 14,404 active photoelements, consisting of high performance 'pinned diodes' for improved sensitivity, lower noise and the elimination of lag. The pixel height and pitch is 5 micron and the center-to-center spacing between color channels is 160 microns, giving an effective 32 line delay between adjacent channels during imaging.

Each row is selectively covered with a red, green or blue integral filter stripe for unparalleled spectral separation. Electronic exposure control is provided to achieve system color balance.

Readout of the pixel data for each channel is accomplished through the use of a single CCD shift register allowing for a single output per channel with no multiplexing artifacts. Sixteen light shielded photoelements are supplied at the output end of each channel to act as a dark reference.

The devices are manufactured using NMOS, buried channel processing and utilize dual layer polysilicon and dual layer metal technologies.

The die size is 76.89 mm X 1.06 mm and is housed in a custom 40-pin, 0.600" wide, dual in line package with AR coated cover glass.

The KLI-14403 device is a member of a family of Tri-Linear CCD imagers that can ease transitional designs between different resolution solutions. Other family of devices; KLI-10203 (10K pixel trilinear), KLI-8023 (8K pixel trilinear), the KLI-6013 (6K trilinear with improved color filters) and the KLI-6003 (6K trilinear) are designed for ease in transitional designs.

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Image Specifications

Specifications given under nominally specified operating conditions for the given mode of operation @ 25^{O}C, f_{CLK} = 500kHz (data rate = 1 MHz), 14.45 ms integration period, AR coverglass, color filters, and an active load as shown in Figure 4, unless otherwise specified. See notes on next page for further descriptions.

Symbol	Parameter	Min.	Nom.	Max.	Units	Remarks
Vsat	Saturation Output Voltage	2.2	2.7	- - -	Vp-p	Notes 1, 9
deltaVo/deltaNe	Output Sensitivity	- - -	10.8	- - -	µV/e-	
Ne,sat	Saturation Signal Charge	- - -	250,000	- - -	electrons	
R	Responsivity					Notes 2, 9, 10
	(@ 450 nm)	- - -	3.5	- - -	V/microJ/cm2	± 10 %
	(@ 550 nm)	- - -	4	- - -	V/microJ/cm2	± 10 %
	(@ 650 nm)	- - -	6.5	- - -	V/microJ/cm2	± 10 %
DR	Dynamic Range	- - -	78	- - -	dB	Note 3
Idark	Dark Current	- - -	0.002	0.10	pA/pixel	Note 4
CTE	Charge Transfer Efficiency	0.999995	0.999998	- - -	- - -	Note 5
L	Lag	- - -	0.06	0.1	%	1st Field
Vo,dc	DC Output Offset	6.0	7.5	9.0	Volts	Note 9
PRNU, Low	Photoresponse Non-Uniformity, Low Frequency	- - -	7.5	15	% p-p	Note 6
PRNU, Med	Photoresponse Non-Uniformity, Medium Frequency	- - -	5	10	% p-p	Note 7
PRNU, High	Photoresponse Non-Uniformity, High Frequency	- - -	10	20	% p-p	Note 8
Dark Def	Darkfield Defect, brightpoint	- - -	- - -	0	Allowed	Notes 11,12
Bfld Def	Brightfield Defect, dark or bright	- - -	- - -	0	Allowed	Notes 11,13
Exp Def	Exposure Control Defects	- - -	30	64	Allowed	Notes 11,14
BW	Amplifier Bandwidth	- - -	57	- - -	MHz	
Rout	Output Resistance	- - -	300	- - -	Ohms	
delta OE	Odd-Even Offset	- - -	- - -	20	mV	
delta OE dark variance	Odd Even Offset Variance (Dark)	- - -	- - -	40	mV	
delta OE brt variance	Odd Even Offset Variance (Bright)	- - -	- - -	40	mV	

Image Specification Notes

1 Defined as the maximum output level achievable before linearity or PRNU performance is degraded beyond specification

2. With color filter. Values specified at filter peaks. 50% bandwidth = ±30 nm. Color filter arrays become transparent after 710 nm. It is recommended that a suitable IR cut filter be used to maintain spectral balance and optimal MTF. See chart of typical responsivity later in this document.

3. This device utilizes 2-phase clocking for cancellation of driver displacement currents. Symmetry between PHI1 and PHI2 phases must be maintained to minimize clock noise.

4. Dark current doubles approximately every +9°C.

5 Measured per transfer. For the total line: (.999995) * 14,436 = 0.9304.

6. Low frequency response is measured across the entire array with a 1000 pixel-moving window and a 5 pixel median filter evaluated under a flat field illumination.

7. Medium frequency response is measured across the entire array with a 50 pixel-moving window and a 5 pixel median filter evaluated under a flat field illumination.

8. High frequency response non-uniformity represents individual pixel defects evaluated under a flat field illumination. An individual pixel value may deviate above or below the average response for the entire array. Zero individual defects allowed per this specification.

9. Increasing the current load (nominally 4mA) to improve signal bandwidth will decrease these parameters.

10. If resistive loads are used to set current, the amplifier gain will be reduced, thereby reducing the output sensitivity and net responsivity.

11. Defective pixels will be separated by at least one non-defective pixel within and across channels.

12. Pixels whose response is greater than the average response by the specified threshold, (16mV). See line 1 in figure below.

13. Pixels whose response is greater or less than the average response by the specified threshold, (±20%). See lines 2 and 3 in figure below.

14. Pixels whose response deviates from the average pixel response by the specified threshold, (5mV), when operating in exposure control mode. See lines 4 and 5 in figure below. If dark pattern correction is used with exposure control, the dark pattern acquisition should be completed with exposure control actuated. Dark current tends to suppress the magnitude of these defects as observed in typical applications, hence line rate changes may effect perceived defect magnitude. Note: Zero defects allowed for those pixels whose response deviates from the average pixel response by a 20mV threshold.

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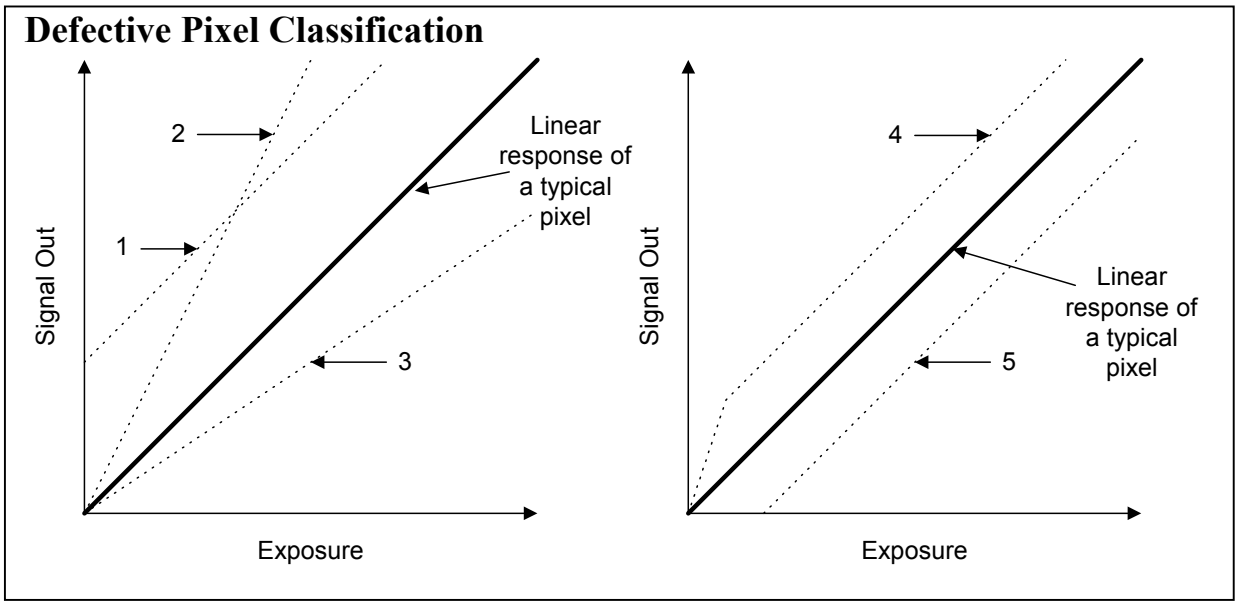


Notes:
1 – Dark Offset Error
2,3 - Brightfield Defects; bright (2), or dark (3)
4,5 - Exposure control mode defects, fast (4), or slow (5) pixels.

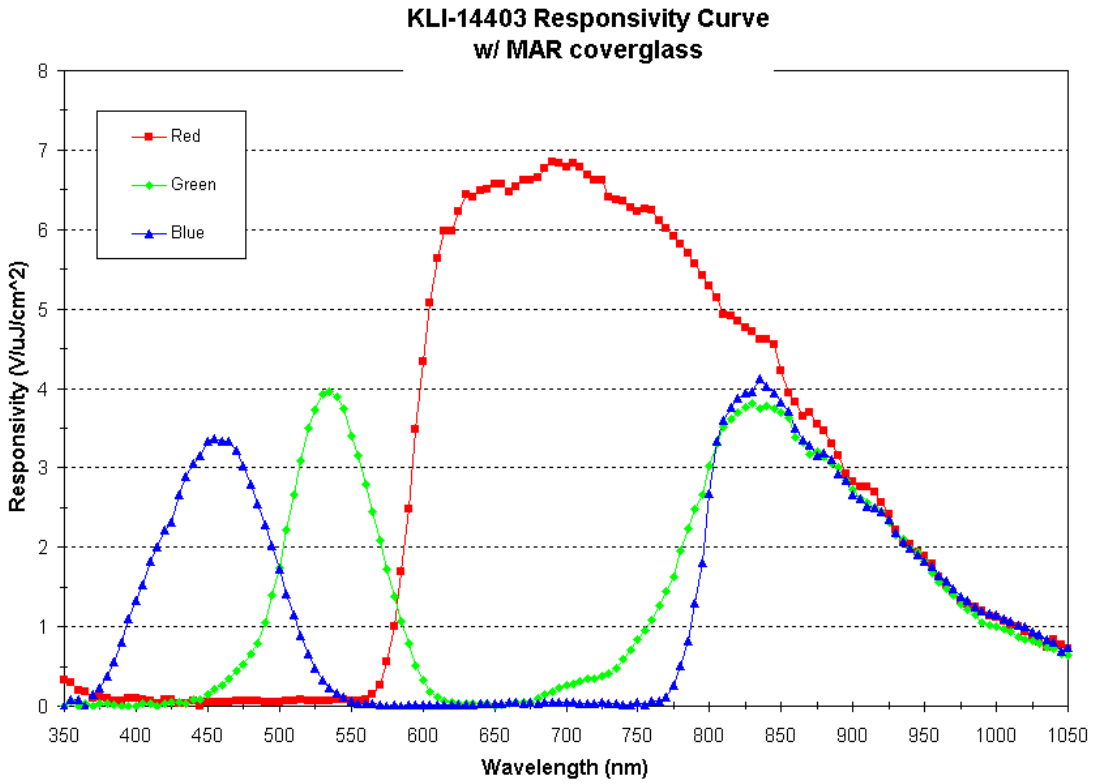
Color Filter Response and Description

A filter set has been implemented for a series of tri-linear image sensors optimized for color negative scanning. Values for the various nominal wavelength positions are shown below with corresponding tolerances for responsivity and wavelength as indicated. See Figure 1 for clarification of parameters.

Independent of filter type, a degree of variation in the spectral response for the KLI-series tri-linear image sensors can be expected from the natural manufacturing tolerances of the process. This variation is due to the combined variations in filter properties (net density and filter peak wavelength position) and the device properties (sensitivity and film thickness variations).

Values for gauging filter performance are determined from Figure 1. The center (or peak) transmission wavelength is specified as lambda0, and the 50% points are given as lambda1 and lambda2, corresponding to the near and far wavelength sides of the filter pass band.

For the red filter, only the near wavelength value is presented. The red filter, as well as the blue and green filters, exhibits a high level of transmission beyond the 700nm (i.e., the filters become transparent). The far wavelength edge is assumed controlled by the system IR cut filter characteristics.



Filter Variation Parameters Color Image Sensors

Filter	Parameter	Wavelength (nm) (typical)	Responsivity Tolerance 3 sigma	Wavelength Tolerance (nm) (typical)
Green	Lambda 0,g	535	± 12%	± 8
	Lambda 1,g	506	-	± 8
	Lambda 2,g	577	-	± 8
Blue	Lambda 0,b	462	± 12%	± 8
	Lambda 1,b	413	-	± 8
	Lambda 2,b	505	-	± 8
Red	Lambda 0,r	650	± 12%	
	Lambda 1,r	598	-	± 8

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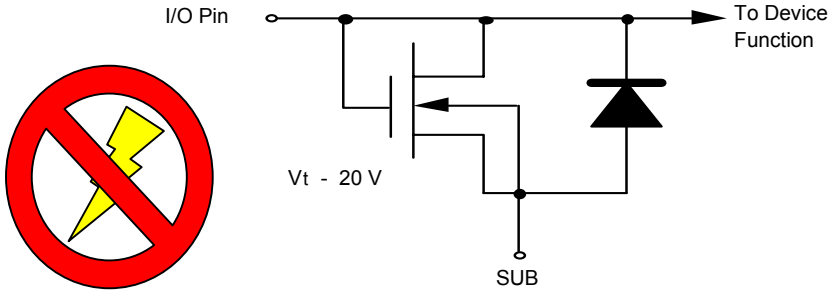
Absolute maximum Ratings (Note 10)

Parameter	Symbol	Min.	Max.	Units	Notes
Gate Pin Voltages	VGate	0	16	V	1, 2
Pin-to-Pin Voltage	VPin-Pin		16	V	1, 3
Diode Pin Voltages	VDiode	-0.5	16	V	1, 4
Output Bias Current	IDD	-10	-1	mA	5
Output Load Capacitance	CVID,Load		10	pF	9
CCD Clocking Frequency	fclk		5	MHz	6
Operating Temperature	TOP	0	70	°C	7
Storage Temperature	TST	-25	80	°C	8

Notes:

1. Referenced to substrate voltage.
2. Includes pins: H1n, H2n, TG1, PHIA, PHIR, OG, IG, and LOGn.
3. Voltage difference (either polarity) between any two pins.
4. Includes pins: VIDn, VSSn, RD, VDD, LS and ID.
5. Care must be taken not to short output pins to ground during operation as this may cause permanent damage to the output structures.
6. Charge transfer efficiency will degrade at frequencies higher than the maximum clocking frequency. VIDn load resistor values may need to be decreased as well.
7. Noise performance will degrade with increasing temperatures.
8. Long term storage at the maximum temperature may accelerate color filter degradation.
9. Exceeding the upper limit on output load capacitance will greatly reduce the output frequency response. Thus, direct probing of the output pins with conventional oscilloscope probes is not recommended.
10. The absolute maximum ratings indicate the limits of this device beyond which damage may occur. The Operating ratings indicate the conditions that the device is functional. Operating at or near these ratings do not guarantee specific performance limits. Guaranteed specifications and test conditions are contained in the Image Specifications section.

Device Input ESD Protection Circuit (schematic)



CAUTION:
To allow for maximum performance, this device was designed with limited input protection; thus, it is sensitive to electrostatic induced damage. These devices should be installed in accordance with strict ESD handling procedures!

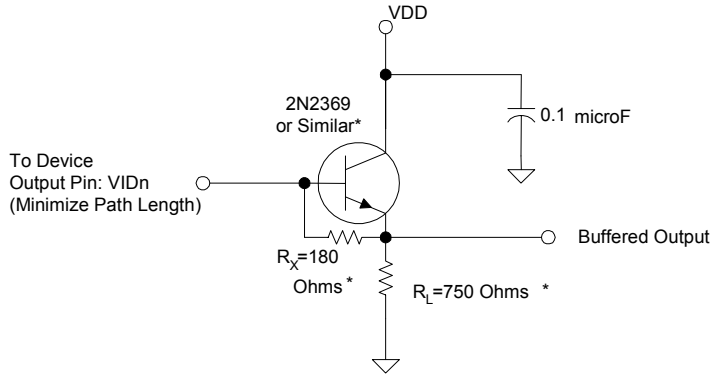
DC Bias Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Units	Notes
V_{SUB}	Substrate	-----	0	-----	V	
V_{VSS}	Output Buffer Return	0.5	0.65	0.75	V	
V_{RD}	Reset Drain Bias	10.5	11	11.5	V	
V_{VDD}	Output Buffer Supply	14.5	15	15.5	V	
I_{IDD}	Output Bias Current/Channel	-8	-4	-2	mA	1
V_{OG}	Output Gate Bias	0.5	0.65	0.75	V	
V_{PHIA}	Acummulation Phase Bias	-0.25	0	0.5	V	
V_{LS}	Light Shield / Drain Bias	12	15	15.5	V	
V_{IG}	Test Pin - Input Gate	-----	0	-----	V	
V_{ID}	Test Pin - Input Diode	12	15	15.5	V	

Notes:

1. A current sink must be supplied for each output. Load capacitance should be minimized so as not to limit bandwidth. Circuit below is just one solution.

Typical Output Bias/Buffer Circuit



*Rx serves as the load bias for the on-chip amplifiers. Choose the values of Rx and RL to optimize for specific operating frequency. Rx should not be less than 75 Ohms.

AC Electrical Characteristics – AC Timing Requirements (typical)

Symbol	Parameter	5MHz CCD operation	500KHz CCD operation	Units	Remarks
1e = 1/fCLK	CCD Element Duration	0.2	2	µs	1e count
trise	H1A/B, H2A/B Rise Time	20	200	ns	
1L = tint	Line/Integration Period	1.445	14.45	ms	7218e counts
tpd	PD-CCD Transfer Period	3.2	32	µs	16e counts
ttg	Transfer Gate Clear	0.2	2	µs	1e count
tdr	Charge Drain Duration	100	1000	ns	Note 2
trst	Reset Pulse Duration	20	--	ns	
tcd	Clamp to H2 Delay	8	--	ns	Note 1
tsd	Sample to Reset Edge Delay	8	--	ns	Note 1

Notes:

1. Recommended delays for Correlated Double Sampling (CDS) of output.
2. Minimum value required to ensure proper operation, allowing for on-chip propagation delay.

AC Electrical Characteristics – AC Timing Requirements

Symbol	Parameter	Min.	Nom.	Max.
VH1nH,VH2nH	CCD Readout Clocks High	6.25	6.5	7.0
VH1nL,VH2nL	CCD Readout Clocks Low	-0.1	0.0	0.1
VTGnH	Transfer Clocks High	6.25	6.5	7.0
VTGnL	Transfer Clocks Low	-0.1	0.0	0.1
VPHIRH	Reset Clock High	6.25	6.5	7.0
VPHIRL	Reset Clock Low	-0.1	0.0	0.1
VLOGnH	Exposure Clocks High	6.25	6.5	7.0
VLOGnL	Exposure Clocks Low	-0.1	0.0	0.1

Notes:

1. Care should be taken to insure that low rail overshoot does not exceed -0.5 VDC. Exceeding this value may result in non-photogenerated charged being injected into the video signal.
2. Connect pin to ground potential for applications where exposure control is not required.

Clock Line Capacitance

Symbol	Parameter	Min.	Nom.	Max	Units	Notes
C_{H1}	Phase 1 Clock Capacitance	--	1940	--	pF	1
C_{H2}	Phase 2 Clock Capacitance	--	2010	--	pF	1
C_{TG1}	Transfer Gate 1 Capacitance	--	680	--	pF	
C_{PHIR}	Reset Gate Capacitance	--	12	--	pF	
C_{LOG}	Exposure Gate Capacitance	--	140	--	pF	(1 of 3)

Notes:

1. This is the total load capacitance per CCD phase. Since the CCDs are driven from both ends of the sensor, the effective load capacitance per drive pin is approximately half the value listed.

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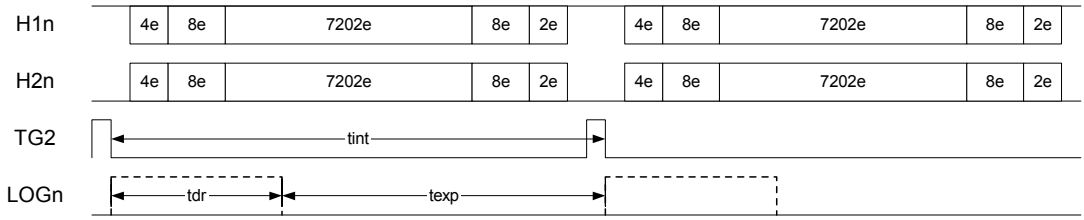
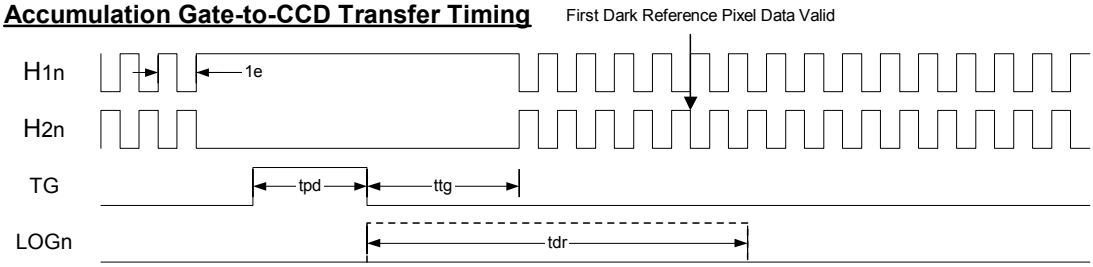
Timing Diagram

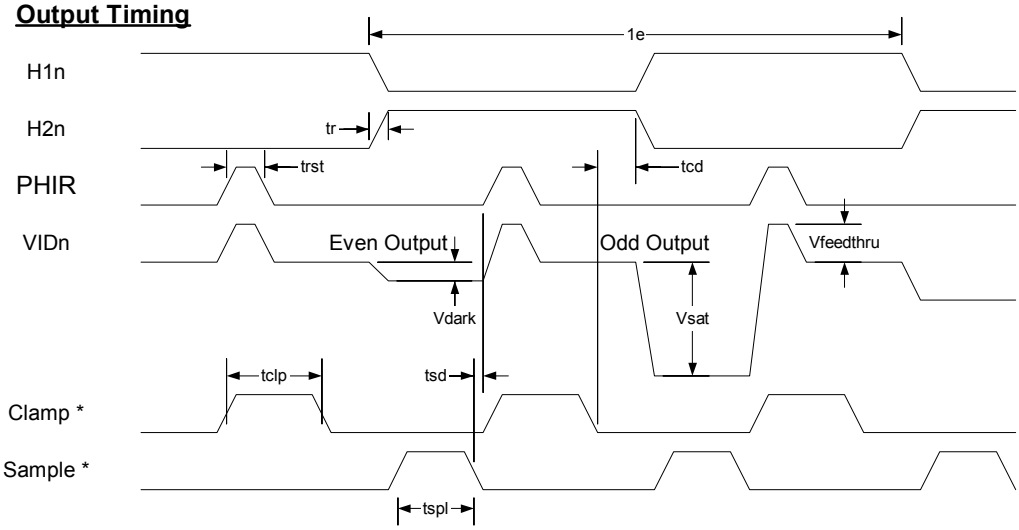
Line Timing



Accumulation Gate-to-CCD Transfer Timing



Output Timing



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KLI-14403 Functional Description

Imaging

During the integration period, an image is obtained by gathering electrons generated by photons incident upon the photodiodes. The charge collected in the photodiode array is a linear function of the local exposure. The charge is stored adjacent the photodiode in the accumulation region PHIA, and is isolated from the CCD shift registers during the integration period by the transfer gates TGn, which are held at a barrier potential. At the end of a given integration period, the CCD register clocking is stopped with the H1 and H2 gates being held in a 'high' and 'low' state respectively. Next, the TG gate is turned 'on' causing the charge to drain from the PHIÅ region, into the TG region. As the TG gate is turned to an 'off' state, charge is transferred into the H1 storage region, isolating the shift registers from the detector region once again. Complementary clocking of the H1 and H2 phases is then resumed for readout of the current line of data while the next line of data is integrated. Separate TG gates are provided for each channel allowing for independent transfer to the shift register, for each channel. However, the parallel connection of the shift register clocks requires that H1/H2 clocking of all three channels be momentarily suspended, during the parallel transfer from any channel photosites.

Charge Transport and Sensing

Readout of the signal charge is accomplished by two-phase, complementary clocking of the $H1$ and $H2$ gates. The register architecture has been designed for high speed clocking with minimal transport and output signal degradation, while still maintaining low (6.25V_{p-p} min) clock swings for reduced power dissipation, lower clock noise and simpler driver design. The data in all registers is clocked simultaneously toward the output structures. The signal is then transferred to the output structures in a parallel format at the falling edge of the $H2$ clock. Re-settable floating diffusions are used for the charge-to-voltage conversion while source followers provide buffering to external connections. The potential change on the floating diffusion is dependent on the amount of signal charge and is given by $dV_{FD} = dQ/C_{FD}$. Prior to each pixel output, the floating diffusion is returned to the RD level by the reset clock, $PHIR$.

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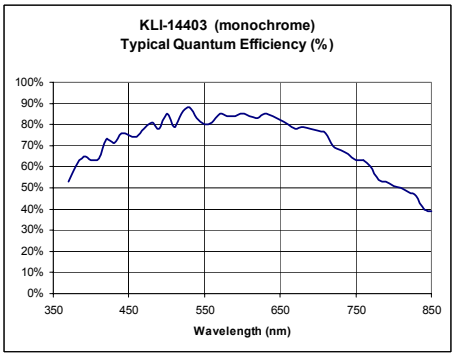
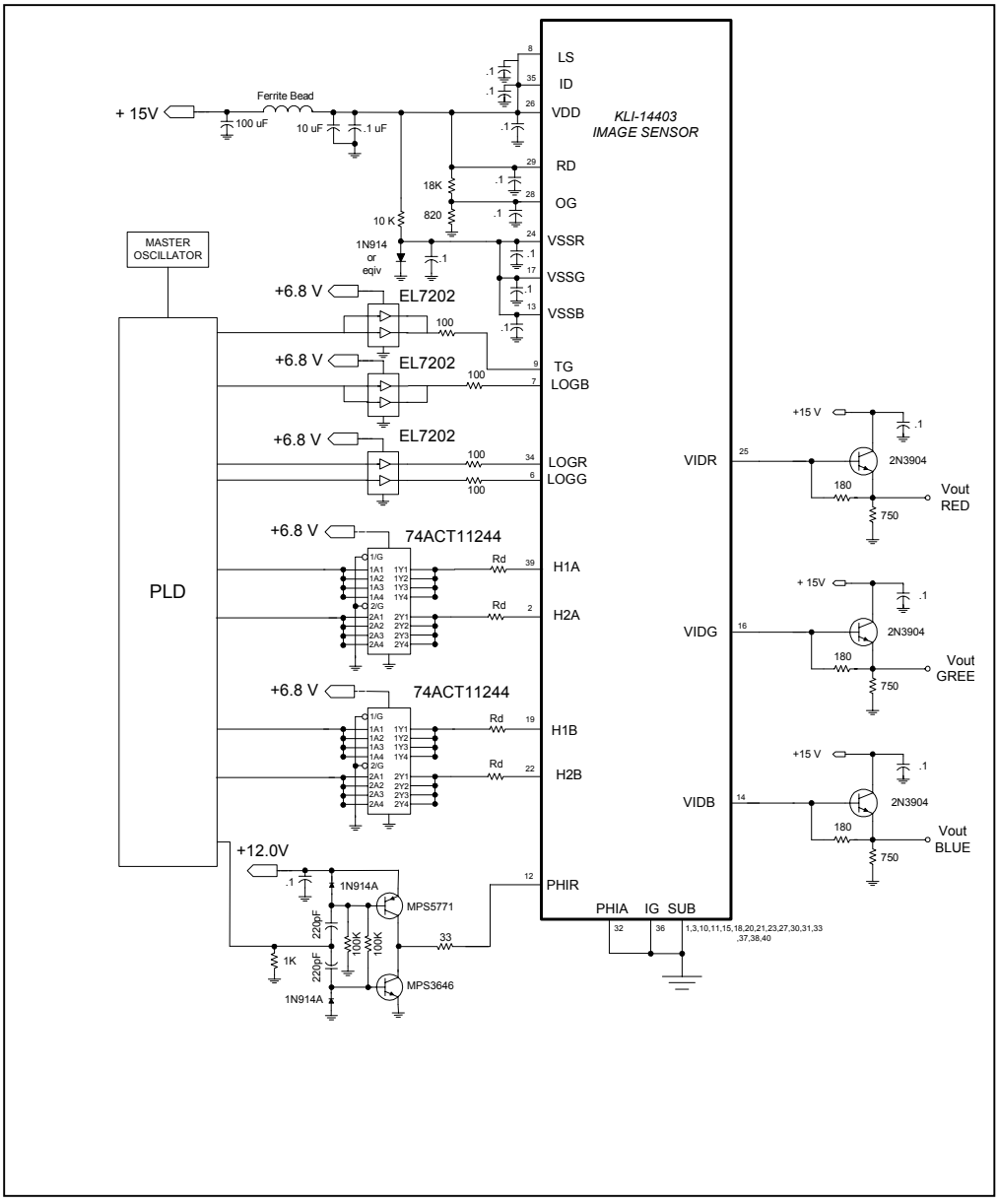
Typical Performance Measurements



KLI-14403 Reference Design

The Kodak KLI-14403 Reference Design provides a baseline reference for the design of a KLI-14403 image sensor into your electronic imaging application. The circuit below uses inexpensive off-the-shelf components to provide voltage-translated clock signals and DC bias supplies required to



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Reference Design Circuit Overview

Programmable Logic

See the timing waveform requirements earlier in this document before programming a logic device.

Clock Drivers

There are three types of clock drivers (voltage translating buffers) used in this reference design. The most important performance consideration is the ability of the clock driver to drive the capacitive loads presented by the various gates of the CCD.

Reset Driver

The RESET gate presents a small capacitive load of 100 pF, and requires fast rise and fall times. The complimentary bipolar switching transistor circuit shown above provides a low cost solution. The circuit alternately drives the PNP and NPN transistors into saturation, which switches the output between VCC and ground. A 33-ohm series damping resistor is used to suppress ringing.

Exposure Control and Transfer Gates

The exposure control gates; LOGR, LOGG, and LOGB, and the transfer gate; TG each present a moderate capacitive load of 500 pF. The Elantec 7202 Dual-Channel Power MOSFET driver delivers a peak output current of 2 amperes - more than enough to meet the rise and fall requirements of the LOG and TG gate. Series damping resistors are used to prevent ringing in the LOG gates. The transfer gates are connected together and driven by a single EL7202.

CCD Shift Register Driver

The CCD clock phases (H1A, H2A, H1B and H2B) present a significant load of 3100 pF per phase. Two 74ACT11244 octal buffers provide an efficient solution. Each clock phase is driven by four gates connected in parallel to increase output drive current. The 6.5-volt swing required by the shift register is obtained by setting VCC to 6.8 volts. Series damping resistors Rd are used to suppress ringing of the clock signals. Values for Rd should be varied to eliminate ringing and achieve 50% crossover between each pair of shift register clocks.

Bias Supplies

VDD, RD and OG

VDD and VRD are supplied directly from the 15V input power supply and OG is supplied by a voltage divider. The input power should be sufficiently filtered to prevent noise from coupling into the output stage of the KLI-14403 through the VDD node. Current spikes in the VRD and VDD nodes, due to switching of the on-chip reset FET, are suppressed by the addition of a 0.1 uF decoupling capacitor to ground at each node. The decoupling capacitors should be located as close as possible to the pins of the CCD and should have a solid connection to ground. OG is also decoupled to suppress voltage spikes the output gate of the device. The OG node draws negligible current.

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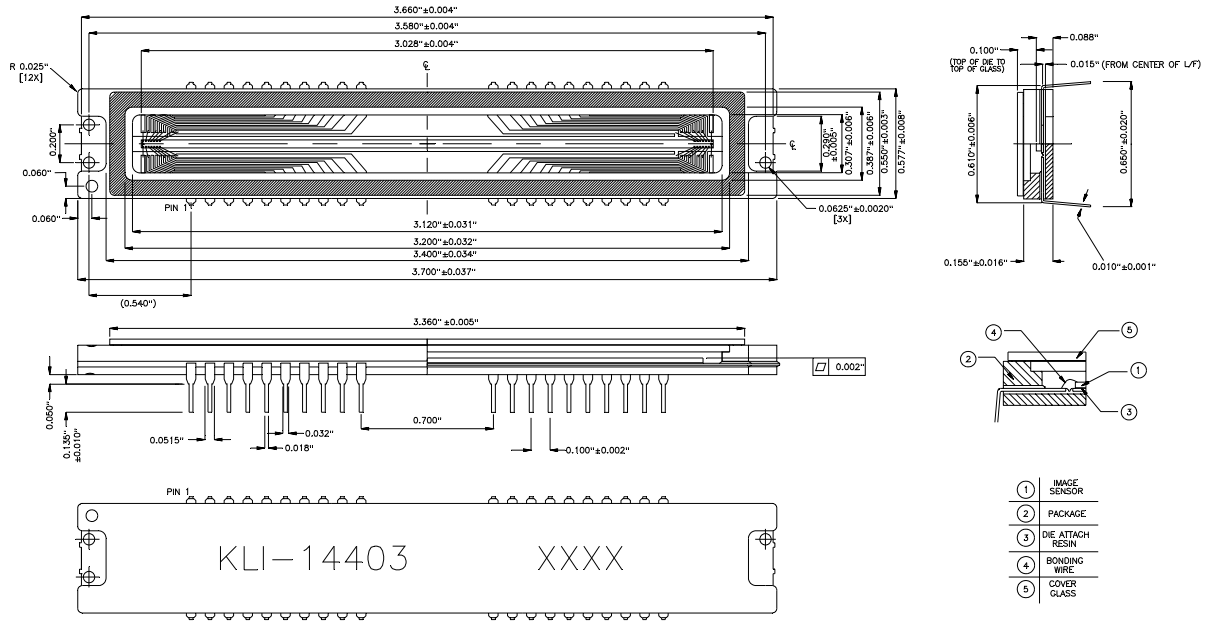
OG,VSSR,VSSG,VSSB, PHIA
A forward-biased diode provides an inexpensive and reliable voltage source for all three VSS nodes. The switching action of the reset FET of the output stage can cause voltage spikes to occur on the VSS nodes. A decoupling capacitor located as close as practical to each VSS pin, and connected to a solid system ground, will minimize voltage spiking. In high dynamic range systems, crosstalk between VSS channels might present a noise problem. A separate supply for each of the three VSS nodes will minimize channel crosstalk if it proves to be a problem.

Output Buffers

An emitter follower circuit buffers each output channel. The emitter follower provides a high impedance load to the on-chip source follower output stage, and provides low output impedance for driving the downstream analog signal processing circuits. A 180-ohm resistor connected between the base and emitter of the emitter follower uses the forward biased base to emitter voltage drop to provide a constant current load for the on-chip output stage.

Package Configuration



For the serialized version, a non-sequential, non-repeating serial number will be written on the back of the package.

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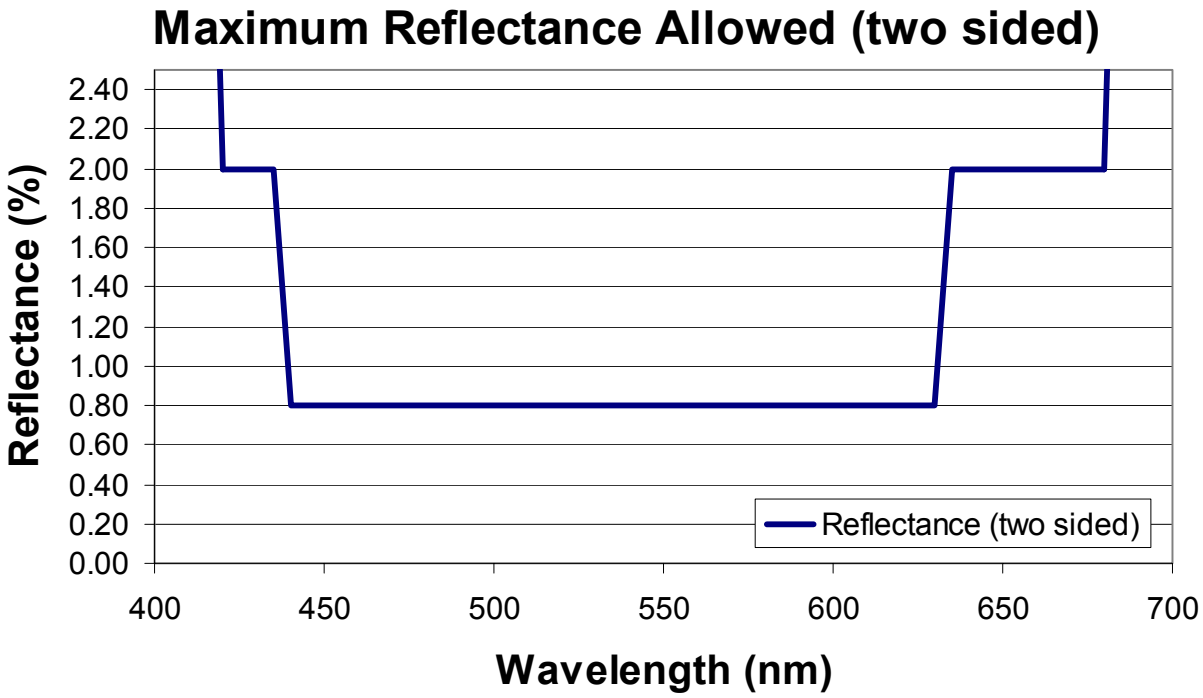
Two-Sided Multilayer Anti-Reflective Cover Glass Specification (MAR)



Eastman Kodak Company - Image Sensor Solutions
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General Device and Parameter Descriptions

Charge Transfer Efficiency

Charge Transfer Efficiency (CTE) is a measure of how efficiently electronic charge can be transported by a Charge Coupled Device (CCD). This parameter is especially important in linear imager technology due to the fact that CCDs are often required to transport charge packets over long distances at very high speeds. The result of poor CTE is to reduce the overall MTF of the line image in a nonlinear fashion: the portion of the line image at the far end of the CCD will be degraded more than the image at the output end of the CCD, since it will undergo more CCD transfers. There are many possible mechanisms that can negatively influence the CTE. Amongst these mechanisms are included excessive CCD clocking frequency, insufficient drive potential on the CCD clocking gates, and incorrect voltage bias on the output gate (OG signal). The effect of these mechanisms is that some charge is "left behind" during a CCD transfer clocking cycle. Depending on the limiting mechanism, the lost charge could be added to the immediate trailing cell or to a cell further back in time; thus, causing a horizontal smearing of the line image. The charge lost from a CCD cell, after being transferred out of the CCD, is measured with respect to the original charge level and is termed the charge transfer inefficiency (CTI). CTI is defined as

$$\mathrm{CTI} = \left(\frac{\text{Total Charge Lost}}{\text{Charge Injected in each Pixel}}\right) \times \left(\frac{1}{\text{Number of CCD Transfers}}\right).$$

The efficiency of the CCD transfer (CTE) is then defined as simply

$$\mathrm{CTE} = 1 - \mathrm{CTI}, \quad \text{or}$$

$$\mathrm{CTE} = 1 - \left(\frac{\text{Total Charge Lost}}{\text{Charge Injected in each Pixel}}\right) \times \left(\frac{1}{\text{Number of CCD Transfers}}\right).$$

Note that the total transfer efficiency for the entire line (TTE) is equal to $(\mathrm{CTE})^N$, where N is the total number of transfers which is equal to the number of phases per cell times the number of cells (n).

Dark Reference Pixels

Dark reference pixels are groups of photosensitive pixels covered by a metal light shield. These pixels are used as a black level reference for the image sensor output. Since the incident light is blocked from entering these pixels, the signal contained in these pixels is due only to dark current. It is assumed that each photosensitive pixel (active and dark reference) will have approximately the same dark signal; thus, subtracting the average dark reference signal from each active pixel signal will remove the background dark signal level. Dark reference pixels are typically located at one or both ends of the arrays, as shown earlier in this document for a linear image sensor in the single channel schematic.

Dark Signal Evaluation

The dark signal evaluation measures the thermally generated electronic current (i.e.

background noise signal) at a specific operating temperature. Dark current is measured will all incident radiation removed (i.e. imager is in the dark). The current measured by the picoammeter is the dark current of the photodiode array plus the dark current of the CCD array. Multiplying the dark current by the total integration time yields the quantity of dark charge. And dividing the dark current by the number of photodiodes yields the dark current per photodiode (I_{Dark}). Dark voltage increases linearly with integration time, the worst case value occurs at the slowest clocking frequency. Additionally, dark current doubles for approximately every 9°C increase in temperature.

Dynamic Range

Dynamic Range (DR) is the ratio of the maximum output signal, or saturation level, of an image sensor to the dark noise level of the imager. The dark noise level, or noise floor of an imager is typically expressed as the root mean square (rms) variation in dark signal voltage. The dark signal includes components from dark current within the photosite and CCD regions, reset transistor and output amplifier noise, and input clocking noise. An input referred noise signal in the charge domain can be calculated by dividing the dark noise voltage by the imager charge-to-voltage conversion factor. The dynamic range is typically expressed in units of decibels as: DR = 20 . LOG

Exposure Control

Exposure control is implemented by selectively clocking the LOG gates during portions of the scanning line time. By applying a large enough positive bias to the LOG gate, the channel potential is increased to a level beyond the 'pinning level' of the photodiode. (The 'pinning' level is the maximum channel potential which the photodiode can achieve and is fixed by the doping levels of the structure.) With TG in an 'off' state and LOG strongly biased, all of the photocurrent will be drawn off to the LS drain. Referring to the timing diagrams, one notes that the exposure can be controlled by pulsing the LOG gate to a 'high' level while TG is turning 'off' and then returning the LOG gate to a 'low' bias level sometime during the line scan. The effective exposure (texp) is the net time between the falling edge of the LOG gate and the falling edge of the TG gate (end of the line). Separate LOG connections for each channel are provided enabling on-chip light source and image spectral color balancing. As a cautionary note, the switching transients of the LOG gates during line readout may inject an artifact at the sensor output. Rising edge artifacts can be avoided by switching LOG during the photodiode-to-CCD transfer period, preferably, during the TG falling edge. Depending on clocking speeds, the falling edge of the LOG should be synchronous with the H1/H2 shift register readout clocks. For very fast applications, the falling edge of the LOG gate may be limited by on-chip RC delays across the array. In this case artifacts may extend across one or more pixels. Correlated double sampling (CDS) processing of the output waveform can remove the first order magnitude of such artifacts. In high dynamic range applications, it may be advisable to limit the LOG fall times to minimize the current transients in the device substrate and limit the magnitude of the artifact to an acceptable level.

Fixed Pattern Noise

If the output of an image sensor under no illumination is viewed at high gain a distinct non-uniform pattern, or fixed pattern noise, can be seen. This fixed pattern can be

removed from the video by subtracting the dark value of each pixel from the pixel values read out in all subsequent frames. Dark fixed pattern noise is usually caused by variations in dark current across an imager, but can also be caused by input clocking signals abruptly starting or stopping or by having the CCD clocks not being close compliments of each other. Mismatched CCD clocks can result in high instantaneous substrate currents, which when combined with the fact that the silicon substrate has some non zero resistance can result in the substrate potential bouncing. The pattern noise can also be seen when the imager is under uniform illumination. An imager which exhibits a fixed pattern noise under uniform illumination and shows no pattern in the dark is said to have Light pattern noise or Photosensitivity pattern noise. In addition to the reasons mentioned above, light pattern noise can be caused by the imager entering saturation, the nonuniform clipping effect of the antiblooming circuit, and by non-uniform, photosensitive pixel areas often caused by debris covering portions of some pixels.

Imager Responsivity

Responsivity is a measure of the imager output when exposed to a given optical energy density. It is measured on monochrome and color (if applicable) versions of an imager over the entire wavelength range of operation. Imagers having multiple photodiode arrays with differing color filters and/or photodiode dimensions have responsivity measured on each array

Lag

Lag, or decay lag is a measure of the amount of photogenerated charge left behind during a photodiode-to-CCD transfer cycle. Ideally, no charge is left behind during such transfers and lag is equal to zero; that is, 100% of the collected photogenerated charge is transferred to the adjacent CCD. The use of "pinned" photodiode technology enables the linear imagers to achieve near perfect lag performance. Improper Transfer Gate (TG) clocking levels can introduce a lag type response. Thus, care must be taken to ensure that the clocking levels are not limiting the lag performance.

Linearity

The non-linearity of an image sensor is typically defined as the percent deviation from the ideal linear response, which is defined by the line passing through Vsat and Vdark. The percent linearity is then 100 minus the non-linearity. The output linearity of a solid state image sensor is determined from the linearity of the photon collection process, the electron exposure structure nonlinearities (if it exists), the efficiency of charge transportation from the photosite to the output amplifier, and the output amplifier linearity. The absorption of photons within the silicon substrate can be considered an ideal linear function of incident illumination level when averaged over a given period of time. The existence of an electronic exposure control circuit adjacent to the photosensitive sites can introduce a non-linearity into the overall response by allowing small quantities of charge to remain isolated in unwanted potential wells. Whether or not any potential wells exist depends on the design and manufacturing of the particular image sensor. The existence of such potential wells in the exposure circuitry, also called exposure defects, will degrade the linearity only at small

signal levels and may be different from one photosite to the next. An image sensor with excessive exposure defects would be rejected during quality assurance testing. The loss of charge during the transportation of charge packets from the photosite to the CCD, which is termed lag, tends to effect the linearity only at very small signal levels. "Pinned" photodiodes, or buried photodiodes, have extremely small lag (< 0.5%), and can be considered to be lag free. The CCD charge transfer inefficiency (CTI) will reduce the amplitude of the charge packet as it is transported towards the output amplifier, with the greatest effect realized at very small signal levels. Modern CCD's have CTE in excess of 0.999999 per CCD transfer; thus, the overall effect on linearity is generally not a concern. If biased properly, the output amplifier will yield a nonlinearity of typically less than 2%. Non linearity at signal levels beyond the saturation level is expected and can often vary significantly from pixel to pixel.

Linearity Evaluation

Ideally, the output video amplitude should vary linearly with incident light intensity over the entire input range of irradiance. There are many possible phenomena which can cause non-linearity in the response curve; inadequate CTE and improper biasing or clocking to name a few.

Electronic exposure control could be used to vary the photodiode integration time; however, since electronic exposure control can introduce non-linearity, it is not recommended as a method of input signal variation. The output signal versus relative irradiance is graphed and a least-squares, linear regression fit to the data is performed. The best-fit data curve should pass through zero volts and remain linear ($R^2 > 0.99$) up to the Vsat level.

Modulation Transfer Function (MTF)

MTF is the magnitude of the spatial frequency response of a solid-state imager. The three main components of imager MTF are termed the aperture MTF, diffusion MTF, and charge transfer efficiency MTF. The aperture MTF results from the discrete sampling nature of solid state imagers, with smaller pixel pitches yielding a higher MTF response. The diffusion of photogenerated charge degrades the imager response and is responsible for the second component. The third component is due to inefficient charge transfer in the shift register. The maximum frequency an imager can detect without aliasing occurring is defined as the Nyquist frequency and is equal to one over two times the pixel pitch. MTF is typically reported at the Nyquist frequency, 1/2 Nyquist, and 1/4 Nyquist. The aperture MTF limits the maximum response at Nyquist to 0.637 (Note that the maximum MTF response is 1.0). The diffusion component will further degrade this value, especially at longer optical wavelengths.

Noise

Noise is any unwanted signal added to the imager output. Temporal noise sources present in a typical imager include the dark current, photon shot noise, reset transistor noise, CCD clocking noise, and the output amplifier noise. Dark current is dependent on the imager operating temperature and can be reduced by cooling the imager. The reset transistor noise can be removed using correlated double sampling signal processing. The photon shot noise cannot be eliminated; however, by acquiring and averaging several frames it, and all temporal noise sources, can be reduced. The variation in dark current from pixel to pixel

leads to a dark noise pattern across an imager. The effects of this dark pattern noise can be minimized by averaging several frames and then using the pixel-referenced, dark frame data as the zero reference level for each pixel.

Noise Evaluation

The noise evaluation measures the noise levels associated with operating the imager at the specified clocking speeds and temperatures. The test is performed with imager temperature held stable and all incident light is removed. The noise contributions of the evaluation circuitry need to be removed from the calculation. Once this is done, the total imager noise will be approximately equal to the sum of squares of each of the CCD clocking noise, output amplifier noise, and the dark current noise.

Photodiode Quantum Efficiency

For a given area, absolute quantum efficiency is defined as the ratio of the number of photogenerated electrons captured during an integration period to the number of impinging photons during that period. Higher values indicate a more efficient photon conversion process and hence are more desirable.

Absolute photodiode quantum efficiency is calculated from the charge-to-voltage, imager responsivity, and measured active photodiode area. It's calculated over the entire wavelength range of operation and graphed on a curve as percent Quantum Efficiency versus Wavelength.

Given that the charge-to-voltage, responsivity, and active photodiode dimensions have all been measured, the absolute quantum efficiency can be calculated as

$$\text{Quantum Efficiency } (\lambda) = \text{Responsivity } (\lambda) \div \text{Charge to Voltage} \div \text{Active Photodiode Area} \times \text{Energy per Photon } (\lambda)$$

where $$\text{Energy per Photon } (\lambda) = \frac{h \cdot c}{\lambda} \quad \text{and} \quad h \cdot c = 1.98647E-25 \ [J-m]$$

Care should be taken to ensure that all quantities are represented in similar units before any calculations are performed. Using the above formulas, the absolute quantum efficiency can be expressed as

$$QE(\lambda) = 100\% \times R(\lambda) \div \frac{dV}{dN_e} \div Area_{Diode} \times \frac{hc}{\lambda}.$$

Photoresponse Non-Uniformity (PRNU)

The measurement is taken in a flat field white light. The intensity of the collimated light is set to a value approximately 10% to 20% below the saturated signal level. Depending on the windowing length used, one region of pixels is observed for uniformity at a time. The average response is calculated for each non-overlapping windowed section. In the case of medium or low frequency PRNU measurements, a medium filter of 3-7 pixels is applied to this region to eliminate the effects of single point defects. The maximum and minimum pixel is determined for each windowed section. Again, for each section, the following formula is applied:

$$PRNU = 100\% \times \frac{(Maximum\_Pixel\_Value - Minimum\_Pixel\_Value)}{Mean\_Pixel\_Value}.$$

Each section is then compared against the specification to identify the region with the largest percent deviation from the average response for the imager.

Resolution

The resolution of a solid state image sensor is the spatial resolving power of that sensor. The spatial resolution of a sensor is descried in the spatial frequency domain by plotting the modulation transfer function (MTF) versus spatial frequency. The discrete sampling nature of solid state image sensors gives rise to a sampling frequency which will determine the upper limit of the sensor's frequency response. Resolution is frequently described in terms of the number of dots or photosites per inch (DPI) in the imager or object planes. For example, a linear image sensor with a single array of 1000 photosites of pitch 10 µm would have a resolution of 2540 DPI (1000 / (1000 x .01mm x 1"/25.4mm)). If the sensor is used in an optical system to image an 8" wide document, then the resolution in the document plane would be 125 DPI (1000 pixels / 8"). This example is slightly misleading in that it does not consider the frequency response of the sensor or the optics. In reality, the sensor will have an MTF of between 0.2 and 0.7 at the Nyquist spatial frequency and the optics are likely to have an MTF of 0.6 to 0.9 at the Nyquist frequency. It is important to note that even though a sensor may have a high enough sampling frequency for a particular application, the overall frequency response of the sensor and optics may not be sufficient for the application!

Saturation Voltage

The saturated signal level is the output voltage corresponding to the maximum charge packet the imager can handle. Adding charge above the saturated level results in the excess charge "spilling" over into neighboring photosites or CCD structures. Either the photodiode capacity or the CCD capacity, with the latter being the most typical case can limit the charge capacity. The saturated signal level is measured by monitoring the dark-to-light transition between the first-out dark reference pixels and the first active pixels while the irradiance is slowly increased. Note that improper settings on either the output gate (OG) or the reset gate (PHIR) can have a clipping effect on the output waveform.

Smear

Smear, also referred to as Photodiode-to-CCD Crosstalk, occurs when photogenerated charge diffuses to an adjacent CCD and is collected, as opposed to being collected in the photodiode where the photon absorption occurred. The result of smear is to increase the background signal within the dark reference pixels and CCD buffer pixels. This increased background signal reduces the achievable dynamic range; hence, a high smear value is undesirable. The further the photodiode array and the CCD are apart, the less the smear. Contributors to increased smear are a short photodiode-to-CCD separation and improper transfer gate clocking levels or timing. Smear is also highly dependent on incident photon wavelength. In the application, an IR cut-off filter (~710nm) is recommended.

Quality and Reliability

- Quality Strategy: All devices will conform to the maximum and minimum specifications stated in this document. This is accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target.
- Replacement: All devices are warranted against failures in accordance with the Terms of Sale.
- Cleanliness: Devices are shipped free of mobile contamination inside the package cavity. Immovable particles and scratches that are within the imager pixel area and the corresponding cover glass region directly above the pixel sites are also not allowed. The cover glass is highly susceptible to particles and other contamination. Touching the cover glass must be avoided. See ISS Application Note DS 00-009, Cover Glass Cleaning, for further information.
- Mechanical: Device assembly drawing is provided as a reference. The device will conform to the published package tolerances.
- ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe workstations.
- Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions, and can be supplied upon request.
- Test Data Retention: Devices have an identifying number traceable to a test data file. Test data is kept for a period of 2 years after date of shipment.

Ordering Information

Contact the Eastman Kodak Company for more information.

Address all inquiries and purchase orders to:

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Revision Changes

Revision Number	Description of Change
3.0	AC Electrical Characteristics – AC Timing Requirements table on page 10 corrected and updated for 5MHz and 500KHz operation. Eliminate reference to Color Filter Type II on page 7 – now only one type of filter.

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Ordering Options

Part Number	Description
KEK-4H0095-KLI-14403-12-5	Evaluation Board (Complete Kit)
KLI-14403-AAA-ED-AA	Monochrome, No Microlens, CERDIP Package (leadframe), Clear Cover Glass with AR coating (both sides), Standard Grade
KLI-14403-AAA-ED-AE	Monochrome, No Microlens, CERDIP Package (leadframe), Clear Cover Glass with AR coating (both sides), Engineering Sample
KLI-14403-DAA-ED-AA	Color (RGB), No Microlens, CERDIP Package (leadframe), Clear Cover Glass with AR coating (both sides), Standard Grade
KLI-14403-DAA-ED-AE	Color (RGB), No Microlens, CERDIP Package (leadframe), Clear Cover Glass with AR coating (both sides), Engineering Sample