W198

Caesar Clock Generator

Features

- **Three clock outputs**
- **Less than ± 250 ps cycle-to-cycle jitter**
- **Supports 3.3V to 5V operation**
- **TTL compatible logic: V_{IL} = 0.8V max., V_{IH} = 2.0V min., V_{OL} = 0.4V max. and V_{OH} = 2.4V min.**
- **OE pin has internal pull-up resistor**
- **45/55% duty cycle on all outputs**
- **40Ω output drivers**
- **Accepts 20MHz input reference**
- **Built-in crystal oscillator circuit. The load presented to the crystal is 12pF.**
- **Available in 16-pin SSOP (Shrink Small Outline Package)**

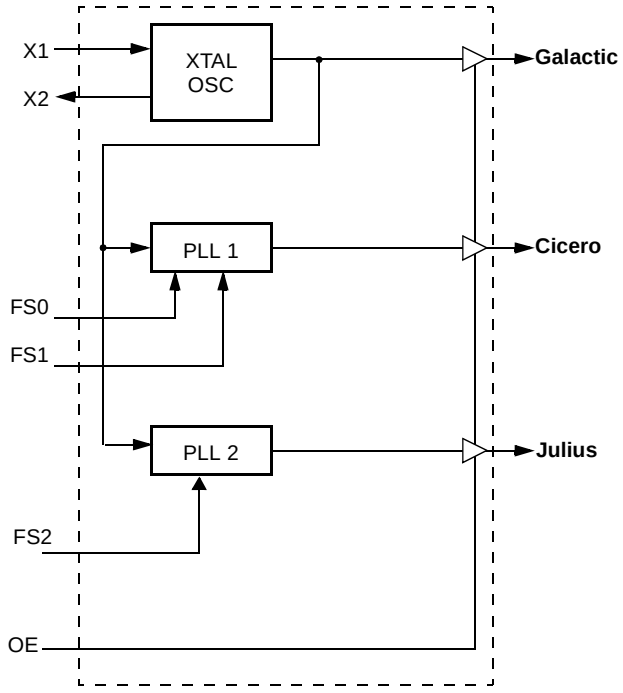
General Description

The W198 is designed to meet the needs of HPs “Caesar” DAT data storage system. Given a single crystal input frequency of 20 MHz, two PLLs are utilized to deliver all the required frequencies. A frequency decoder is utilized to select required outputs

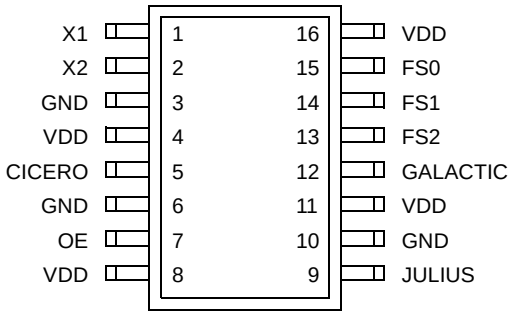
Table 1. Frequency Selection

FS2	FS1	FS0	Cicero	Julius	Galactic
X	0	0	108 MHz		
X	0	1	90 MHz		
X	1	0	54 MHz		
X	1	1	0 MHz		
0	X	X		60 MHz	
1	X	X		2.857 MHz	
X	X	X			20 MHz

Block Diagram



Pin Configuration



Pin Definitions[1]

Pin Name	Pin No.	Pin Type	Pin Description
OE	7	I	***Output Enable:*** When LOW, this input signal puts all outputs into a high-impedance state.
CICERO	5	O	***Clock Output:*** Refer to *Table 1* for frequency selection. Output voltage swing is set by VDD
JULIUS	9	O	***Clock Output:*** Refer to *Table 1* for frequency selection. Output voltage swing is set by VDD
GALACTIC	12	O	***Clock Output:*** Refer to *Table 1* for frequency selection. Output voltage swing is set by VDD.
FS0:1	15,14	I	***Frequency Selection Inputs 0 and 1:*** The FS0 (LSB) and FS1 (MSB) input signals are used to select the Cicero frequencies output. (See *Table 1* for frequency reference)
FS2	13	I	***Frequency Selection Input 2:*** The FS2 input signal is used to select the Julius frequency output. (See *Table 1* for frequency reference)
X1	1	I	***External Crystal Input:*** This pin has dual functions. It can be used as an external 20-MHz crystal connection or as an external reference frequency input.
X2	2	I	***External Crystal Output:*** An input connection for an external 20-MHz crystal. If using an external reference, this pin must be left unconnected.
VDD	4,8,11,16	P	***Power Supply Connections***: Connect all VDD pins to the same voltage, either 3.3V or 5.0V. Each VDD pin should have a decoupling capacitor (such as 0.1 µF) placed as close to the pin as possible.

Note:
1. All inputs, except X1 or X2, have an internal pull-up resistor. Unconnected inputs will assume a logic HIGH condition.

Power Supply Connections

The recommended single voltage power supply configuration for the W198 is shown schematically in *Figure 1*. These recommendations should be followed to both ensure adequate device performance and to control EMI. The major considerations can be summarized as follows:

1. Decoupling Capacitor—A 0.1-µF decoupling capacitor should be used for each VDD pin to minimize crosstalk between output frequencies. The trace to the VDD pin and to the ground via should be as short as possible.
2. Ferrite Bead (FB)—A common supply connection should be used for all W198 VDD pins. A ferrite bead should be used on this common supply as shown to remove high frequency system noise.
3. 22-µF Supply Filter Capacitor—The 22-µF capacitor filters low-frequency supply noise that may produce clock output jitter. Depending on the particular application, this capacitor may not be required; its use should be considered optional. Mounting pads should be implemented in PCB layout. Use of this capacitor in production should be determined upon prototype evaluation.
4. PCB power supply traces should be at least 20 mils wide to assure adequate trade impedance.

Ground Connections

All ground connections should be made to the main system ground plane. These connections should be as short as possible. No cuts should be made in the ground plane around the clock device since this can increase system EMI and reduce clock performance.

Clock Output Lines

1. The clock line width should be set to provide a 60Ω trace impedance. This width will vary depending on the PCB material; the PCB supplier can suggest what width to use for a 60Ω clock line. In general, an 8-mil trace will provide a 60Ω impedance on a multi-level board.
2. The series termination resistor (sometimes called “damping resistor”) must be placed in series with the clock line as close to the clock output as possible (within one inch).
3. Assume an output resistance from the W198 of 40Ω, choose series resistors appropriate to the number of driven traces.

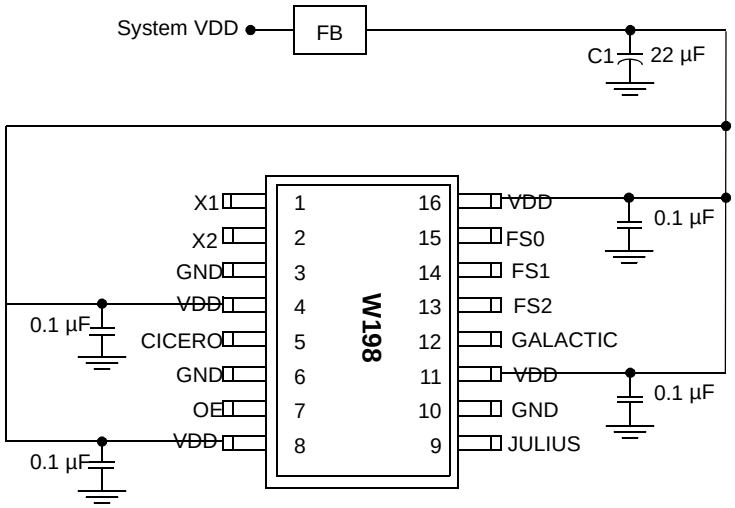


Figure 1. Test Circuit

Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. These represent a stress rating only. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability.

Parameter	Description	Rating	Unit
V_{DD}, V_{IN}	Voltage on Any Pin with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–65 to +150	°C
T_B	Ambient Temperature under Bias	–55 to +125	°C
T_A	Operating Temperature	0 to +70	°C

DC Electrical Characteristics: T_A = 0°C to +70°C, V_{DD} = 3.3V±5% or 5.0V±10%

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current	Note: Cicero CLK outputs = 108 MHz output loaded			50	mA
V_{IL}	Input Low Voltage	V_{CC} = 5.0V			0.8	V
V_{IH}	Input High Voltage	V_{CC} = 5.0V	2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 1 mA			50	mV
V_{OH}	Output High Voltage	I_{OH} = –1 mA	3.1			V
I_{IL}	Input Low Current				10	µA
I_{IH}	Input High Current				10	µA
R_P	Input Pull-up Resistor	V_{IN} = 0V		500		kΩ
C_I	Input Capacitance	Except X1 and X2			6	pF
L_I	Input Inductance	Except X1 and X2			7	nH
C_L	XTAL Load Capacitance	Total load to crystal		12		pF

AC Electrical Characteristics: T_A = 0°C to +70°C, V_{CC} = 3.3V±5% or 5.0V±10%[2]

Parameter	Description	Test Condition	Min.	Typ.	Max.	Unit
Clock Outputs						
t_{JC}	Output Clock Jitter, Cycle-to-Cycle			±175	±250	ps
Z_O	Output Buffer Impedance			40.0		Ω
d_T	Output Duty Cycle		45.0	50.0	55.0	%
t_R	Rise Time	Between 0.4V and 2.4V	0.6	1.0	1.5	ns
t_F	Fall Time	Between 2.4V and 0.4V	0.6	1.0	1.5	ns
t_{PU}	Stabilization Time from Power-Up	To within 0.1% of final frequency		1.5	3.0	ms
Freq_tt	Frequency Transition Time	pin 9 (Julius) pin 5 (Cicero)	0.342 0.362	0.36 0.381	0.378 0.40	MHz/µs
f_A	Long Term Output Frequency Stability[3]	Over V_{DD} and T_A range			0.01	%

Notes:

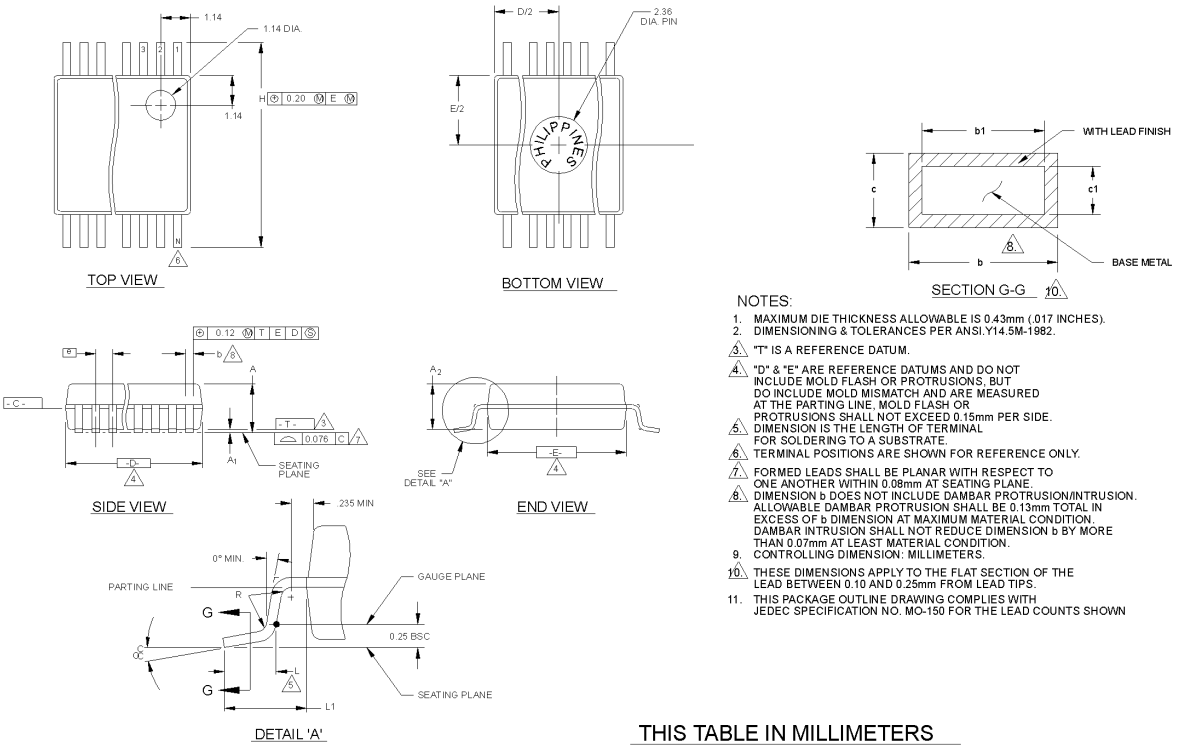
2. All AC tests are performed using the circuit shown in *Figure 1* to simulate typical system load conditions. Measurements are taken at the load. Threshold voltage for timing measurements is 1.5V.
3. Consideration of reference crystal shift only.

Ordering Information

Ordering Code	Package Name	Package Type
W198	H	16-pin SOIC (209 mil)

Package Diagram

16-Pin Shrink Small Outline Package (SSOP, 209 mils)



NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS 0.43mm (.017 INCHES).
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M-1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.08mm AT SEATING PLANE.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13mm TOTAL IN EXCESS OF b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION b BY MORE THAN 0.07mm AT LEAST MATERIAL CONDITION.
9. CONTROLLING DIMENSION: MILLIMETERS.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25mm FROM LEAD TIPS.
11. THIS PACKAGE OUTLINE DRAWING COMPLIES WITH JEDEC SPECIFICATION NO. MO-150 FOR THE LEAD COUNTS SHOWN

THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	1.73	1.86	1.99		AA	6.07	6.20	6.33	14
A_1	0.05	0.13	0.21		AB	6.07	6.20	6.33	16
A_2	1.68	1.73	1.78		AC	7.07	7.20	7.33	20
b	0.25	-	0.38	8,10	AD	8.07	8.20	8.33	24
b1	0.25	0.30	0.33	10	AE	10.07	10.20	10.33	28
c	0.09	-	0.20	10	AF	10.07	10.20	10.33	30
c1	0.09	0.15	0.16	10					
D	SEE VARIATIONS			4					
E	5.20	5.30	5.38	4					
e	0.65 BSC								
H	7.65	7.80	7.90						
L	0.63	0.75	0.95	5					
L1	1.25 REF.								
N	SEE VARIATIONS			6					
∝	0°	4°	8°						
R	0.09	0.15							

VARIATION AF
IS DESIGNED BUT NOT TOOLED

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE	4			6
	MIN.	NOM.	MAX.		VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	.068	.073	.078		AA	.239	.244	.249	14
A_1	.002	.005	.008		AB	.239	.244	.249	16
A_2	.066	.068	.070		AC	.278	.284	.289	20
b	.010	-	.015	8,10	AD	.318	.323	.328	24
b1	.010	.012	.013	10	AE	.397	.402	.407	28
c	.004	-	.008	10	AF	.397	.402	.407	30
c1	.004	.006	.006	10					
D	SEE VARIATIONS			4					
E	.205	.209	.212	4					
e	.0256 BSC								
H	.301	.307	.311						
L	.025	.030	.037	5					
L1	.049 REF.								
N	SEE VARIATIONS			6					
∝	0°	4°	8°						
R	.004	.006							

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REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	111391	02/25/02	IKA	Convert from ICW format to Cypress format New data sheet