Features

- **Operating Voltage: 5V**
- **Access Time: 40 ns**
- **Very Low Power Consumption**
  - **Active: 275 mW (Max)**
  - **Standby: 10 mW (Typ)**
- **Wide Temperature Range: -55·C to +125·C**
- **400 Mils Width Packages: FP32 and SB32**
- **TTL Compatible Inputs and Outputs**
- **Asynchronous**
- **No Single Event Latch-up below a LET Threshold of 80 MeV/mg/cm^2@125°C**
- **Tested up to a Total Dose of 300 krads (Si) according to MIL STD 883 Method 1019**
- **ESD better than 4000V**
- **Deliveries at least equivalent to QML procurement according to MIL-PRF38535**

Description

The AT65609EHV is a very low power CMOS static RAM organized as 131072 x 8 bits. Utilizing an array of six transistors (6T) memory cells, the AT65609EHV combines an extremely low standby supply current with a fast access time at 40 ns over the full military temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

The AT65609EHV is processed according to the methods of the latest revision of the MIL PRF 38535 or ESCC 9000.

It is manufactured on the same process as the MH1RT RAD-hard sea of gates series.

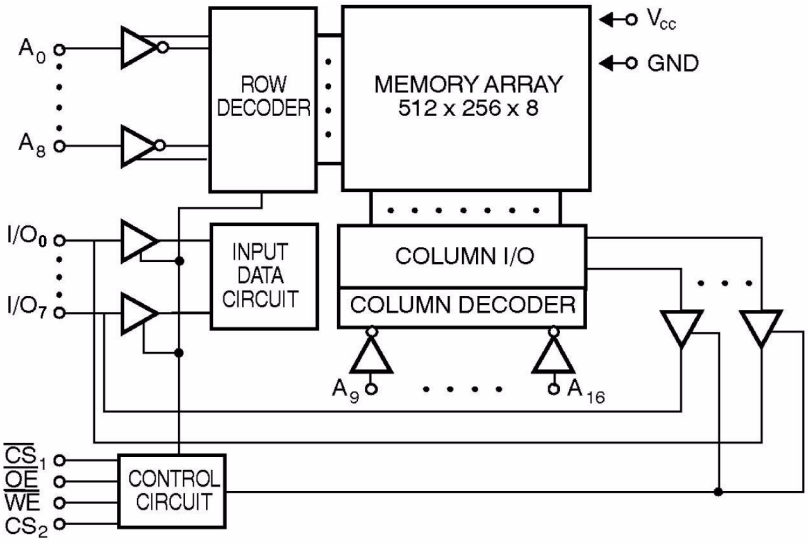
Rad. Tolerant 128K x 8 5-volts Very Low Power CMOS SRAM

AT65609EHV

PRELIMINARY

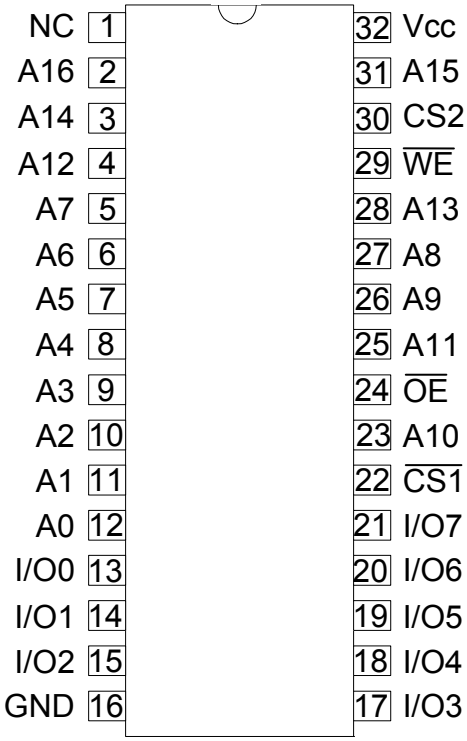
7832B–AERO–11/09

Block Diagram



Pin Configuration

32-lead DIL side-brazed or 32-lead Flat Pack - 400 Mils



Note: NC pin is not bonded internally. So, it can be connected to GND or VCC.

Pin Description

Table 1. Pin Names

Names	Description
A0 - A16	Address inputs
I/O0 - I/O7	Data Input/Output
$\overline{CS1}$	Chip select 1
CS2	Chip select 2
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	Power
GND	Ground

Table 2. Truth Table

$\overline{CS1}$	CS2	$\overline{WE}$	$\overline{OE}$	Inputs/ Outputs	Mode
H	X	X	X	Z	Deselect/Power-down
X	L	X	X	Z	Deselect/Power-down
L	H	H	L	Data Out	Read
L	H	L	X	Data In	Write
L	H	H	H	Z	Output Disable

Note: L = low, H = high, X = H or L, Z = high impedance.

Electrical Characteristics

Absolute Maximum Ratings

Supply voltage to GND potential:.....-0.5V + 7.0V DC input voltage: .....GND - 0.5V to VCC + 0.5 DC output voltage high Z state: .....GND - 0.5V to VCC + 0.5 Storage temperature: .....-65·C to +150·C Output current into outputs (low): ..... 20 mA Electro Static Discharge voltage with HBM method (MIL STD 883D method 3015): ..... > 4000V Electro Static Discharge voltage with Socketed CDM method (ANSI/ESD SP5.3.2-2004): ..... > 1000V	*NOTE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. **Exposure between recommended DC operating and absolute maximum rating conditions for extended periods may affect device reliability.**

Military Operating Range

Operating Voltage	Operating Temperature
5V ± 10%	-55·C to + 125°C·

Recommended DC Operating Conditions

Parameter	Description	Minimum	Typical	Maximum	Unit
V_{CC}	Supply voltage	4.5	5.0	5.5	V
GND	Ground	0.0	0.0	0.0	V
V_{IL}	Input low voltage	GND - 0.5	0.0	0.8	V
V_{IH}	Input high voltage	2.2	–	VCC + 0.5	V

Capacitance

Parameter	Description	Minimum	Typical	Maximum	Unit
Cin(1)	Input low voltage	–	–	8	pF
Cout(1)	Output high voltage	–	–	8	pF

Note: 1. Guaranteed but not tested.

DC Parameters

DC Test Conditions

TA = -55°C to + 125°C; Vss = 0V; V_{CC} = 4.5V to 5.5V

Symbol	Description	Minimum	Typical	Maximum	Unit
IIX (1)	Input leakage current	-1	–	1	µA
IOZ(1)	Output leakage current	-1	–	1	µA
VOL (2)	Output low voltage	–	–	0.4	V
VOH (3)	Output high voltage	2.4	–	–	V

1. GND < Vin < V_{CC}, GND < Vout < V_{CC} Output Disabled.
2. V_{CC} min. IOL = 8 mA
3. V_{CC} min. IOH = -4 mA.

Consumption

Symbol	Description	AT65609EHV	Unit	Value
ICCSB (1)	Standby supply current	5	mA	max
ICCSB1 (2)	Standby supply current	3	mA	max
ICCOP (3)	Dynamic operating current	50	mA	max

1. $\overline{CS1}$ > V_{IH} or CS2 < V_{IL} and $\overline{CS1}$ < V_{IL}.
2. $\overline{CS1}$ > V_{CC} - 0.3V or, CS2 < GND + 0.3V and $\overline{CS1}$ < 0.2V.
3. F = 1/TAVAV, Iout = 0 mA, $\overline{WE}$ = $\overline{OE}$ = V_{CC}, Vin = GND or V_{CC}, V_{CC} max, $\overline{CS1}$=V_{IL}, CS2=V_{IH}

AC Parameters

AC Test Conditions

Input Pulse Levels: ..... GND to 3.0V

Input Rise/Fall Times: ..... 5 ns

Input Timing Reference Levels: 1.5V

Output loading IOL/IOH (see Figure 1 and Figure 2): ..... +30 pF

AC Test Loads Waveforms

Figure 1

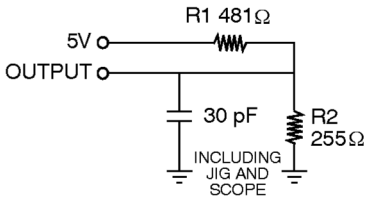


Figure 2

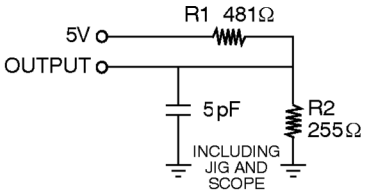
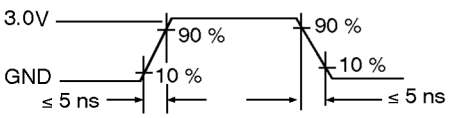
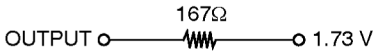


Figure 3



Equivalent to : THEVENIN EQUIVALENT

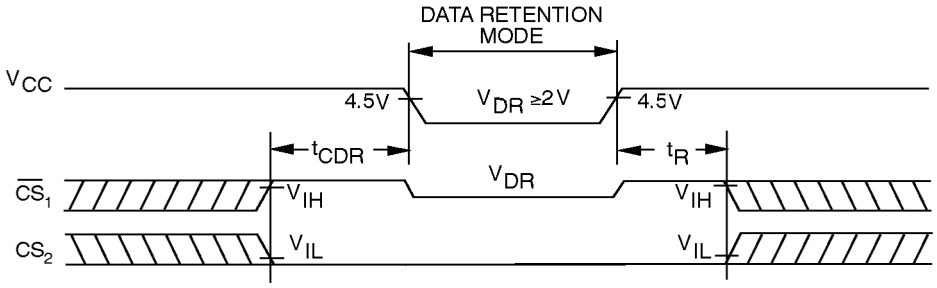


Data Retention Mode

Atmel CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. During data retention chip select $\overline{CS1}$ must be held high within VCC to VCC -0.2V or, chip select CS2 must be held down within GND to GND +0.2V.
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. During power up and power-down transitions $\overline{CS1}$ and $\overline{OE}$ must be kept between VCC + 0.3V and 70% of VCC, or with CS2 between GND and GND -0.3V.
4. The RAM can begin operation > TR ns after VCC reaches the minimum operation voltages (4.5V).

Timing



Data Retention Characteristics

Parameter	Description	Minimum	Typical TA = 25 ·C	Maximum	Unit
VCCDR	V_{CC} for data retention	2.0	–	–	V
TCDR	Chip deselect to data retention time	0.0	–	–	ns
TR	Operation recovery time	TAVAV(1)	–	–	ns
ICCDR1(2)	Data retention current at 2.0V	–	1	1.5	mA
ICCDR2(2)	Data retention current at 3.0V	–	1.5	2	mA

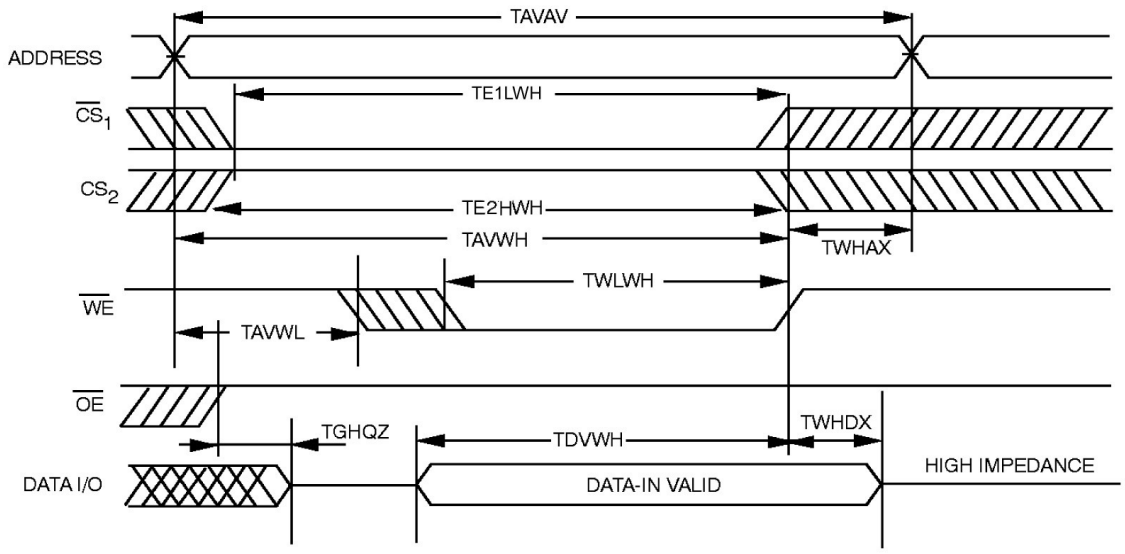
Notes: 1. TAVAV = Read Cycle Time
2. $\overline{CS1}$ = V_{CC} or CS2 = $\overline{CS1}$ = GND, Vin = GND/V_{CC}, this parameter is only tested at V_{CC} = 2V.

Write Cycle

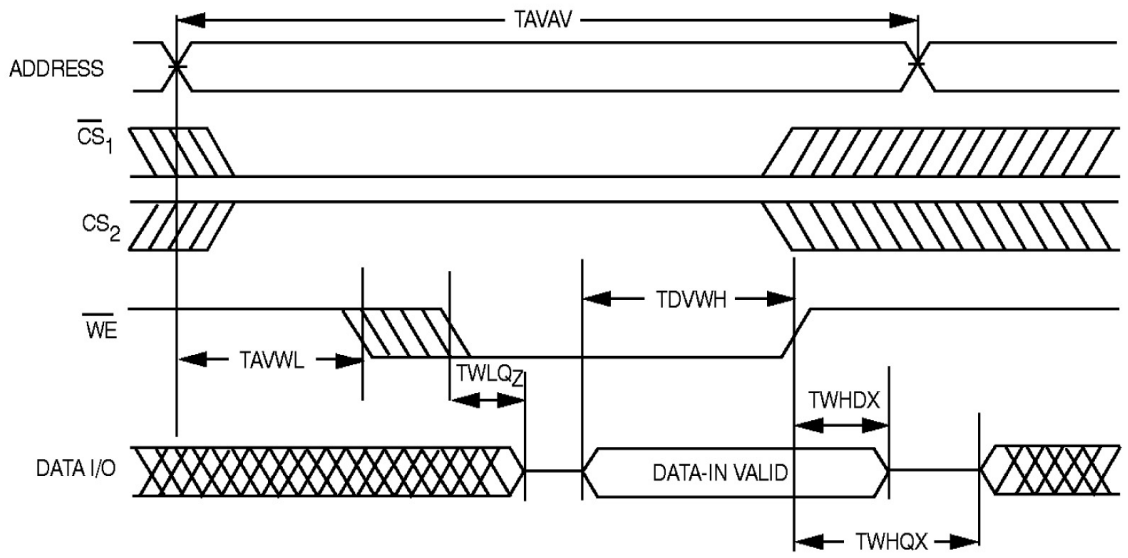
Symbol	Parameter	AT65609EHV	Unit	Value
TAVAW	Write cycle time	35	ns	min
TAVWL	Address set-up time	0	ns	min
TAVWH	Address valid to end of write	30	ns	min
TDVWH	Data set-up time	20	ns	min
TE1LWH	$\overline{CS1}$ low to write end	30	ns	min
TE2HWH	CS2 high to write end	30	ns	min
TWLQZ	Write low to high Z[1]	12	ns	max
TWLWH	Write pulse width	30	ns	min
TWHAX	Address hold from to end of write	3	ns	min
TWHDX	Data hold time	0	ns	min
TWHQX	Write high to low Z[1]	0	ns	min

Note: Parameters guaranteed, not tested, with output loading 5 pF.

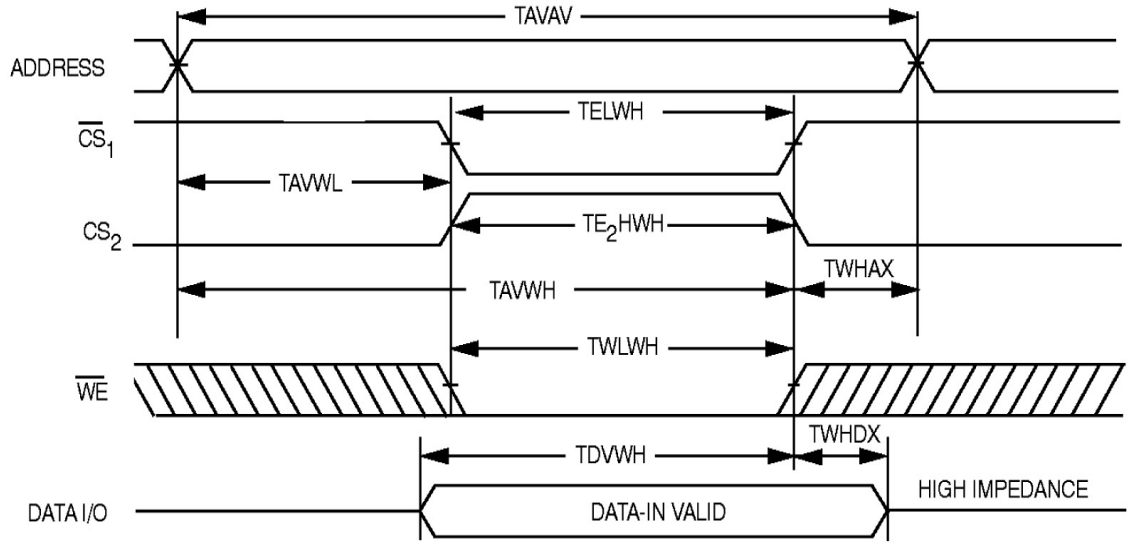
Write Cycle 1 — $\overline{WE}$ Controlled, $\overline{OE}$ High During Write



Write Cycle 2 **$\overline{WE}$ Controlled, $\overline{OE}$ Low**



Write Cycle 3 **$\overline{CS1}$ or CS2 Controlled**



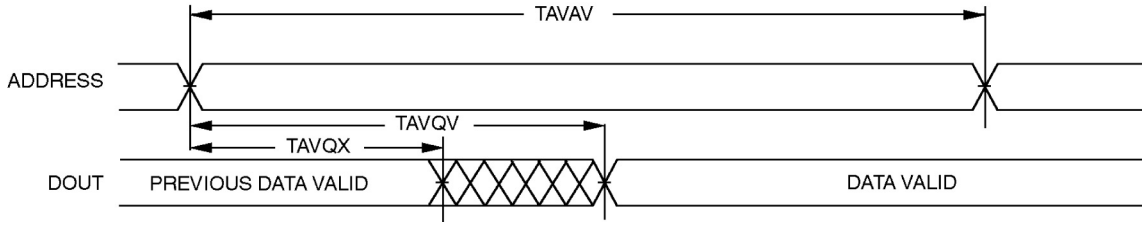
Note: The internal write time of the memory is defined by the overlap of $\overline{CS1}$ Low and CS2 HIGH and $\overline{WE}$ LOW. Both signals must be actived to initiate a write and either signal can terminate a write by going in actived. The data input setup and hold timing should be referenced to the actived edge of the signal that terminates the write. Data out is high impedance if $\overline{OE}$ = V_{IH}.

Read Cycle

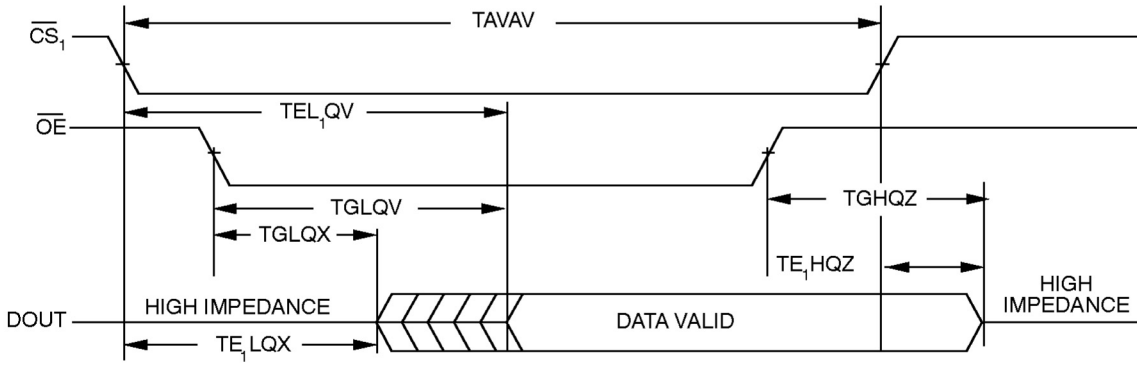
Symbol	Parameter	AT65609EHV	Unit	Value
TAVAV	Read cycle time	40	ns	min
TAVQV	Address access time	40	ns	max
TAVQX	Address valid to low Z(1)	3	ns	min
TE1LQV	Chip-select1 access time	40	ns	max
TE1LQX	$\overline{CS1}$ low to low Z(1)	3	ns	min
TE1HQZ	$\overline{CS1}$ high to high Z(1)	15	ns	max
TE2HQV	Chip-select2 access time	40	ns	max
TE2HQX	CS2 high to low Z(1)	3	ns	min
TE2LQZ	CS2 low to high Z(1)	15	ns	max
TGLQV	Output Enable access time	12	ns	max
TGLQX	$\overline{OE}$ low to low Z(1)	0	ns	min
TGHQZ	$\overline{OE}$ high to high Z(1)	10	ns	max

Note: 1. Parameters Guaranteed, not tested, with output loading 5 pF.

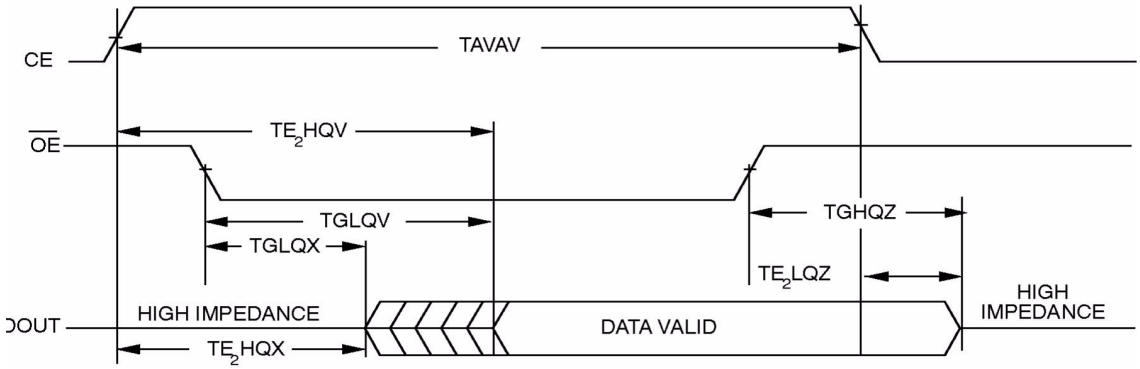
Read Cycle 1 **Address Controlled ($\overline{CS1}$ = $\overline{OE}$ Low, CS2 = $\overline{WE}$ High)**



Read Cycle 2 **$\overline{CS1}$ Controled (CS2 = $\overline{WE}$ High)**



Read Cycle 3 **CS2 Controlled ($\overline{WE}$ High, $\overline{CS1}$ Low)**



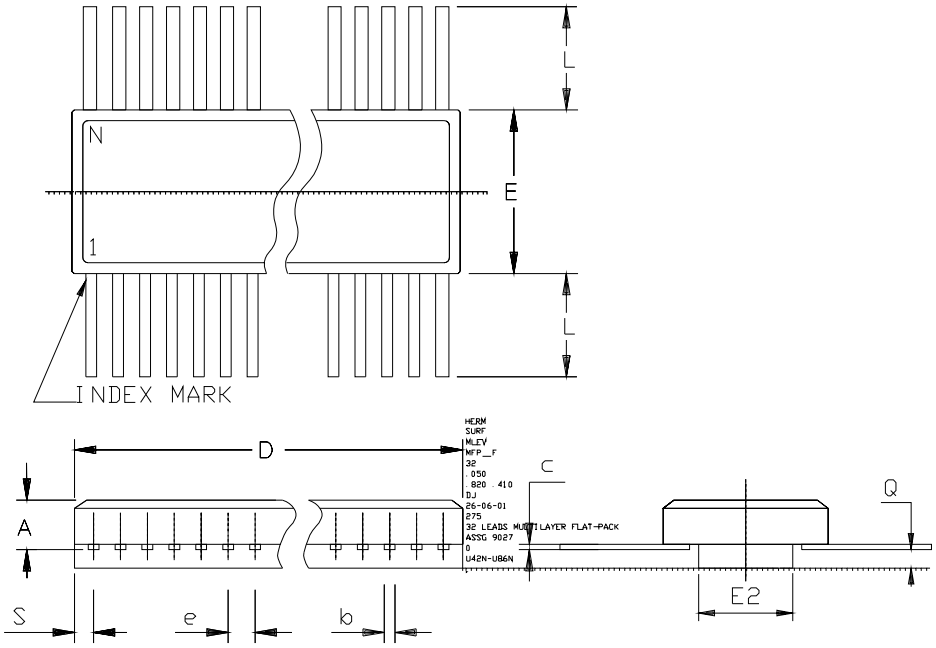
Ordering Information

Part Number	Temperature Range	Speed	Package	Flow
AT65609EHV-C940-E (1)	25·C	40 ns	SB32.4	Engineering Samples
AT65609EHV-DJ40-E (1)	25·C	40 ns	FP32.4	
AT65609EHV-C940MQ	-55· to +125·C	40 ns	SB32.4	Mil Level B
AT65609EHV-DJ40MQ	-55· to +125·C	40 ns	FP32.4	
AT65609EHV-C940SV	-55· to +125·C	40 ns	SB32.4	Space Level B
AT65609EHV-DJ40SV	-55· to +125·C	40 ns	FP32.4	
AT65609EHV-C940SR	-55· to +125·C	40 ns	SB32.4	Space Level B RHA
AT65609EHV-DJ40SR	-55· to +125·C	40 ns	FP32.4	

Note: 1. Contact Atmel for availability.

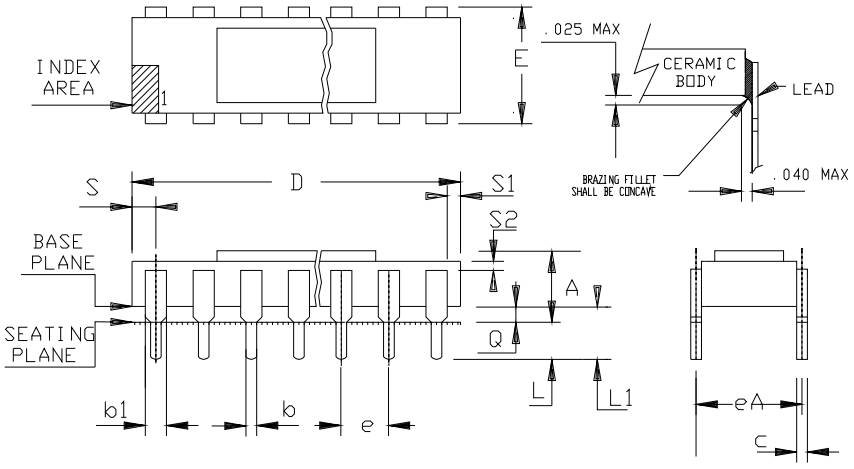
Package Drawings

32-lead Flat Pack 400 Mils



	MM		INCH	
	Min	Max	Min	Max
A	1.78	2.72	.070	.107
b	0.38	0.48	.015	.019
c	0.076	0.15	.003	.007
D	20.62	21.03	.812	.828
E	10.26	10.57	.404	.416
E2	6.96	7.26	.274	.286
e	1.27 BSC		.050 BSC	
L	7.37	7.87	.290	.310
Q	0.51	0.76	.020	.030
S	---	1.14	---	.045
N	32		32	

32-lead Side Braze 400 Mils



	MM		INCH	
A	2.92	4.32	.115	.170
b	0.40	0.51	.016	.020
b1	1.27 TYP		0.05 TYP	
c	0.23	0.30	.009	.012
D	40.13	41.15	1.580	1.620
E	10.16	10.67	.400	.420
eA	9.90	10.41	.390	.410
e	2.54	BSC	.100	BSC
L	3.43	4.20	.135	.165
L1	4.44	5.72	.175	.225
Q	1.02	1.52	.040	.060
S	-	1.65	-	.065
S1	0.13	-	.005	-
S2	0.13	-	.005	-

Document Revision History

Changes from 7832A to 7832B

1. Page 1 : total dose value updated and ESD item added
2. Page 5 : ESD HBM improved and ESD Socketed CDM added
3. Page 6 : note 3 of consumption table updated
4. Page 13 : ordering information section updated

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