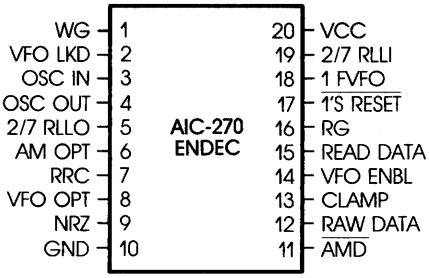
2/7 RLL Encoder/Decoder

ADVANCE

- Supports 2/7 RLL Encoding which Provides up to 50% Increased Bit Density
- Full NRZ to/from 2/7 RLL Encode and Decode
- 2.5 MHz to 10 MHz Bit Rates
- Address Mark Detection
- Minimum Passive Support Components
- Minimum Board Space Requirements
- Two Selectable VFO Sync Patterns
- Two Selectable Address Mark Options
- Single +5V Power Supply



DESCRIPTION

The Adaptec AIC-270 Encode/Decode Chip is a 20 pin custom LSI device which provides an efficient data interface between NRZ data and 2/7 Run Length Limited recorded disk drives with a minimum of external support. The AIC-270 can be used as part of Adaptec's Winchester controller chip set, or can reside on the disk drive and provide increased capacity, with an NRZ output to a controller as in ESDI.

This chip performs all the functions necessary to convert NRZ data to and from 2/7 RLL data. An external variable frequency oscillator (VFO) is also necessary to provide synchronous clock and data. The AIC-270 also incorporates address mark generation and detection logic. This feature includes VFO sync field circuitry which enables the VFO data lock-on and performs address mark search and detection.

This ENDEC (Encode/Decode) device also includes the ability to generate selectable VFO sync field patterns and address marks ahead of the outgoing 2/7 RLL data stream.

The AIC-270 is designed to operate at bit rates from 2.5 MHz to 10 MHz.

AIC-270 PIN DESCRIPTION

SYMBOL	PIN	TYPE	NAME AND FUNCTION
WG	1	IN	WRITE GATE: An input which is used to gate the write data stream to the drive interface.
VFO LKD	2	OUT	VFO LOCKED: An output generated by the preamble detect section when a count of 64 or greater has been reached.
−OSC IN	3	IN	OSCILLATOR INPUT.
+OSC OUT	4	OUT	OSCILLATOR OUTPUT.
2/7 RLLO	5	OUT	2/7 RLL OUT: This is 2/7 output data generated by the chip.
AM OPT	6	IN	AM OPTION: A control input that selects one of two different address mark patterns used by both the encoder and the decoder.
RRC	7	OUT	READ REFERENCE CLOCK: Output to the Winchester controller which is sourced from the VFO oscillator during Read Gate active, otherwise sourced from the write oscillator.
VFO OPT	8	IN	VFO SYNC OPTION: A control signal that selects one of two different VFO sync field patterns used during encoding.
NRZ	9	IN/OUT	NRZ READ/WRITE DATA: Non-return to zero data input to, or output from, the AIC-270. This pin is an output when RG is active, and an input at all other times.
GND	10		GROUND.
$\overline{\text{AMD}}$	11	OUT	ADDRESS MARK DETECT: When read gate is active, a latch is set when an address mark has been detected. The output is tristated when RG is false.
RAW DATA	12	OUT	RAW DATA: The raw data stream to be output to the external VFO. Source for this output is OSC IN if VFO ENABLED is low. When VFO ENABLED is high, the source is READ DATA.
CLAMP	13	OUT	CLAMP: An output generated by the preamble detect section whenever the state of VFO ENABLED changes.
VFO ENBL	14	OUT	VFO ENABLED: An output generated by the preamble detect section when a count of 16 or greater has been reached.
READ DATA	15	IN	READ DATA: A pulse input to the preamble section that increments the counter. This is the data that is input from the drive.
RG	16	IN	READ GATE: An input which signals the phase lock loop to lock onto the read data stream coming from the drive.
$\overline{\text{1's RESET}}$	17	IN	1's RESET: A pulse input to the preamble detect section that resets the counter.
1FVFO	18	IN	1FVFO: This is a fundamental VFO input from the external data/clock standardizer.
2/7 RLLI	19	IN	2/7 RLL IN: This provides the 2/7 code to be converted to NRZ data.
V_{CC}	20		+5 Volts.

FUNCTIONAL DESCRIPTION

The AIC-270 Encode/Decode Chip has three major areas of logic:

- Data encode circuitry.
- The sync field search circuitry and counter.
- Address mark detect and data decode circuitry.

The functional block diagram is shown in Figure 1. The data encode circuitry and address mark generation is used during a disk write operation (NRZ to 2/7 RLL conversion), and the sync field search circuitry, address mark detect and data decode circuitry are used during a disk read operation (2/7 RLL to NRZ conversion).

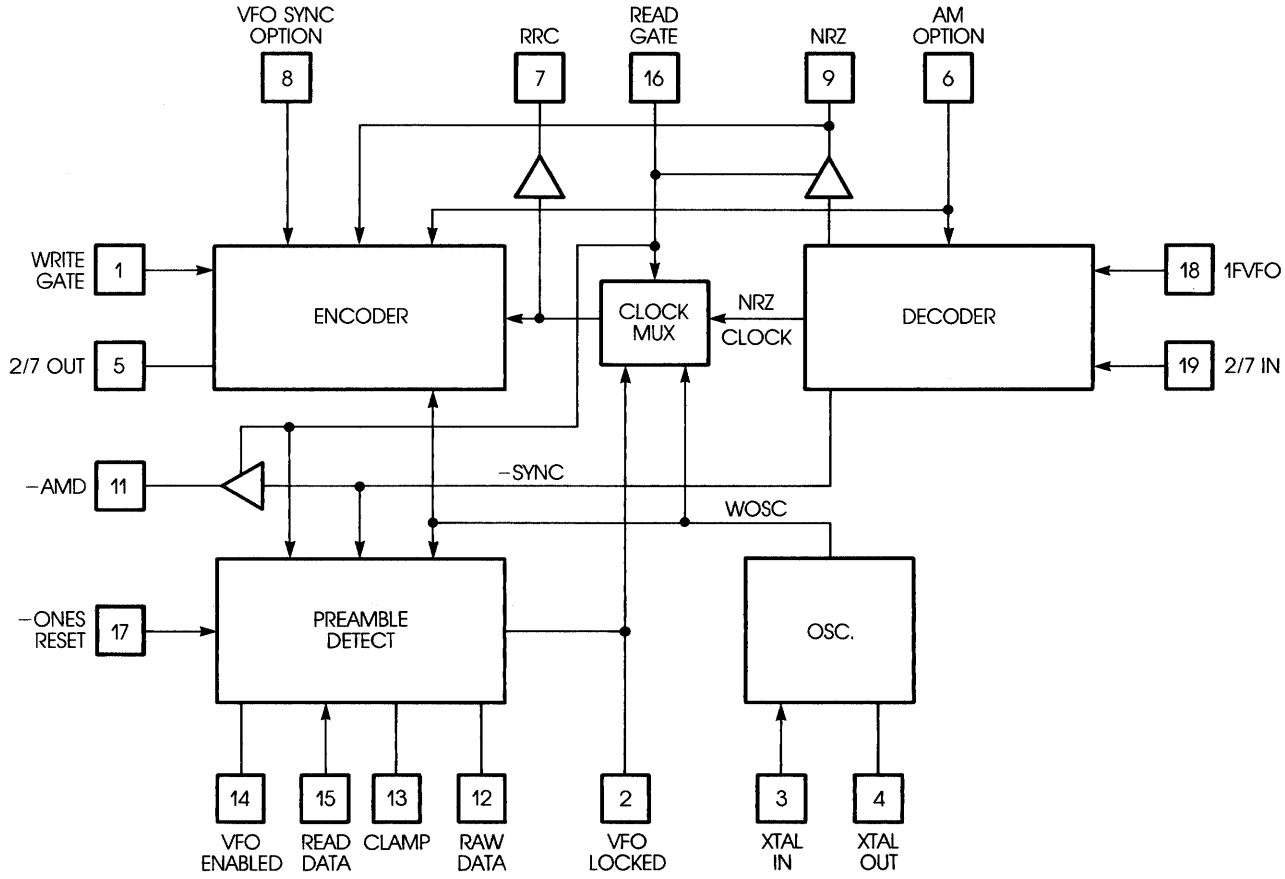


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

Write Operation

During a write operation, the AIC-270 chip converts NRZ format data to 2/7 RLL format. In addition to this, during a format operation, the chip also automatically generates one of two possible VFO sync fields (preamble patterns). The VFO sync field is generated between the time write gate goes high and the first low to high transition on the NRZ line. The two possible patterns are: a) 100100100... (VFO sync=0) or b) 100010001000... (VFO sync = 1), selectable by the VFO sync option pin. On the first low to high NRZ transition, the device stops sending the preamble pattern and then generates an address mark.

There are two possible address marks used, which are selectable by an external pin (AM option). The first option (AM option = 1) uses a 5EAxH pattern that satisfies the 2/7 constraints but never occurs during a normal encoding sequence. Use of this feature provides a zero probability of erroneous syncing, say in the middle of a data field. The second option (AM option = 0) uses a FFH pattern for syncing. This option requires some additional external mechanism to prevent false syncing such as a DC erased area on the disk.

Read Disk Operation

During a read operation, the AIC-270 chip works in conjunction with external VFO circuitry, to convert 2/7 RLL data to NRZ data. The VFO circuitry can also be referred to as a data standardizer. A block overview of the data standardizer is shown in Figure 2.

The two signals that interface to the VFO are "RAW DATA" and "CLAMP." The raw data input to the VFO is the signal that the VFO is required to track. When "READ GATE" is off, the raw data output of the AIC-270 is "2FOSC." The purpose is simply to provide an input to the VFO that will keep the VFO pumped to nominal disk data rates.

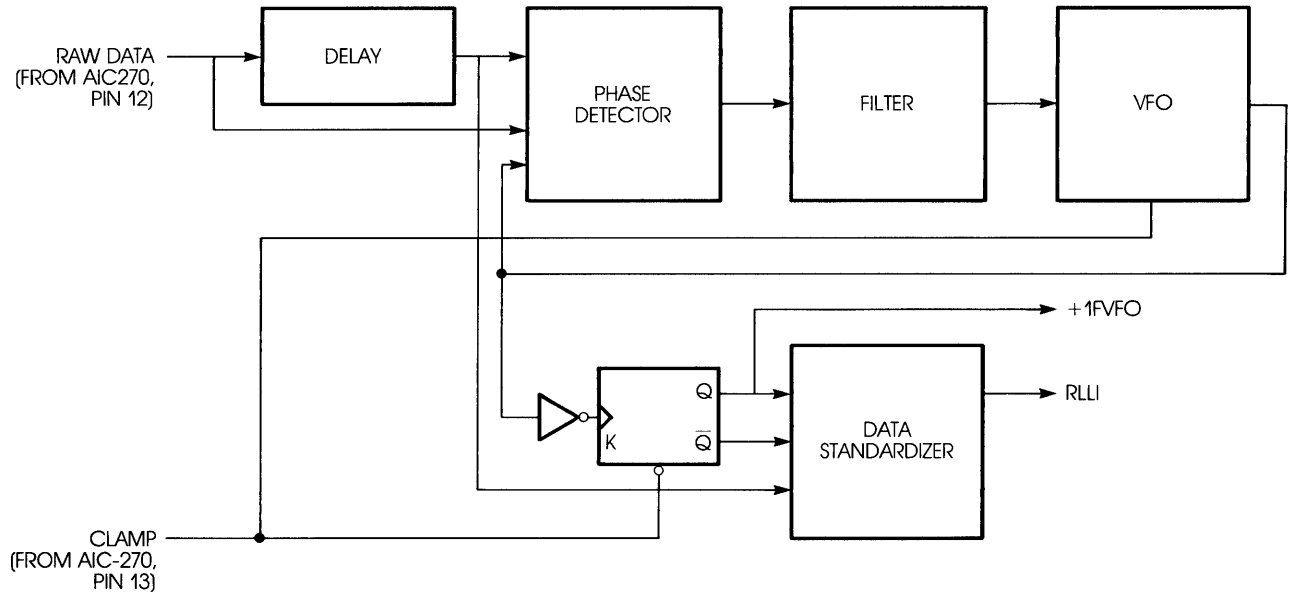


FIGURE 2. VFO BLOCK OVERVIEW

When "READ GATE" is turned on, a sequence of events must occur for a successful transition from "2FOSC" feeding the VFO to "READ DATA" feeding the VFO. The sequence is as follows.

1. After RG is on, the counter must count 16 bit transitions in a row. Any time a greater than expected space between bit transitions is detected externally, a "ONE'S RESET" input will occur to restart the counter. The "ONE'S RESET" input will be a minimum of 40 ns in width, and is typically implemented with a retriggerable one shot of 2.5 × bit cell duration for the 100100100... preamble, and 3.5 × bit cell duration for the 1000100010000... preamble. This is done to ensure that the VFO is enabled only when reading the VFO sync field. A "ONE'S RESET" implies that the pattern being observed on the drive is not the VFO sync field.

2. When count 16 is reached, a latch is set that will switch the "RAW DATA" source from "2FOSC" to "READ DATA" and generate a "CLAMP" output. The "CLAMP" signal is guaranteed to be at least 2 data periods in length and its trailing edge will follow the "RAW DATA" output by not more than 20 ns or precede it by no more than 10 ns. The "CLAMP" signal is used by the VFO circuit to minimize the phase error between "READ DATA" and "2FVFO." The "VFO ENABLE" signal is asserted at this time.

3. With "READ DATA" feeding the VFO, the counter will continue for 48 more counts to a maximum of 64. During this period, if a "ONE'S RESET" occurs, the counter will be reset, a "CLAMP" signal will occur, and the "RAW DATA" source will be switched back to "2FOSC." If "ONE'S RESET" does not occur, a latch will be set that allows for the detection of an address mark and disallows any further "ONE'S RESET" from affecting the counter. This latch will also switch the "RD/REF CLOCK" output source from the divided "2FOSC" to "1FVFO." There are no timing constraints for this switch to occur and a glitch will be output on the RD/REF clock at this point. The "VFO LOCKED" signal is asserted at this time.

4. The counter continues to run while the AM detector is looking for an address mark. If the counter reaches count 128 without an AM detected, the count 16 latch will be reset, causing a "CLAMP" signal to be generated and "2FOSC" to be output to the VFO. Also, the search AM latch will be reset, disabling the AM detector and switching the source for the "RD/REF CLOCK" output. The VFO will be input with "2FOSC" for 4 byte times and the sequence will begin again at Step 1. If an address mark is found, the "AMD" latch will be set and its output will appear on the "AMD" pin. The AMD latch being set will disable any further contributions to the sequence by the counter, allowing the data field to be read.

5. At any time "RG" may be turned off, resetting the counter and causing a "CLAMP" signal to be generated and the "RAW DATA" source changed to "2FOSC."

NOTE: The device has additional outputs such as VFO ENABLE (count 16) and VFO LOCKED (count 64) which may be used in the VFO interface.

ABSOLUTE MAXIMUM RATINGS

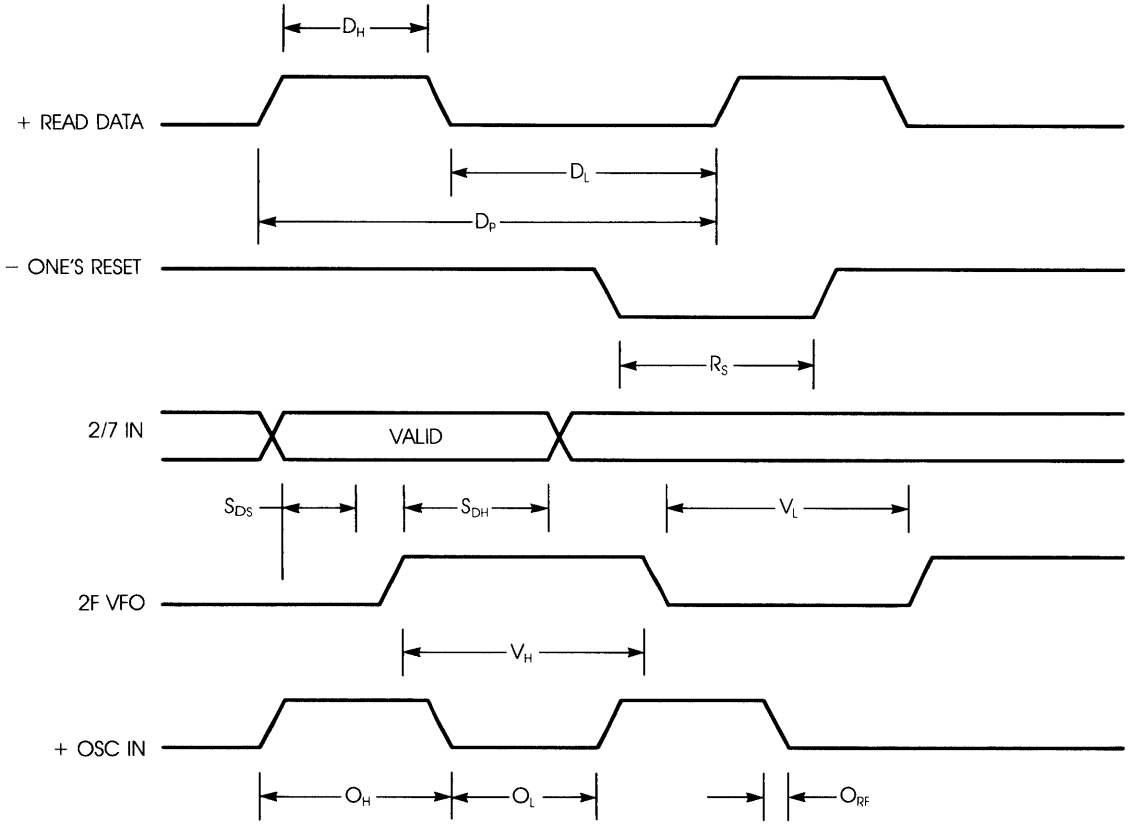
Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to 150°C
Voltage on Any Pin with Respect to Ground ..... −0.3 to V_{CC} + 0.3
Power Dissipation ..... 0.25 watt
Power Supply Voltage ..... 4.75 to 5.25 volts

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

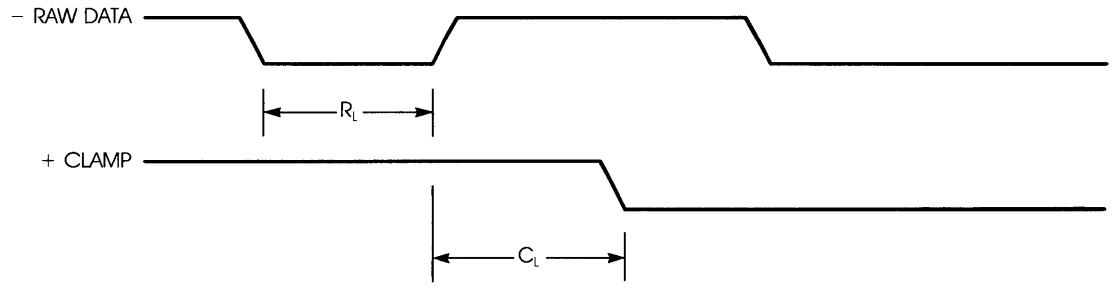
SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage (NRZ, RG, WG, 1FVFO, −1'S RESET, READ DATA, AM OPT and VFO OPT)	−0.3	0.8	V	
V_{IL}	Input Low Voltage (OSC)		0.4 × V_{CC}	V	
V_{IH}	Input High Voltage (NRZ, RG, WG, 1FVFO, −1'S RESET, READ DATA, AM OPT and VFO OPT)	2.0	V_{CC} + 0.3	V	
V_{IH}	Input High Voltage (OSC)	0.8 × V_{CC}		V	
V_{OL}	Output Low Voltage (NRZ, RRC, 2/7 OUT, RAW DATA, CLAMP, AMD, VFO LKD, VFO ENBL)		0.4	V	I_{OL} = 4 mA*
V_{OH}	Output High Voltage (NRZ, RRC, 2/7 OUT, RAW DATA, CLAMP, AMD, VFO LKD, VFO ENBL)	4.0			I_{OH} = −400 µA
I_{CC}	Supply Current		50	mA	
C_{IN}	Input Capacitance	10		pF	
C_{OUT}	Output Capacitance	50		pF	

AIC-270 INPUT TIMING



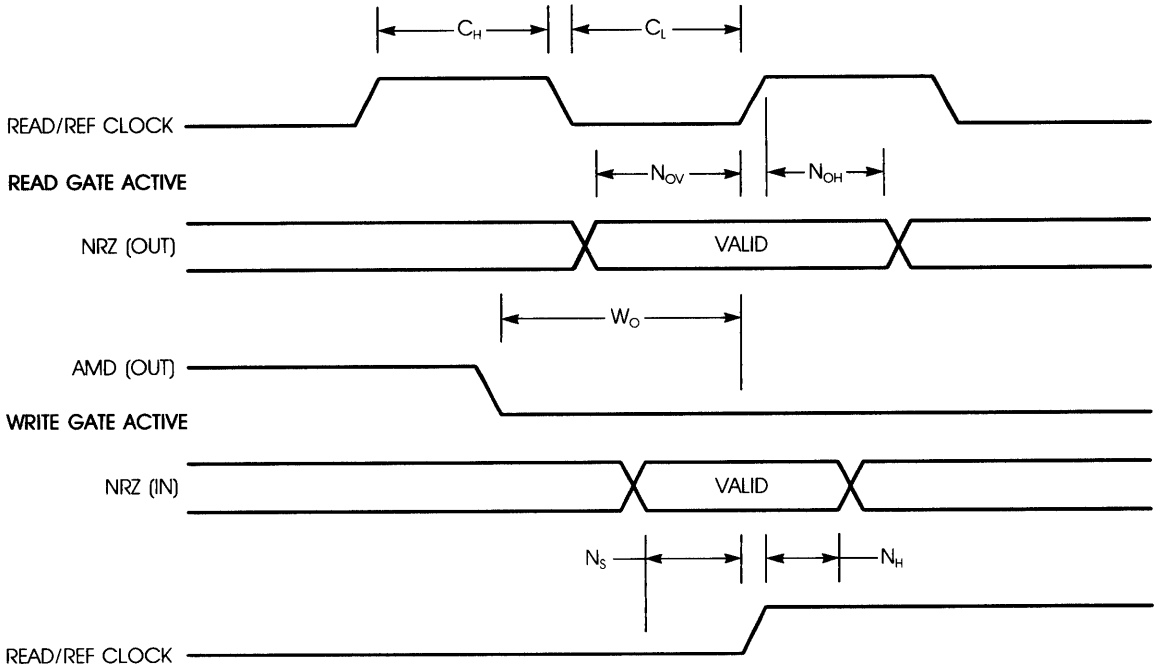
SYMBOL	PARAMETER	MIN	MAX	UNITS
D_H	Read Data High	20		ns
D_L	Read Data Low	100		ns
D_P	Read Data Period	140	4000	ns
R_S	One's Reset Low	20		ns
V_H	1FVFO High	16		ns
V_L	1FVFO Low	16		ns
S_{DS}	Std Data Setup to 1FVFO ↑	15		ns
S_{DH}	Std Data Hold	10		ns
O_H	OSC in High	16		ns
O_L	OSC in Low	16		ns
O_{RF}	OSC in Rise or Fall		5	ns

AIC-270 OUTPUT TIMING



SYMBOL	PARAMETER	MIN	MAX	UNITS
R_L	Raw Data Active Low	20		ns
C_L	Raw Data ↑ to Clamp ↓		20	ns

AIC-270 BI-DIRECTIONAL TIMING



SYMBOL	PARAMETER	MIN	MAX	UNITS
C_H	Read/Ref Clock High	40		ns
C_L	Read/Ref Clock Low	40		ns
N_S	NRZ in Setup to Read/Ref ↑	25		ns
N_H	Read/Ref ↑ to NRZ in Hold	15		ns
N_{OV}	NRZ Out Valid to Read/Ref ↑	30		ns
W_O	Read/Ref ↑ to WAM Out Valid	30		ns
N_{OH}	NRZ Out Hold	20		ns

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