Winbond Electronics Corp.

W9953F/ W9954F
TV ENCODER

The W9953F may be purchased by Macrovision Authorized Buyers only. The W9953F is protected by U.S. patent numbers 4,631,601, 4,577,216 and 4,819,098 and other intellectual property rights. The use of Macrovision's copy protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-per-view uses only. Reverse engineering or disassembly is prohibited. For more information please contact Winbond sales office.

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Winbond Electronics Corp.

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GENERAL DESCRIPTION

The W9953F/W9954F is a high performance digital video encoder which converts a CCIR 601 4:2:2 pixel digital video stream into a standard analog baseband television signal compatible with world wide standards. Both interlaced mode and non-interlaced mode are supported. In addition, the chip provides Closed-Captions, WSS (Wide Screen Signal), CGMS (Copy Generation Management System) and Teletext encoding functions. The W9953F also allows Macrovision 7.01 copy protection.

Synchronization of the W9953F/W9954F can be operated in one of six modes (2 master and 4 slave). The on-chip 2X oversampling eases the analog post-filtering. Three 10-bit resolution D/A converters provide Y, C and CVBS signals, all in standard video-level at doubly terminated 75 ohms load.

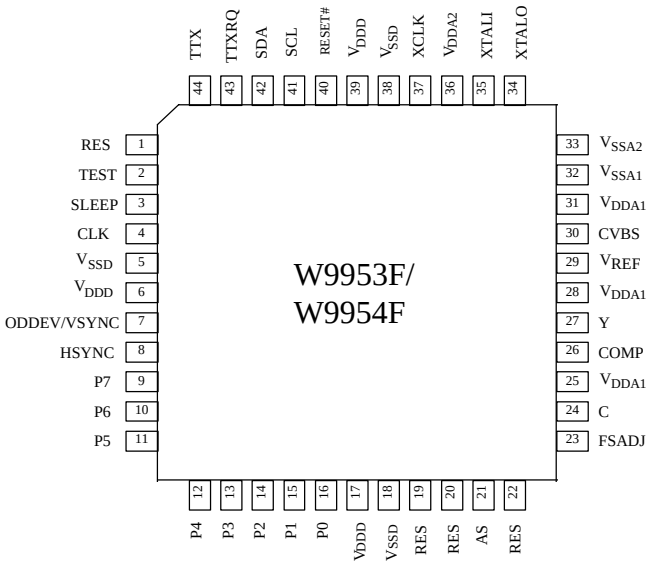
FEATURES

- Monolithic CMOS 3.3V (5V) device
- NTSC-M, PAL-B, D, G, H, I, N_C, M encoding
- Interlaced or non-interlaced operation
- Standard CCIR 601 or extended input data range
- 8-bit YCbCr or 8-bit BT656 input format
- Master or slave operation modes
- Programmable sync polarity and horizontal phase
- Programmable Y/C delay relationship
- Sync extraction from digital input data
- Three 10-bit DACs run at 2X pixel rate, provide Y, C and CVBS output formats
- Closed captioning and WSS/CGMS encoding
- PAL-WST and NABTS Teletext encoding
- Fast I^2C-bus control port
- Macrovision Rev 7.01 copy protection process (W9953F only)
- On chip color-bar generator
- On chip voltage reference
- Power-down mode of chip or individual DACs
- QFP44 package

APPLICATIONS

- DVD Players
- Video CD players
- Digital Set-top box
- Multimedia PCs

PIN CONFIGURATION

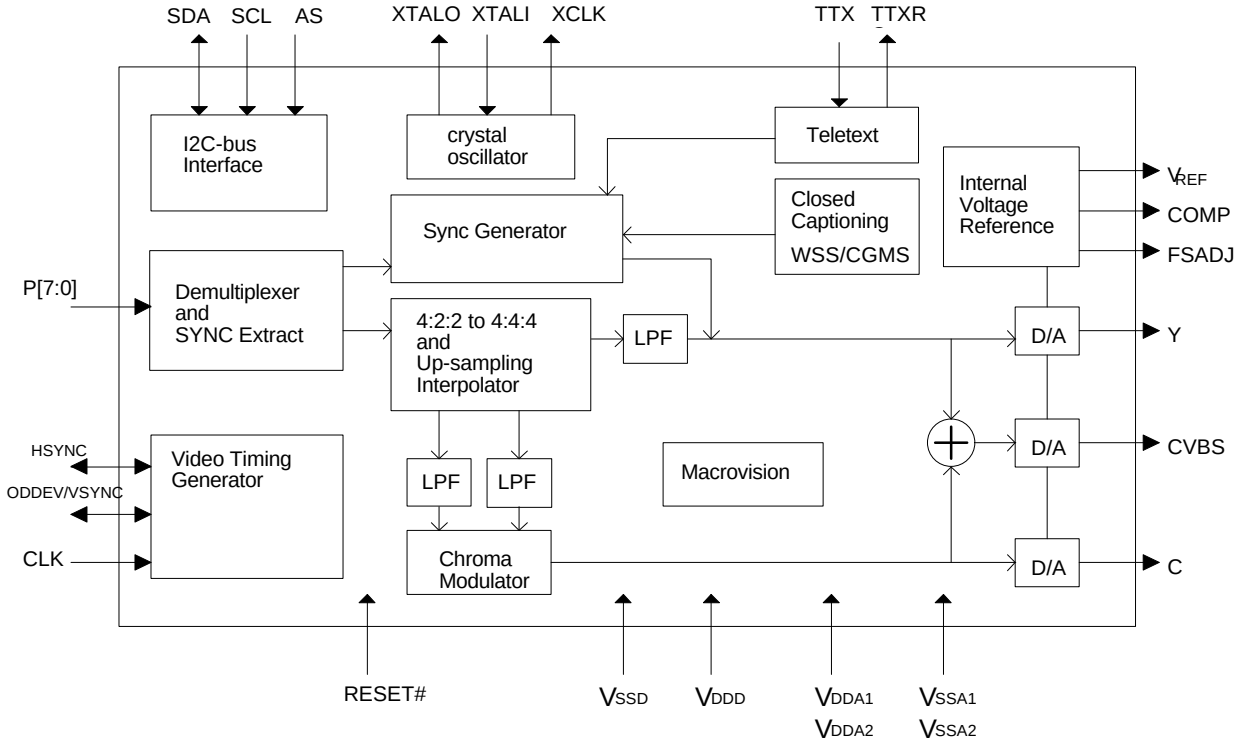


PIN DESCRIPTION

PIN	NAME	I/O	DESCRIPTION
2	TEST	I	Test pin; connected to ground.
3	SLEEP	I	Power-down control pin; HIGH will configure the device for power-down mode; connected to LOW for normal operation.
4	CLK	I	27 Mhz master clock.
7	ODDEV/ VSYNC	I/O	Frame sync or Vertical sync input/ouput.
8	HSYNC	I/O	Horizontal sync input/ouput.
9 -16	P[7:0]	I	YCrCb pixel inputs. They are latched on the rising edge of CLK.
21	AS	I	I^2C chip slave address selection; LOW: 40H, HIGH: 42H.
23	FSADJ	O	Full-scale adjust control pin. The full-scale current of DAC is controlled by connecting a resister (R_{SET}) between this pin and V_{SSA2}. The full-scale current I_{OUT} = K * V_{REF} / R_{SET} (mA), K = 2820 for 5V VDD and K = 2765

			for 3.3V VDD.
24	C	O	Analog chrominance signal output.
26	COMP	O	Compensation pin. A 0.1 uF ceramic capacitor with lead length as short as possible must be used to decouple this pin to V_{DDA1}.
27	Y	O	Analog luminance signal output.
29	V_{REF}	O	Voltage reference output. Typical value is 0.9V. A 0.1 uF ceramic capacitor with lead length as short as possible must be used to decouple this pin to V_{SSA2}.
30	CVBS	O	Analog composite video signal output.
32	V_{SSA1}	I	Analog ground for the DACs.
33	V_{SSA2}	I	Analog ground for the oscillator and reference voltage.
34	XTALO	O	Crystal oscillator output.
35	XTALI	I	Crystal oscillator input. A crystal with double pixel clock frequency can be connected between this pin and XTALO. If internal oscillator is not used, this pin should be connected to ground.
36	V_{DDA2}	I	Analog supply voltage for the oscillator and reference voltage.
37	XCLK	O	Clock output of the crystal oscillator.
40	RESET#	I	Hardware reset, active LOW; after reset is applied, all registers will be set to their default values and Macrovision copy protection will be enabled.
41	SCL	I	I^2C-bus serial data input.
42	SDA	I/O	I^2C-bus serial data input/output.
43	TTXRQ	O	Teletext request output, indicating a new bit has to be sent to TTX pin from the Teletext data source.
44	TTX	I	Teletext bit stream input. Data transmission is synchronized with the rising edges of master clock at a rate controlled by TTXRQ signal.
1,19,20, 22	RES	-	Reserved.
5,18,38	V_{SSD}	I	Digital ground.
6,17,39	V_{DDD}	I	Digital supply voltage.
25,28,31,	V_{DDA1}	I	Analog supply voltage for the DACs.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Data Input Format

The input digital video is a 4:2:2 time-multiplexed 8-bit stream following the ITU_R656(CCIR 656) pixel format. Input data are latched on the rising edge of the clock signal CLK via pins P[7:0]. The frequency of CLK is twice the pixel rate (27mhz) and the data sequence appears as Cb0 Y0 Cr0 Y1 Cb2 Y2 Cr2 Y3 ...The coding format is in compliance with ITU-R601. The ITU-R601 defines the black luminance signal as Y = 16 and the peak white level as Y = 235. Similarly the quantization levels for Cr and Cb color difference signals are defined to have 225 values, centered around 128. When YCrCb samples having values exceed the nominal range defined in ITU-R601, the W9953F/W9954F provides two ways (clamping or extending the range) to handle it depending on the setting of the bit **ex_rang** in register **CONFG2** :

ex_rang = 0 : clamping (default)

- Y values greater than 235 will be clamped at 235
- Y values smaller than 16 will be clamped at 16
- Cr,Cb values greater than 240 will be clamped at 240
- Cr,Cb values smaller than 16 will be clamped at 16

ex_rang = 1 : extending the range

In this mode, values of 0 and 255 are overridden as 1 and 254 respectively. All values between 1 to 254 are interpreted as valid linear values.

Luma scaling will depend on whether or not the 7.5 IRE setup in the output video waveform exists. When 7.5 IRE setup is enabled, Y range of 16-235 represents 7.5-100 IRE. When 7.5 IRE setup is disabled, Y range of 16-235 represents 0-100 IRE. Bit **setup** in register **CONFG1** can be used to control the presentation of the 7.5 IRE setup.

The W9953F/W9954F is able to encode interlaced and non-interlaced video. Set the bit **no_intl** in register CONFG1 will change the operation to non-interlaced mode. In non-interlaced mode, the horizontal lines per field is 262 for 60 Hz system and 312 for 50Hz system.

Video Timing

The W9953F/W9954F outputs interlaced or non-interlaced video in PAL-B, D, G, H, I, M N_C or NTSC-M standards. The W9953F/W9954F generates all of the required horizontal and vertical timing periods and levels for the analog video outputs.

The video waveform timing will be internally adjusted to the correct values for the new clock frequency.

Fig.1 to 4 depict typical video timing.

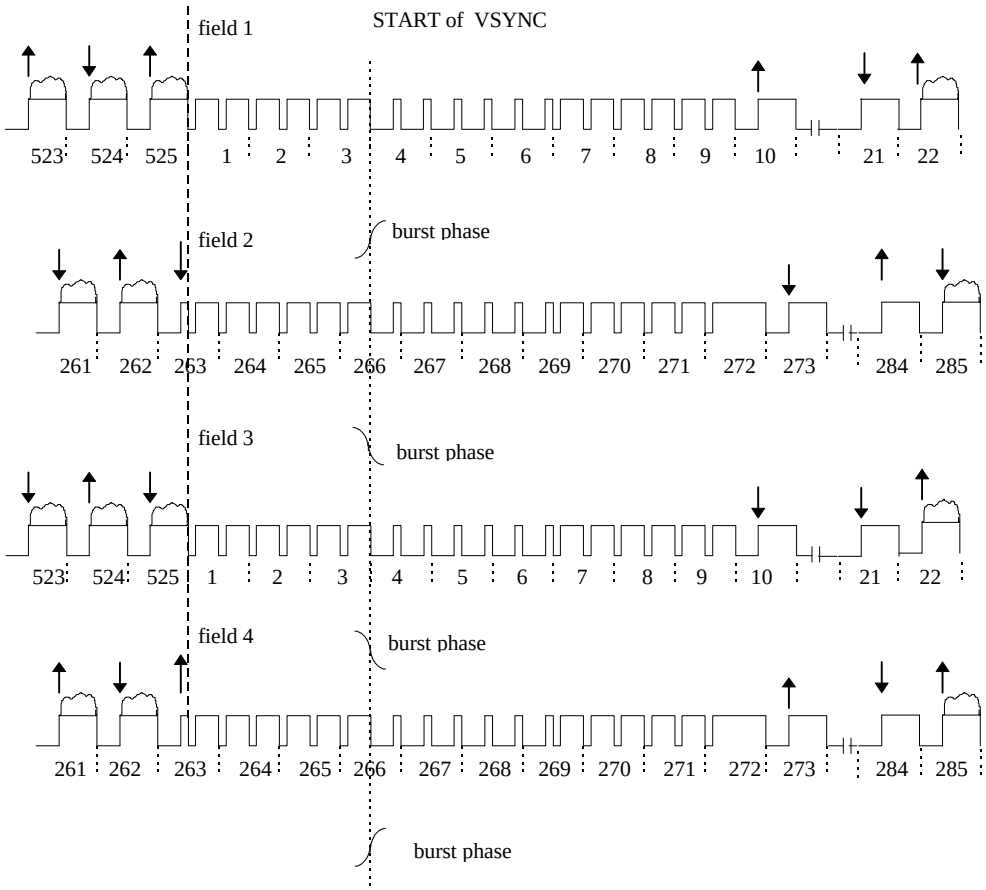


Figure 1. NTSC-M Interlace Video Timing
(SMPTE line conversion rather than CCIR-624 is used)

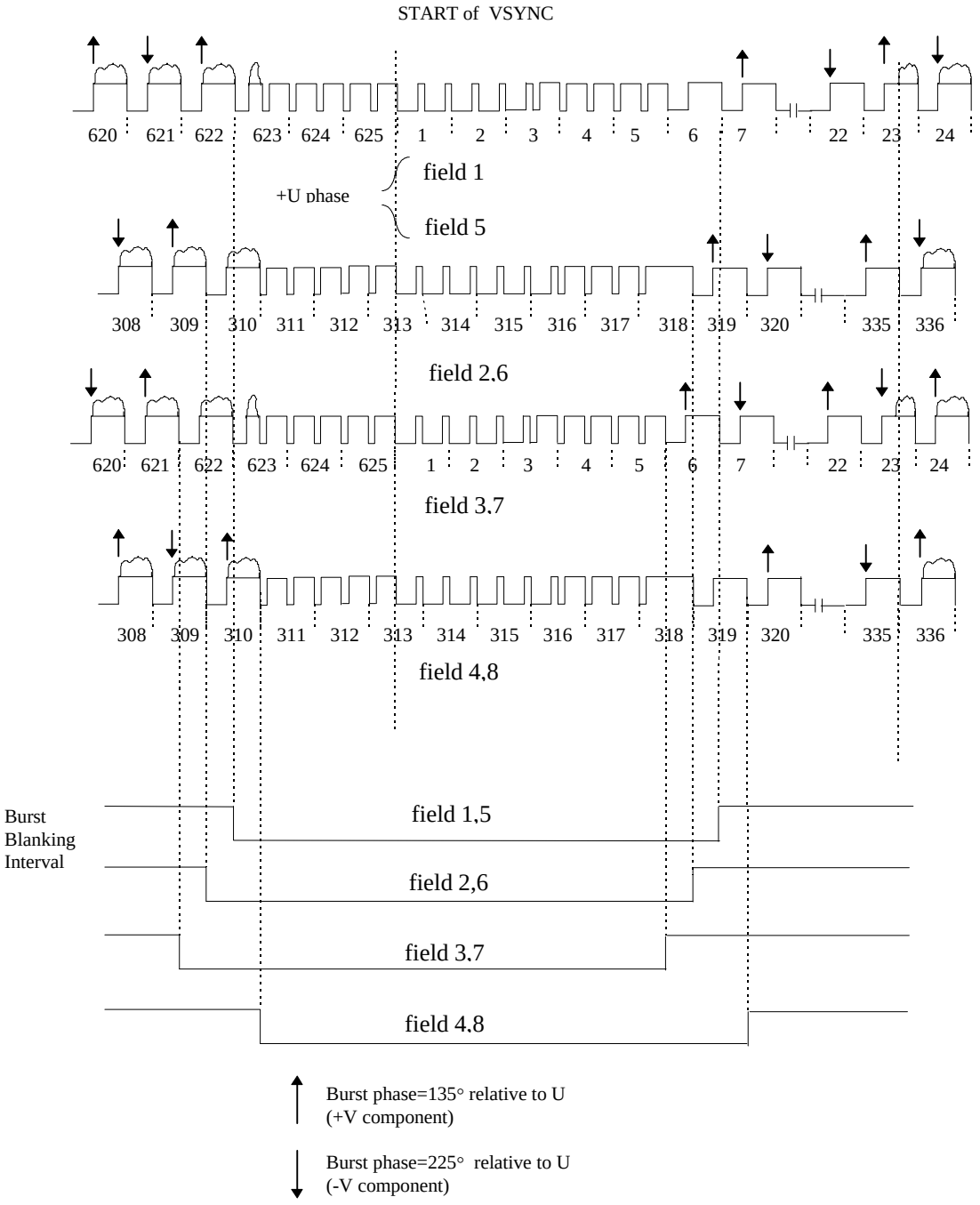


Figure 2. PAL-B,D,G,H,I,N_C Interlace Video Timing

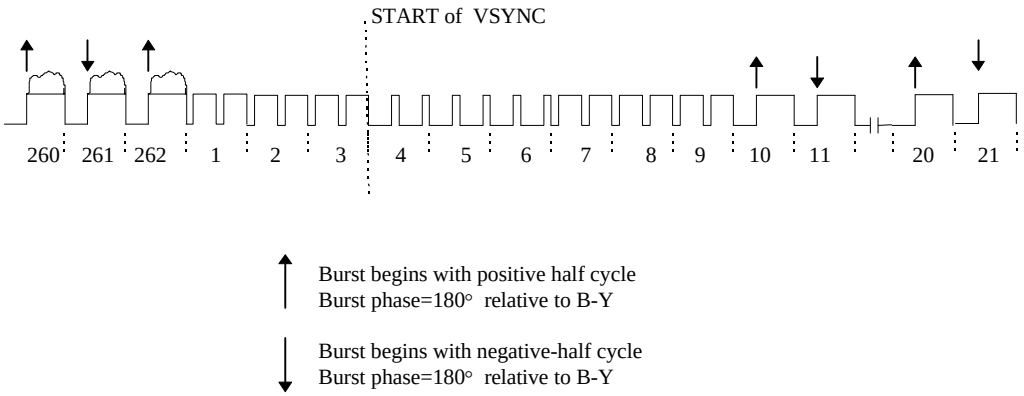


Figure 3. NTSC-M Non-interlace Video Timing

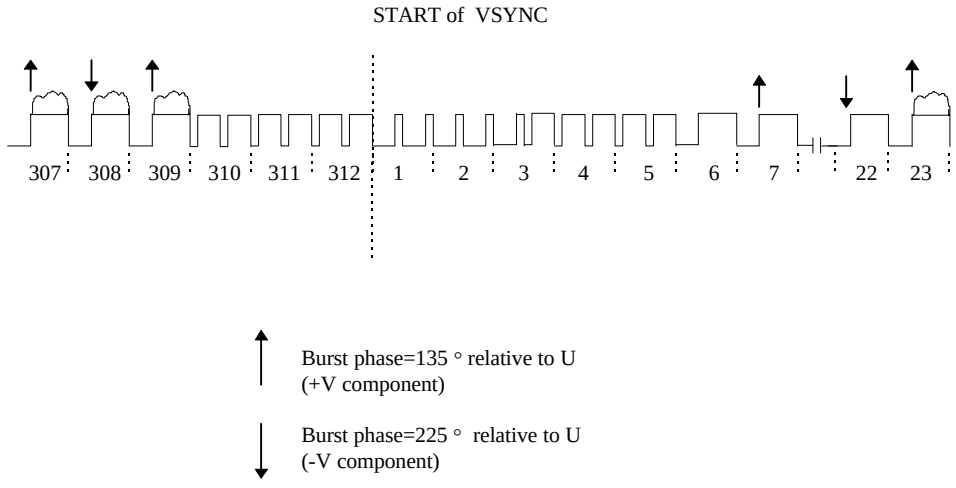


Figure 4. PAL-B,D,G,H,I,N_C Non-interlace Video Timing

Synchronization

synchronization of W9953F/W9954F is able to operate in 2 master and 4 slave modes. In the following description, ODDEV and VSYNC are alternately used to represent the same pin. The choice of the representation depends upon whether ODD/Even field signal or Vertical SYNC signal is presented on this pin.

Master Mode 1 : HSYNC + VSYNC Based

In this mode, the W9953F/W9954F supplies HSYNC and VSYNC sync signals internally to drive the digital video source. The polarities of HSYNC and VSYNC can be programmed independently (bits **pol_h** and **pol_vf** in REGISTER **CONFG2**).

In this mode, the HSYNC and VSYNC pins are output following the rising edge of CLK. The active edge of HSYNC indicates the start of a new line and the active edge of VSYNC indicates the start of a new field (interlaced operation) or a new frame (non-interlaced operation). Coincident active edges of HSYNC and VSYNC indicates the beginning of an odd field. An active edge of VSYNC without a coincident active edge of HSYNCN indicates the beginning of an even field. When non-interlaced operation is selected, the active edges of VSYNC always coincide with the HSYNC; that means all the fields are odd fields.

The phase of HSYNC relative to digital video input data can also be controlled. Normally (by default), the first clock rising edge following the HSYNC active edge samples "Cb" within YCrCb stream. Correspondingly, "Cb" of the first active pixel is sampled at the 245th or 265th CLK rising edge following the HSYNC active edge in CCIR-525 or CCIR-625 system respectively. However, by using configuration bits **syn_dl[1:0]** in REGISTER **CONFG3**, 0 to +3 clock cycles delay can be added to the period between sync and the first active "Cb" sample to cope with any data/sync phasing.

Master Mode 2 : HSYNC + ODDEV Based

In this mode, the W9953F/W9954F supplies HSYNC and ODDEV sync signals internally to drive the digital video source. The polarities of HSYNC and ODDEV can be programmed independently (bits **pol_h** and **pol_vf** in REGISTER **CONFG2**).

In this mode, the HSYNCN and ODDEV pins are output following the rising edge of CLK. The active edge of HSYNC indicates the start of a new line and the transition edges of ODDEV indicates the beginning of a new odd field. HSYNC + ODDEV based synchronization is not suitable for non-interlaced operation mode, because all fields will be defined as odd fields in this mode.

The phase of HSYNC relative to digital video input data can also be controlled. Normally (by default), the first clock rising edge following the HSYNC active edge samples "Cb" within YCrCb stream. Correspondingly, "Cb" of the first active pixel is sampled at the 245th or 265th CLK rising edge following the HSYNC active edge in CCIR-525 or CCIR-625 system respectively. However, by using configuration bits **syn_dl[1:0]** in REGISTER **CONFG3**, 0 to +3 clock cycles delay can be added to the period between sync and the first active "Cb" sample to cope with any data/sync phasing.

Slave Mode 1 : HSYNC + VSYNC Based

In this mode, the W9953F/W9954F accepts external HSYNC and VSYNC sync signals to perform the synchronization. The polarities of HSYNC and VSYNC can be programmed independently (bits **pol_h** and **pol_vf** in REGISTER **CONFG2**).

In this mode, HSYNC and VSYNC sync signals are registered on the rising edge of CLK. The active edge of HSYNC indicates the start of a new line and the active edge of VSYNC indicates the start of a new field (interlaced operation) or a new frame (non-interlaced operation). Coincident active edges of HSYNC and VSYNC (within +/- 4 clock period of CLK) indicates the beginning of an odd field. An active edge of VSYNC without a coincident active edge of HSYNCN (over +/- 4 clock period of CLK) indicates the beginning of an even field. When non-interlaced operation is selected, the active edges of VSYNC should always coincide with the HSYNC; that means all the fields are odd fields.

Only the active edges of the HSYNC and VSYNC are taken into account for synchronization and the non-active edges are not critical. The only restriction is that both the HIGH and LOW periods of HSYNC or ODDEV signal must not be shorter than 2 clock cycles.

The phase of HSYNC relative to digital video input data can also be controlled. Normally (by default), the first clock rising edge following the HSYNC active edge samples "Cb" within YCrCb stream. Correspondingly, "Cb" of the first active pixel is sampled at the 245th or 265th CLK rising edge following the HSYNC active edge in CCIR-525 or CCIR-625 system respectively. However, by using configuration bits **syn_dl[1:0]** in REGISTER **CONFG3**, 0 to +3 clock cycles delay can be added to the period between sync and the first active "Cb" sample to cope with any data/sync phasing.

Slave Mode 2 : HSYNC + ODDEV Based

In this mode, the W9953F/W9954F accepts external HSYNC and ODDEV sync signals to perform the synchronization. The polarities of HSYNC and ODDEV can be programmed independently (bits **pol_h** and **pol_vf** in REGISTER **CONFG2**).

In this mode, HSYNC and ODDEV sync signals are registered on the rising edge of CLK. The active edge of HSYNC indicates the start of a new line and the active edge of ODDEV indicates the beginning of a new odd field but encoding of the first line does not start until an HSYNC active edge is detected (the HSYNC can active as early as the same time of ODDEV).The subsequent lines are then initialized by HSYNC active edges.

Only the active edge of the HSYNC and ODDEVE are taken into account for synchronization and the non-active edges are not critical. The only restriction is that both the HIGH and LOW periods of HSYNC or ODDEV signal must not be shorter than 2 clock cycles.

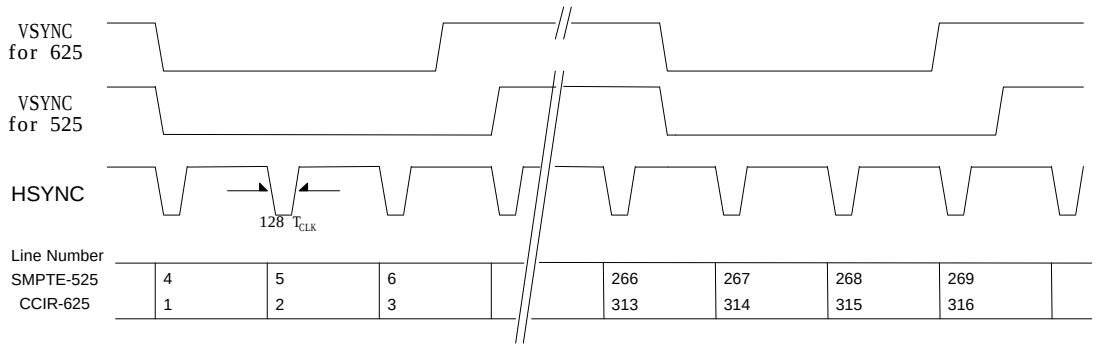
The phase of HSYNC relative to digital video input data can also be controlled. Normally (by default), the first clock rising edge following the HSYNC active edge samples "Cb" within YCrCb stream. Correspondingly, "Cb" of the first active pixel is sampled at the 245th or 265th CLK rising edge following the HSYNC active edge in CCIR-525 or CCIR-625 system respectively. However, by using configuration bits **syn_dl[1:0]** in REGISTER **CONFG3**, 0 to +3 clock cycles delay can be added to the period between sync and the first active "Cb" sample to cope with any data/sync phasing.

Slave Mode 3 : Data-embedded with HSYNC + VSYNC Output

In this mode, synchronization is performed by extracting the 'H' and 'V' flags from 'SAV' (Start of Active Video) and 'EAV' (End of Active Video) which are embedded in ITU-R656 compliant digital video streams at P[7:0]. Both the line sync signal (HSYNC) and field sync signals (VSYNC) are output on the HSYNC and VSYNC/ODDEV pins. The polarities of HSYNC and VSYNC can be programmed independently (bits **pol_h** and **pol_vf** in REGISTER **CONFG2**). The data/sync phasing also can be controlled by using configuration bits **syn_dl[1:0]** in REGISTER **CONFG3.**

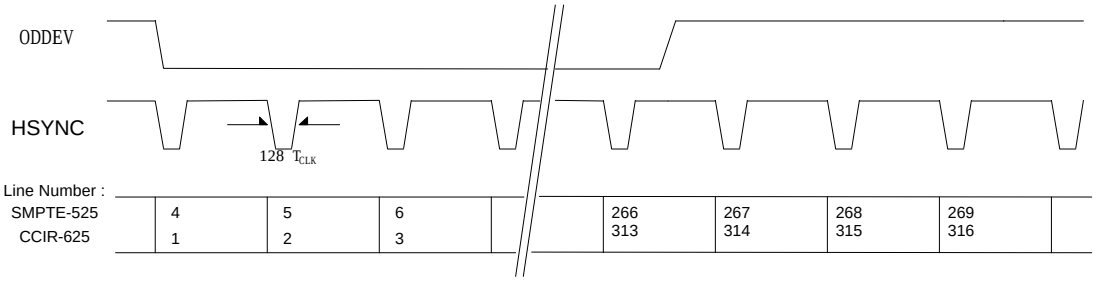
Slave Mode 4 : Data-embedded with HSYNC + ODDEV Output

In this mode, synchronization is performed by extracting the 'H' and 'V' flags from 'SAV' (Start of Active Video) and 'EAV' (End of Active Video) which are embedded in ITU-R656 compliant digital video streams at P[7:0]. Both the line sync signal (HSYNC) and frame sync signal (ODDEV) are outputs on the HSYNC and ODDEV/VSYNC pins. The polarities of HSYNC and VSYNC can be programmed independently (bits **pol_h** and **pol_vf** in REGISTER **CONFG2**). The data/sync phasing also can be controlled by using configuration bits **syn_dl[1:0]** in REGISTER **CONFG3.**



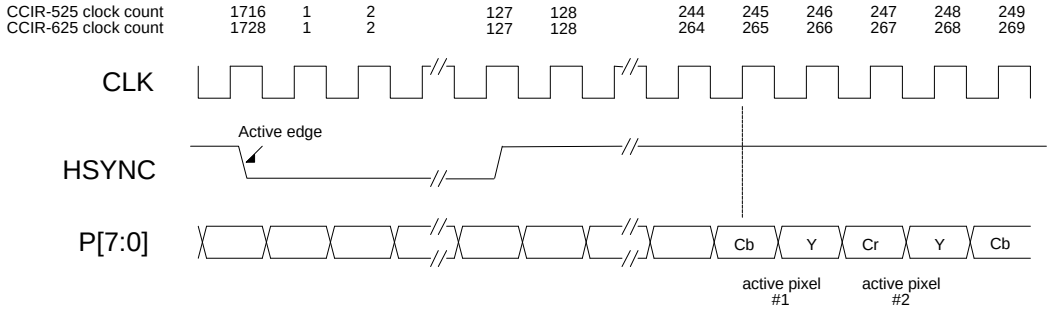
Note: polarities of VSYNC and HSYNC are programmable (default setting is shown).

Figure 5. Vertical Timing in Master Mode 1, Slave Mode 1 and Slave Mode 3



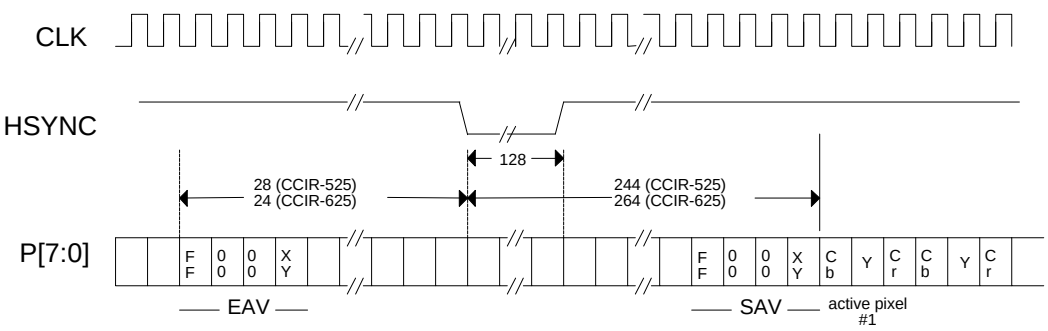
Note: polarities of ODDEV and HSYNC are programmable (default setting is shown).

Figure 6. Vertical Timing in Master Mode 2, Slave Mode 2 and Slave Mode 4



Note: Polarity and phase of HSYNC are programmable (default setting is shown)

Figure 7. Horizontal Timing in Master Mode 1, Master Mode 2, Slave Mode 1 and Slave Mode 2



Note: Polarity and phase of HSYNC are programmable (default setting is shown)

Figure 8. Horizontal Timing in Slave Mode 3 and Slave Mode 4

Crystal Oscillator

The W9953F/W9954F provides an independent crystal oscillator for double pixel clock frequency or other usage. A crystal with frequency up to 30MHz can be connected between XTALI and XTALO pins and the oscillator output can be taken from XCLK pin. Both fundamental and 3rd overtone mode crystal can be used. Of course the LC resonant circuit should be added to attenuate fundamental frequency gain when 3rd overtone crystal is used.

Luminance Encoding

The de-multiplexed Y samples are oversampled twice to ease the analog post-filtering. The transients of synchronization pulses and blanking period are also smoothed by the interpolation filter.

By programming bit **setup** in REGISTER **CONFG1,** the 7.5 IRE pedestal setup can be added to or removed from all standards.

A programmable delay can be added on the luminance path to compensate any chroma/luma delay introduced by analog post-filtering (**l_dl[2:0]** in register **CONFG3**).

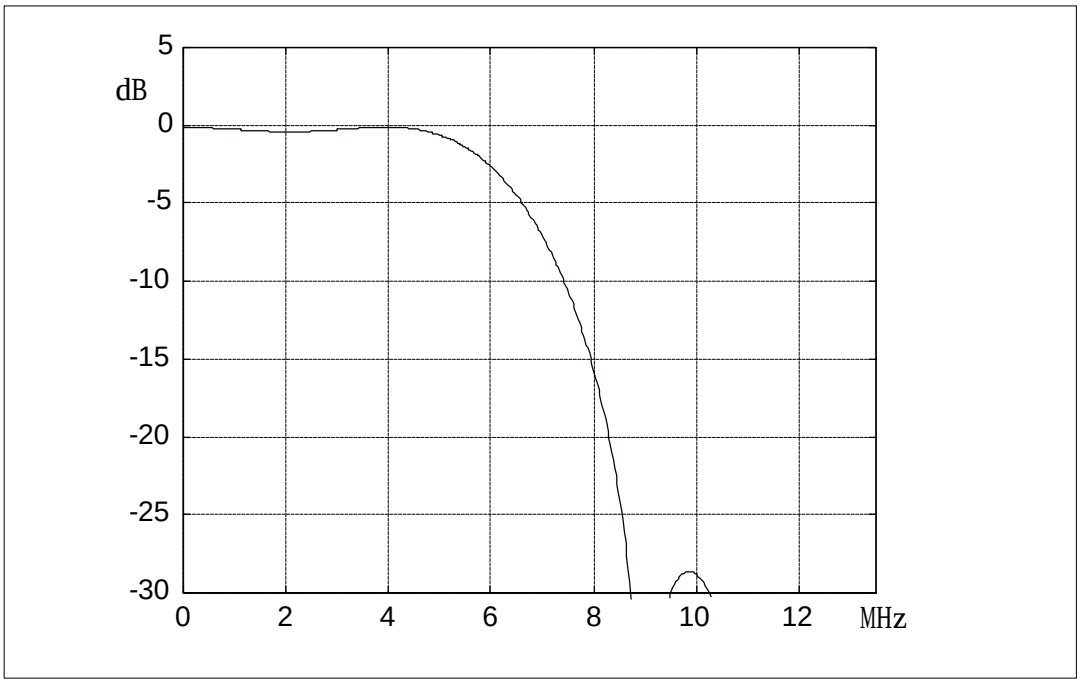


Figure 9. Luminance Upsampling Filter Response

Chrominance Encoding

De-multiplexed component color Cb and Cr samples are oversampled fourfold at clock rate to easy the analog post-filtering and allows more accurate encoding. Depending on the output standard selected, the suitable color subcarrier is generated and modulated by the chroma components to create the video chroma signal.

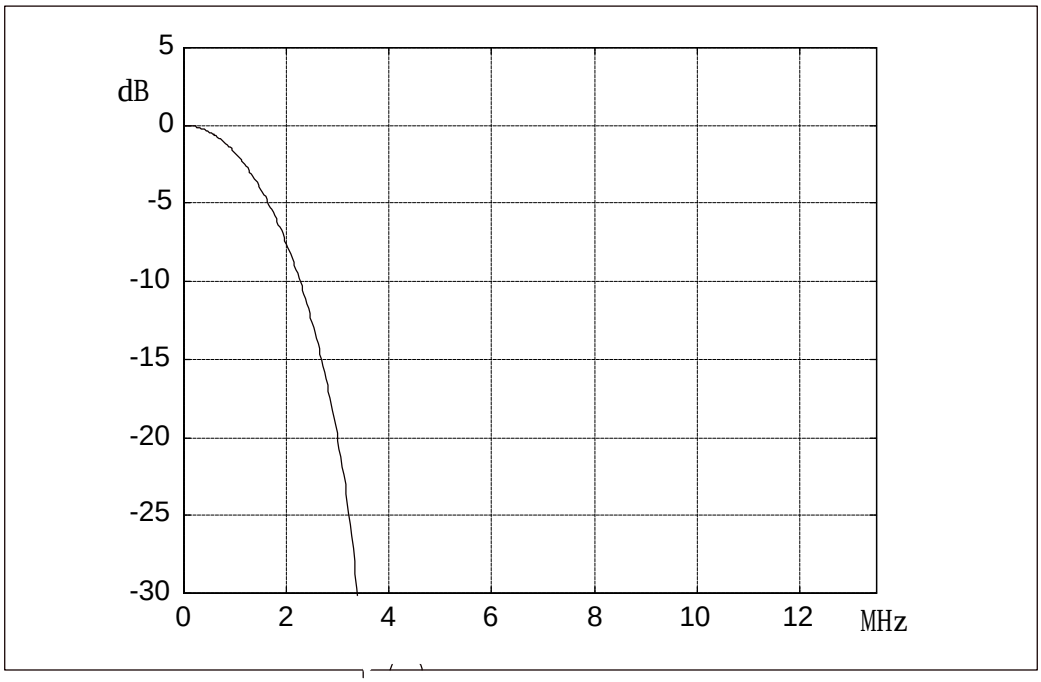


Figure 10. Chrominance filter Respond

Composite Video and S-video Outputs

Adding the luminance and the chroma signal forms the digital composite video signal. Through three 10-bit D/A converters, the digital composite signal, the digital luminance signal and the digital chrominance signal are converted to analog CVBS, Y and C signals respectively. All analog outputs are designed to drive standard video level into a doubly terminated 75 Ohms load. Unused outputs should be connected to ground. A resister (R_{SET}) connected between pin FSADJ and GND is used to adjust the full-scale output current on the D/A converters' outputs. The relationship is

$$R_{SET}(\Omega) = 2820 * V_{REF} / I_{full}\,(mA) \quad \text{for 5V VDD;}$$

or $$R_{SET}(\Omega) = 2765 * V_{REF} / I_{full}\,(mA) \quad \text{for 3.3V VDD.}$$

Connection diagram of the analog portion of W9953F/W9954F with a typical Low pass filter design is illustrated in Fig.11.

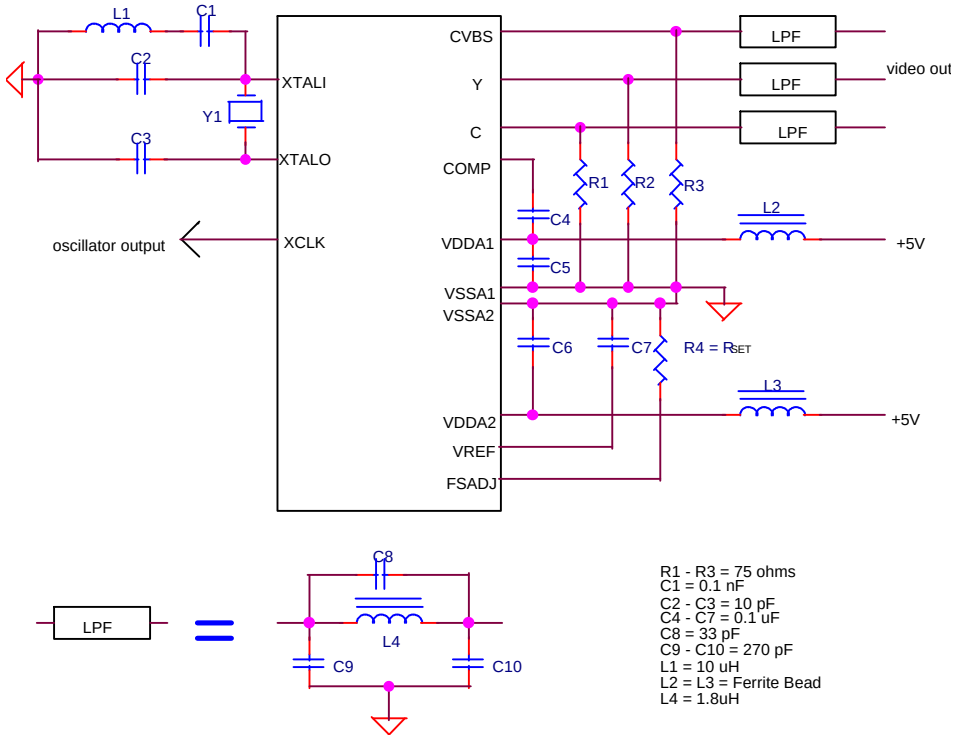


Figure 11. Typical Connection Diagram

Closed Captioning

The W9953F/W9954F can be programmed to insert a Closed Caption signal on a certain line within a wide range on ODD and/or EVEN fields in both NTSC and PAL modes. Closed captioning has priority over any configurations of the encoder: it will override any CGMS, Macrovision anticopy signals or even the video data (and any 7.5 IRE pedestal setup) for the same line.

Two byte data pairs are encoded for each field. The data is delivered to the register through the I^2C interface. There are four registers (registers **CC_O1, CC_O2**, **CC_E1** and **CC_E2**) for holding the data - two bytes per field. The W9953F/W9954F automatically generates the required clock run in and start bit. When closed-captioning is enabled, the system controller should load the data registers once each frame at most. Two bits of REGISTER **STATUS** are used to regulate loading rate (**cco_ rdy** and **cce_ rdy**). The closed caption encoder considers that closed caption data has been updated on completion of the write operation into REGISTER **CC_O2** for the odd field, or into REGISTER **CC_E2** for the even field. If the closed captioning encoding has been enabled and the data bytes have not been updated when the encoder begins producing a line for closed caption insertion, then two NULL bytes (hex 00 with odd parity) will be sent.

The data rate is 32 times the horizontal line frequency. Data "0" at the output of the DACs corresponds to 0 IRE, data "1" at outputs of the DACs corresponds to 50 IRE. Refer to Fig.12.

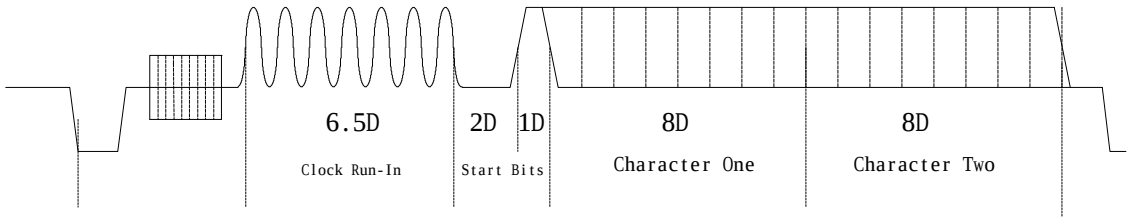


Figure 12. Closed-caption Waveform

Wide Screen Signaling (WSS) / Copy Generation Management System (CGMS) Encoding

Both EIAJ CPX-1024 (for 525 Line System) and ITU-R BT.1119 (for 625-Line System) based WSS/CGMS data can be encoded by W9953F/W9954F. When WSS/CGMS encoding is enabled, the WSS/CGMS waveform is continuously present once in each field, on lines 20 and/or 283 (525-SMPTE line number convention) for 525 Line System or on lines 23 and/or 336 (625-CCIR/ITU-R line number convention) for 625 Line System. WSS/CGMS data has priority over Macrovision anticopy signals for the same line.

The WSS/CGMS data bits are delivered to the chip via the I^2C bus (REGISTERs **WSS_O[1..3]** for the odd field, **WSS_E[1..3]** for the even field). The WSS/CGMS encoder considers that new WSS/CGMS data has been updated on completion of the write operation into REGISTER **WSS_O3** for the odd field and **WSS_E3** for the even field. Two bits of REGISTER **STATUS** are used to regulate loading rate (**wsso_ rdy** and **wsse_ rdy**).

525-Line System (NTSC-M, PAL-M):

The reference bits (' 1 0 ') are generated locally by the W9953F/W9954F and encoded first, then followed by the 20 WSS/CGMS data bits with **wsso1** (or **wsse1**) shifted out first. Refer to Fig.13 for a typical waveform.

625-Line System (PAL-B, D, G, H, I, N_C):

The run-in code and start code are generated locally by the W9953F/W9954F and encoded first, then followed by the 14 WSS/CGMS data bits with **wsso1** (or **wsse1**) shifted out first. Refer to Fig.14 for a typical waveform. Note that although **WSS_O3** (**WSS_E3** for the even field) contains useless data in 625-line system, all three registers must be written to complete a data update process (you can fill in it with 00H for example).

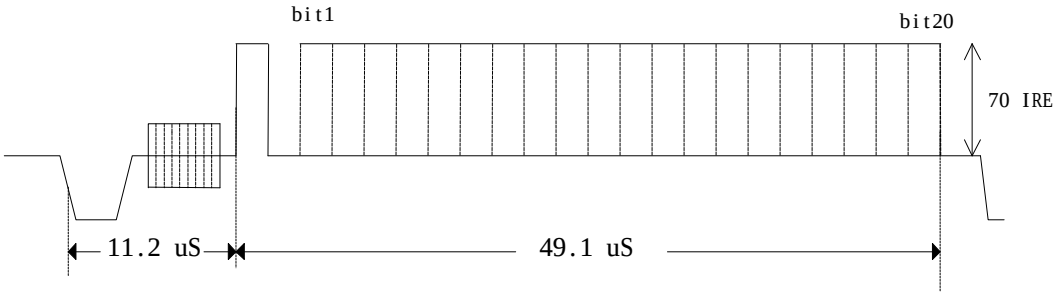


Figure 13. 525-Line WSS/CGMS Waveform

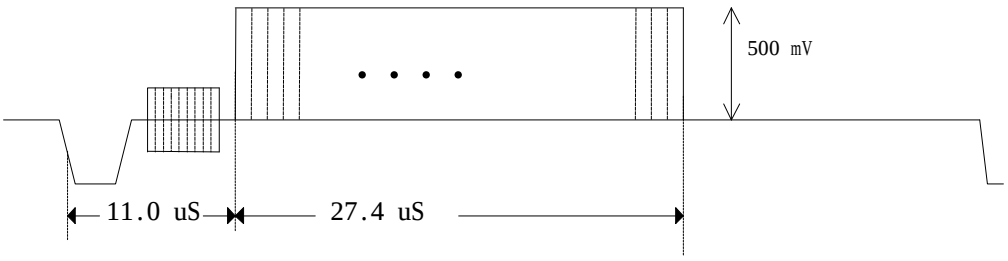


Figure 14. 625-Line WSS/CGMS Waveform

Teletext Encoding

The W9953F/W9954F is able to encode Teletext according to the PAL-WST and NABTS specifications. Teletext data are delivered to the encoder via TTX pin, and the request signal, TTXRQ, from W9953F/W9954F is used to indicate the timing to transmit the data bit stream. At each rising edge of output signal TTXRQ, a teletext data bit has to be provided after a programmable delay (t_{PD}) at TTX pin. t_{PD} can be adjusted by programming **txdl[2:0]** in register **CONFG4.** Data is clocked synchronously with the master clock (CLK) at an average rate the same with that TTXRQ signal has. Bitstream phase is internally adjusted to eliminate the phase jitters on the output signal to a sufficient small level.

ttx_en in **CONFG2** enable the teletext encoding function. Bits **txlo1** ~ **txlo17** of REGISTERs **LINE_O[1:3]** and **txle1** ~ **txle17** of REGISTERs **LINE_E[1:3]** indicate which lines are used to encode the teletext data for odd fields and even fields respectively. The teletext timing is shown in Fig.15 and Fig.16. Time t_{TTXWin} is the insertion window for TTX data; its length is fixed to 360 teletext bits at rate of 6.9375 Mbits/s (PAL-WST) or 288 teletext bits at rate of 5.7272 Mbits/s (NABTS).

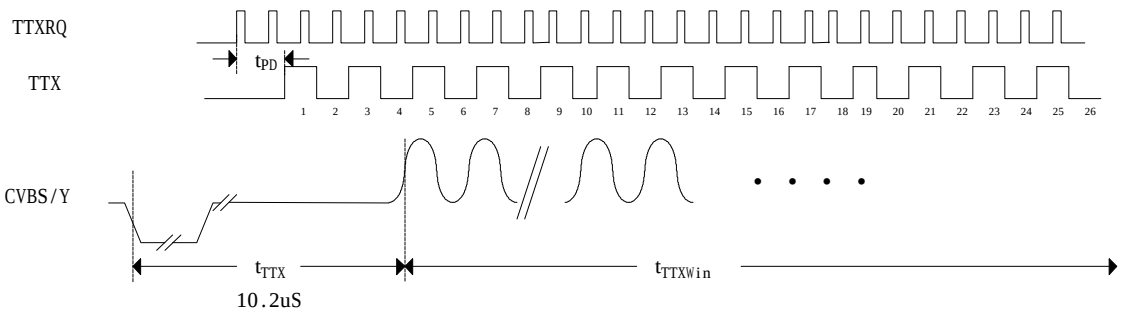


Figure 15. Teletext Timing

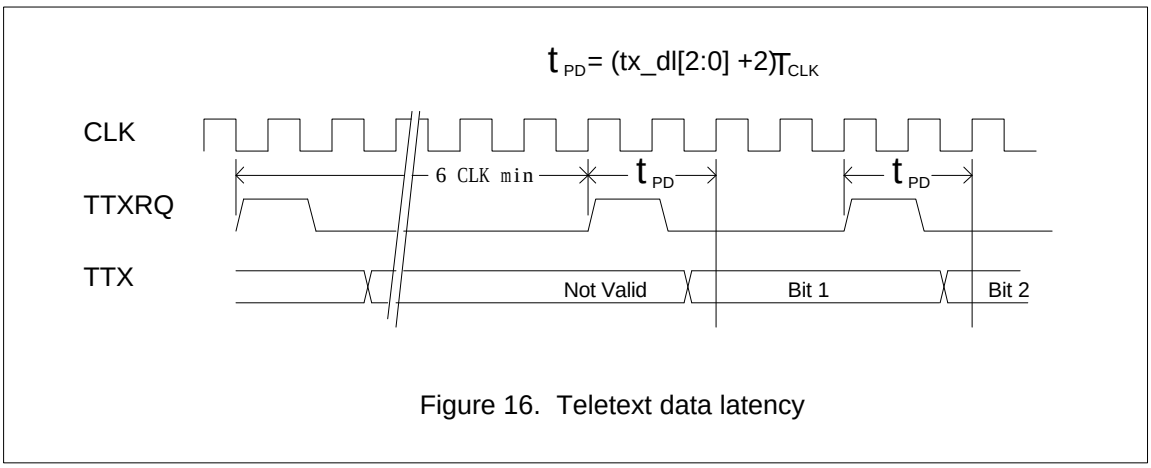


Figure 16. Teletext data latency

Macrovision (W9953F Only)

The W9953F allows MACROVISION 7.0 antitaping process. All luminance, chrominance and composite video waveforms include the MACROVISION Antitaping Process.

The W9953F may be purchased by Macrovision Authorized Buyers only. The W9953F incorporates Macrovision antitaping process technology that is protected by U.S. patent numbers 4,631,601, 4,577,216 and 4,819,098 and other intellectual property rights. The use of Macrovision's copy protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-per-view uses only. Reverse engineering or disassembly is prohibited. For more information please contact Winbond sales office.

Internal Color Bars

The W9953F/W9954F can be configured to produce a " 100% saturation, 100% amplitude " color bar pattern internally. The "internal color bar" mode can be invoked by programming the bits **sync[2:0]** in REGISTER **CONFG1.** When internal color bar signal is generated the synchronization will be switched to master HSYNC + VSYNC mode, so that HSYNC and VSYNC signals are outputs.

The typical video output waveforms of the color bar are shown in Fig.17 and Fig.18.

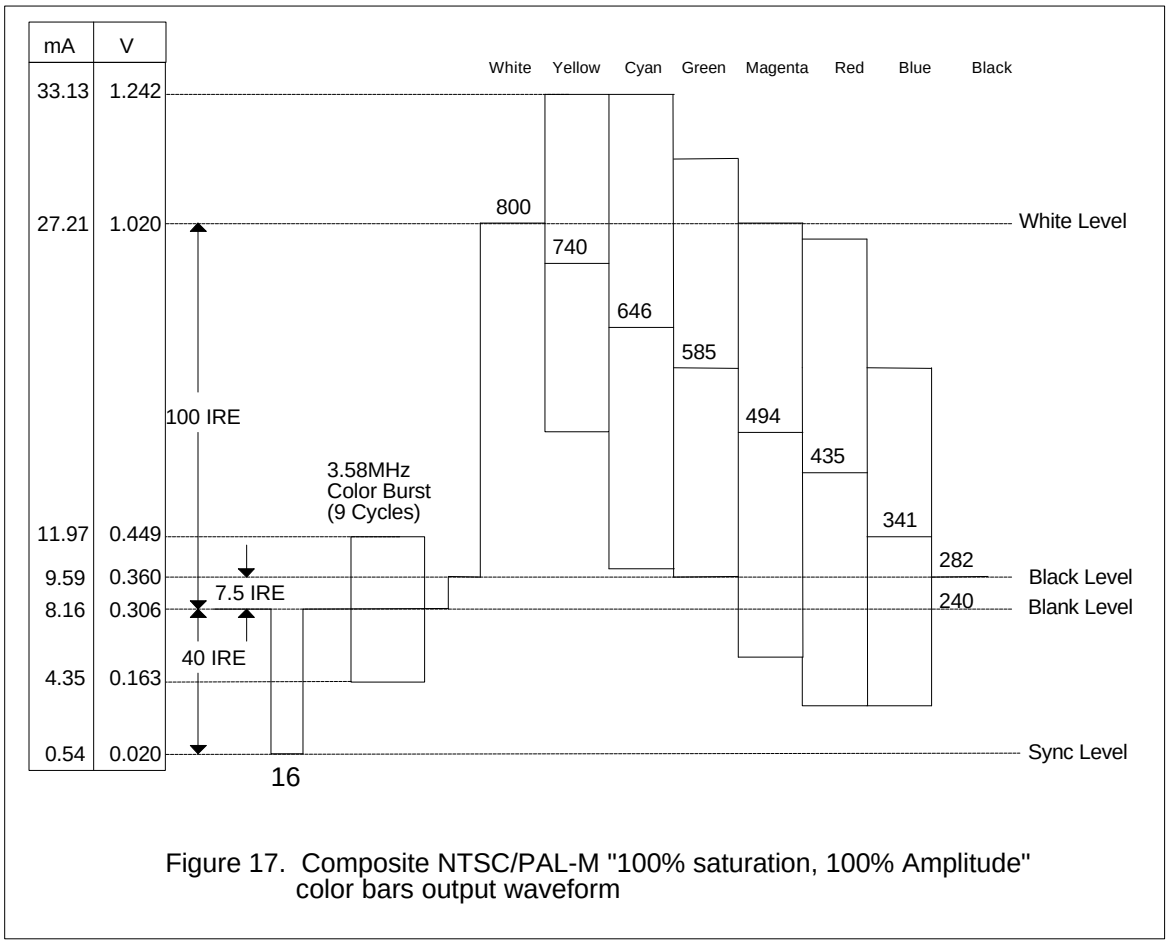


Figure 17. Composite NTSC/PAL-M "100% saturation, 100% Amplitude" color bars output waveform

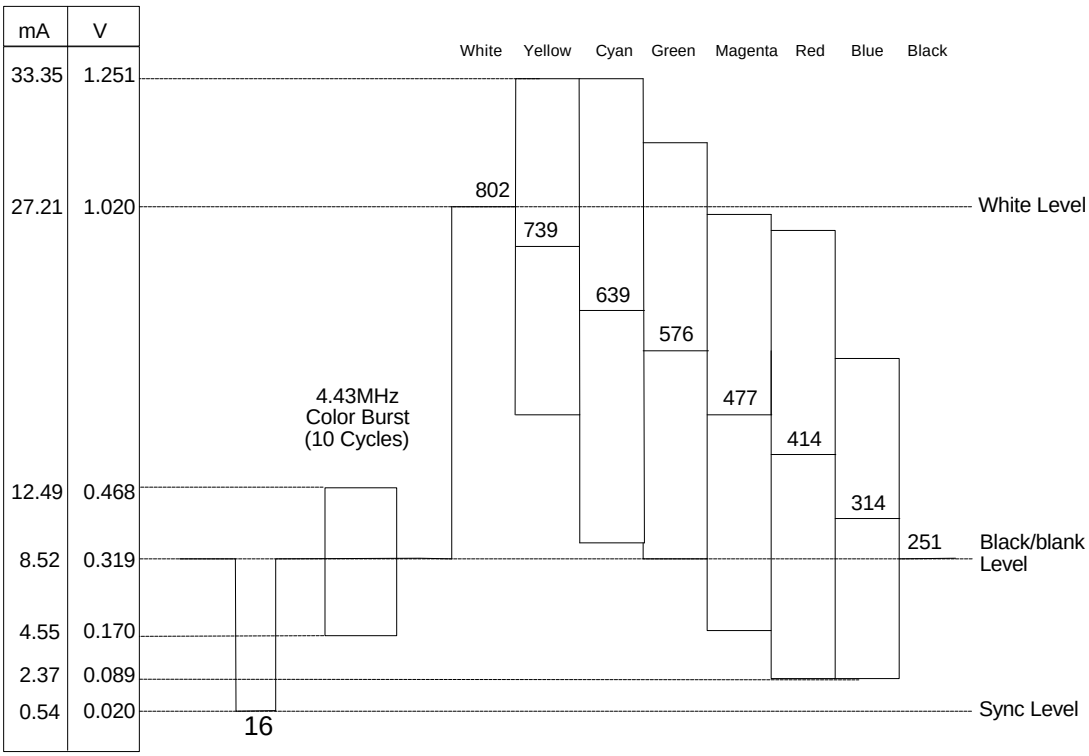


Figure 18. Composite PAL-B,D,G,H,I,N "100% saturation, 100% Amplitude" color bars output waveform

Power-Down Mode

Set SLEEP pin to "1" will turn the device into sleep mode. In sleep mode, the analog circuits except the on chip oscillator are shut down, and the internal clock is held constant, making the analog and digital current draw to a minimum. In sleep mode, all functions of this chip (including outputs and I^2C bus) are disabled but the contents of registers will be preserved. The on chip oscillator is not affected by sleep mode to provide an unbroken output. If the current consumed by oscillator is not permitted when in SLEEP mode, the on chip oscillator should not be used, and connect it's input pin to ground to minimize the power consumption.

Besides shutting down the entire chip, any unused DAC may be individually power down by software control to it's corresponding **daoff**_X bit in REGISTER **CONFG4** to save the system power.

I²C Interface

Control of the internal registers is accomplished through the fast-mode I²C interface. The device acts as a slave for receiving and transmitting data over the serial bus with rate up to 400 kbps. The slave address is chosen at reset as either 40H (AS input pin = 0) or 42H (AS input pin = 1).

Registers have 8-bit sub-address (in fact, only the 6 LSB are effective). All registers are writable and readable except for **CHIP_ID** (add = 3EH) and **STATUS** (add. = 3FH) which are read-only. The subaddress will be incremented automatically in writing/reading cycles unless the sub-address = 3FH. In reading REGISTER **STATUS**, the subaddress (3FH) will not increased automatically for convenience of polling operation. The microcontroller can repeatedly read the status register until the status which the microcontroller is waiting for happens. Write and read operations are detailed in Fig.19 and Fig.20.

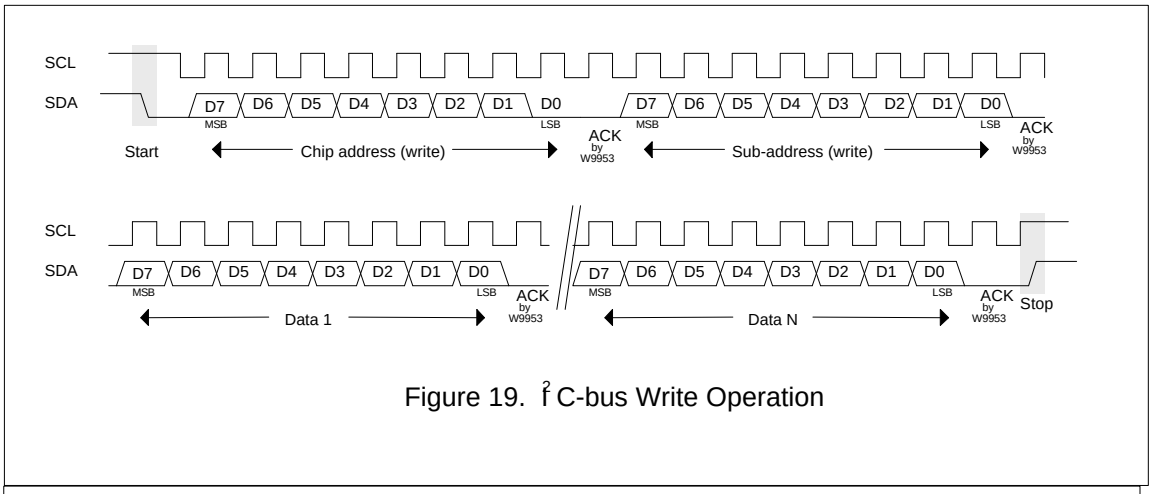


Figure 19. I²C-bus Write Operation

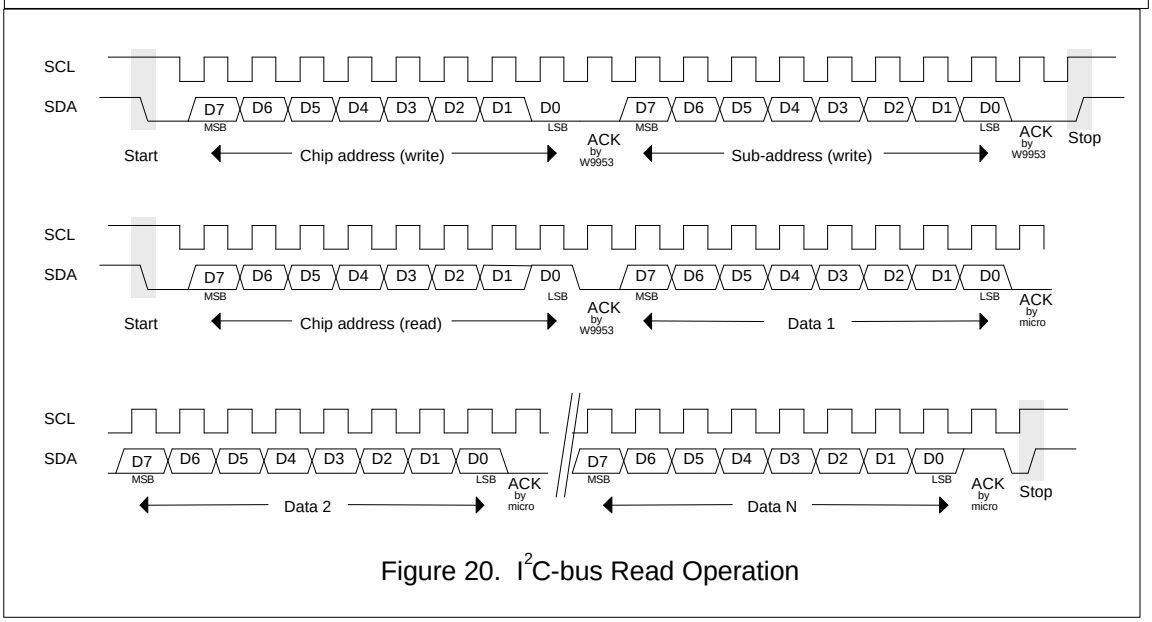


Figure 20. I²C-bus Read Operation

REGISTERS

Register Mapping (not including Macrovisin Process registers)

Register	R/W	Sub-add	D7	D6	D5	D4	D3	D2	D1	D0
CONFG1	R/W	00H	format1	format0	setup	no_intl	0	sync2	sync1	sync0
CONFG2	R/W	01H	pol_h	pol_vf	ex_rang	wsse_en	wsso_en	cce_en	cco_en	ttx_en
CONFG3	R/W	02H	0	0	syn_dl1	syn_dl0	sc_free	l_dl2	l_dl1	l_dl0
CONFG4	R/W	03H	tx_dl2	tx_dl1	tx_dl0	black	no_col	daoff_v	daoff_y	daoff_c
SRESET	R/W	04H	0	0	0	0	0	0	0	sof_rst
LINE_O1	R/W	05H	txlo8	txlo7	txlo6	txlo5	txlo4	txlo3	txlo2	txlo1
LINE_O2	R/W	06H	txlo16	txlo15	txlo14	txlo13	txlo12	txlo11	txlo10	txlo9
LINE_O3	R/W	07H	cclo4	cclo3	cclo2	cclo1	cclo0	0	0	txlo17
LINE_E1	R/W	08H	txle8	txle7	txle6	txle5	txle4	txle3	txle2	txle1
LINE_E2	R/W	09H	txle16	txle15	txle14	txle13	txle12	txle11	txle10	txe9
LINE_E3	R/W	0AH	ccle4	ccle3	ccle2	ccle1	ccle0	0	0	txle17
CC_O1	R/W	0BH	cco7	cco6	cco5	cco4	cco3	cco2	cco1	cco0
CC_O2	R/W	0CH	cco15	cco14	cco13	cco12	cco11	cco10	cco9	cco8
CC_E1	R/W	0DH	cce7	cce6	cce5	cce4	cce3	cce2	cce1	cce0
CC_E2	R/W	0EH	cce15	cce14	cce13	cce12	cce11	cce10	cce9	cce8
WSS_O1	R/W	0FH	wsso8	wsso7	wsso6	wsso5	wsso4	wsso3	wsso2	wsso1
WSS_O2	R/W	10H	0	0	wsso14	wsso13	wsso12	wsso11	wsso10	wsso9
WSS_O3	R/W	11H	0	0	wsso20	wsso19	wsso18	wsso17	wsso16	wsso15
WSS_E1	R/W	12H	wsse8	wsse7	wsse6	wsse5	wsse4	wsse3	wsse2	wsse1
WSS_E2	R/W	13H	0	0	wsse14	wsse13	wsse12	wsse11	wsse10	wsse9
WSS_E3	R/W	14H	0	0	wsse20	wsse19	wsse18	wsse17	wsse16	wsse15
reserved	xxx	15H	xxx	xxx	xxx	xxx	xxx	xxx	xxx	xxx
…	…	…	…	…	…	…	…	…	…	…
reserved	xxx	3DH	xxx	xxx	xxx	xxx	xxx	xxx	xxx	xxx
CHIP_ID	R	3EH	id3	id2	id1	id0	ver3	ver2	ver1	ver0
STATUS	R	3FH	field2	field1	field0	0	wsse_rdy	wsso_rdy	cce_rdy	cco_rdy

Note: 1. All bits label '0' must be programmed with logic 0 to ensure proper operation.

2. The reserved REGISTERs must be kept from access.

Register Contents and Description

REGISTER **CONFG1**: configuration 1

Sub-address = 00 H								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	format1	format0	setup	no_intl	0	sync2	sync1	sync0
Reset value	0	0	1	0	0	0	0	0

format[1:0] : TV standard format select (proper setting of setup bit is required)

0 0 NTSC-M

0 1 PAL-M

1 0 PAL-B,D,G,H,I

1 1 PAL-N_C

setup : Pedestal enable

0 Black level = 0 IRE

1 Black level is 7.5 IRE above blanking level on all lines outside VBI

no_intl : Non-interlaced mode select

0 Interlaced mode (525/60 or 625/50 system)

1 Non-interlaced mode (2x262/60 or 2x312/50 system)

sync[2:0] : Synchronization mode select

0 0 0 Slave Mode 1 : HSYNC + VSYNC Based synchronization

0 0 1 Slave Mode 2 : HSYNC + ODDEV Based synchronization

0 1 0 Slave Mode 3 : Data-embedded with HSYNC + VSYNC Output synchronization

0 1 1 Slave Mode 4 : Data-embedded with HSYNC + ODDEV Output synchronization

1 0 0 Master Mode 1 : HSYNC + VSYNC Based synchronization

1 0 1 Master Mode 2 : HSYNC + ODDEV Based synchronization

1 1 0 Internal 100% color bar pattern

1 1 1 Reserved

REGISTER **CONFG2** : configuration 2

Sub-address = 01 H								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	pol_h	pol_vf	ex_rang	wsse_en	wsso_en	cce_en	cco_en	ttx_en
Reset value	0	0	0	0	0	0	0	0

pol_h : Polarity of HSYNC select

0 HSYNC is a negative pulse with 128 T_{CLK} width when output or falling edge active when input.

1 HSYNC is a positive pulse with 128 T_{CLK} width when output or rising edge active when input.

pol_vf : Polarity of ODDEV/VSYNC select

0 Low level of ODDEV indicates odd fields, and high level indicates even fields.
VSYNC is falling edge active.

1 High level of ODDEV indicates odd fields, and low level indicates even fields.
VSYNC is rising edge active.

ex_rang : Enlarge the dynamic magnitude allowed on YCrCb input.

0 16 to 235 for Y, 16 to 240 for Cr and Cb.

1 1 to 254 for Y,Cr and Cb

wsse_en : Even field WSS/CGMS encoding enable

0 Disabled

1 Enabled

wsso_en : Odd field WSS/CGMS encoding enable

0 Disabled

1 Enabled

cce_en : Even field closed caption encoding enable

0 Disabled

1 Enabled

cco_en : Odd field closed caption encoding enable

0 Disabled

1 Enabled

ttx_en : Teletext encoding enable

0 Disabled

1 Enabled

REGISTER **CONFG3** : configuration 3

Sub-address = 02 H								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	0	0	syn_dl1	syn_dl0	sc_free	l_dl2	l_dl1	l_dl0
Reset value	0	0	0	0	0	0	0	0

syn_dl[1:0] : Sync signals (both incoming and outgoing) phase adjustment

Used to adjust the phase relationship between the incoming video samples and sync signals so the YCrCb sequence can be properly interpreted.

syn_dl[1:0]:	delay added to the duration between HSYNC and ODDEV/VSYNC and the first active pixel. (clock = CLK period)
1 1	+3 clock delay
1 0	+2 clock delay
0 1	+1 clock delay
0 0	Normal (+0 clock delay)

sc_free : Free running of subcarrier phase

Resetting the subcarrier phase forces the value of the accumulator of the DDS (Direct Digital Synthesizer) to its nominal value to avoid accumulating errors so maintaining correct SC-H phasing.

0 The subcarrier phase is reset to zero at the beginning of each field sequence.

1 Free running

l_dl[2:0] : Luminance path delay adjustment

The adjustment range is from -3 CLK delay to +3 CLK delay.

l_dl[2:0]:	delay on luma path with reference to chroma path (CLK period)
0 1 1	+3
0 1 0	+2
0 0 1	+1
0 0 0	Normal (+0 delay)
1 0 1	-1
1 1 0	-2
1 1 1	-3
1 0 0	Reserved

Note: l_dl[2:0] should be set to "011" to compensate the internal 105ns chroma path delay of version 0 chips.

REGISTER **CONFG4** : configuration 4

Sub-address = 03 H								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	tx_dl2	tx_dl1	tx_dl0	black	no_col	daoff_v	daoff_y	daoff_c
Reset value	0	0	0	0	0	0	0	0

tx_dl[2:0] : Teletext data latency

These register bits indicates the delay between rising edge of TTXRQ output and the sampling point of valid data on pin TTX. The W9953F/W9954F will clock in the Teletext data samples on the (2 + tx_dl[2:0])th rising edge of the CLK following each rising edge of TTXRQ signal which is supplied by the W9953F/W9954F to synchronize the teletext data exchange. The minimum delay is 2 CLK cycles (dl[2:0] = 0).

black : Enable black burst

0 Normal video signals are output

1 Enable black burst. Video is blanked on all lines for CVBS and Y outputs, and black for C output.

no_col : Disable color signal

0 Color On

1 Color suppressed on CVBS output signal but color still present on C output.

daoff_v : Power-down the CVBS output DAC

0 Normal operation.

1 Disable the CVBS output DAC. This will reduce the analog supply current but have no effect on the digital current and Y/C outputs.

daoff_y : Power-down the Y output DAC

0 Normal operation.

1 Disable the luminance (Y) output DAC. This will reduce the analog supply current but have no effect on the digital current and CVBS and C outputs.

daoff_c : Power-down the C output DAC

0 Normal operation.

1 Disable the chrominance (C) output DAC. This will reduce the analog supply current but have no effect on the digital current and CVBS and Y outputs.

REGISTER **SRESET** : software reset

Sub-address = 04 H								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	0	0	0	0	0	0	0	sof_rst
Reset value	0	0	0	0	0	0	0	0

sof_rst : Software reset

Software reset acts like hardware reset; all registers are set to their default reset values.

0 No reset

1 Software reset. This bit will be automatically reset (to "0") after internal reset process.

REGISTER **LINE_O1, LINE_O2, LINE_O3** :teletext line map and closed caption line for odd fields

LINE_O1: Sub-address = 05H								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	txlo8	txlo7	txlo6	txlo5	txlo4	txlo3	txlo2	txlo1
Reset value	0	0	0	0	0	0	0	0
LINE_O2: Sub-address = 06H								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	txlo16	txlo15	txlo14	txlo13	txlo12	txlo11	txlo10	txlo9
Reset value	0	0	0	0	0	0	0	0
LINE_O3: Sub-address = 07H								

	D7	D6	D5	D4	D3	D2	D1	D0
Content	cclo_4	cclo_3	cclo_2	cclo_1	cclo_0	0	0	txlo17
Reset value	0	1	1	1	1	0	0	0

Teletext lines (odd fields):

Register bits **txlo1** through **txlo17** allow to map the TV lines in odd fields where teletext data is to be encoded.

- 525/60 system: (525-SMPTE line number convention)

txloN = 1 enables the $(5+N)^{th}$ line in the odd field. For example, **txlo6** = 1 and **txlo10** = 1 enable line 11 and 15 respectively. Any combination of lines 10 to 22 can be defined to insert teletext data by appropriate setting of this map (the setting of **txlo1** to **txlo4** will be ignored).

- 625/50 system (625-CCIR/ITU-R line number convention)

txloN = 1 enables the $(5+N)^{th}$ line in the odd field. For example, **txlo6** = 1and **txlo10** = 1 enable line 11 and 15 respectively. Any combination of lines 6 to 22 can be defined to insert teletext data by appropriate setting of this map.

Closed caption line (odd fields):

cclo[4:0] selects the TV line in odd fields where closed caption or extended data are encoded.

- 525/60 system: (525-SMPTE line number convention)

cclo[4:0] = N selects line (N+6) for closed caption or extended data services. N < 4 corresponds to lines 6 through 9 will be ignored because these lines contain synchronizing and equalizing pulses. In normal condition, only lines 10 through 22 should be used (N = 4 to 16).

- 625/50 system (625-CCIR/ITU-R line number convention)

cclo[4:0] = N selects line (N+6) for closed caption or extended data services. N = 0 corresponds to lines 6 will be ignored (no line is selected). In normal condition, only lines 7 through 23 should be used (N = 1 to 17).

REGISTER **LINE_E1, LINE_E2, LINE_E3** : teletext lines map and closed caption line for even fields

LINE_E1: Sub-address = 08H								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	txle8	txle7	txle6	txle5	txle4	txle3	txle2	txle1
Reset value	0	0	0	0	0	0	0	0
LINE_E2: Sub-address = 09H								

	D7	D6	D5	D4	D3	D2	D1	D0
Content	txle16	txle15	txle14	txle13	txle12	txle11	txle10	txle9
Reset value	0	0	0	0	0	0	0	0
LINE_E3: Sub-address = 0AH								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	ccle_4	ccle_3	ccle_2	ccle_1	ccle_0	0	0	txle17
Reset value	0	1	1	1	1	0	0	0

Teletext lines (even fields):

Register bits **txle1** through **txle17** allow to map the TV lines in even fields where teletext data is to be encoded.

-525/60 system: (525-SMPTE line number convention)

txleN = 1 enables the $(268+N)^{th}$ line in the even field. For example, **txle6** = 1 and **txle10** = 1 enable line 274 and 278 respectively. Any combination of lines 273 to 285 (the setting of **txle1** to **txle4** will be ignored) can be defined to insert teletext data by appropriate setting of this map.

- 625/50 system (625-CCIR/ITU-R line number convention)

txleN = 1 enables the $(317+N)^{th}$ line in the even field. For example, **txle6** = 1 and **txle10** = 1 enable line 323 and 327 respectively. Any combination of lines 318 to 334 can be defined to insert teletext data by appropriate setting of this map.

Closed caption line (even fields):

ccle[4:0] selects the TV line in even fields where closed caption or extended data are encoded.

- 525/60 system: (525-SMPTE line number convention)

ccle[4:0] = N selects line (N+269) for closed caption or extended data services. N < 4 corresponds to lines 269 through 272 will be ignored because these lines contain synchronizing and equalizing pulses. In normal condition, only lines 273 through 284 should be used (N = 4 to 15).

- 625/50 system (625-CCIR/ITU-R line number convention)

ccle[4:0] = N selects line (N+318) for closed caption or extended data services. N = 0 corresponds to lines 318 will be ignored (no line is selected). In normal condition, only lines 319 through 336 should be used (N = 1 to 18).

REGISTER **CC_O1, CC_O2** : closed caption data to be encoded in odd fields

CC_O1 : Sub-address = 0B H								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	cco7	cco6	cco5	cco4	cco3	cco2	cco1	cco0
Reset value	1	0	0	0	0	0	0	0
CC_O2: Sub-address = 0C H								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	cco15	cco14	cco13	cco12	cco11	cco10	cco9	cco8
Reset value	1	0	0	0	0	0	0	0

cco[7:0] is the first byte of captioning data for the odd field. MSB (**cco7**) is used to carry the odd-parity bit (not computed internally). The encoding sequence is LSB (**cco0**) first.

cco[15:8] is the second byte of captioning data for the odd field. MSB (**cco15**) is used to carry the odd-parity bit (not computed internally). The encoding sequence is LSB (**cco8**) first.

REGISTER **CC_E1, CC_E2** : closed caption data to be encoded in even fields

CC_E1 : Sub-address = 0D H								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	cce7	cce6	cce5	cce4	cce3	cce2	cce1	cce0
Reset value	1	0	0	0	0	0	0	0
CC_E2: Sub-address = 0E H								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	cce15	cce14	cce13	cce12	cce11	cce10	cce9	cce8
Reset value	1	0	0	0	0	0	0	0

cce[7:0] is the first byte of captioning data for the even field. MSB (**cce7**) is used to carry the odd-parity bit (not computed internally). The encoding sequence is LSB (**cce0**) first.

cce[15:8] is the second byte of captioning data for the even field. MSB (**cce15**) is used to carry the odd-parity bit (not computed internally). The encoding sequence is LSB (**cce8**) first.

REGISTER **WSS_O1, WSS_O2, WSS_O3 :** odd field WSS/CGMS data

WSS_O1 : Sub-address = 0FH								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	wsso8	wsso7	wsso6	wsso5	wsso4	wsso3	wsso2	wsso1
Reset value	0	0	0	0	0	0	0	0
WSS_O2: Sub-address = 10H								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	0	0	wsso14	wsso13	wsso12	wsso11	wsso10	wsso9
Reset value	0	0	0	0	0	0	0	0
WSS_O3: Sub-address = 11H								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	0	0	wsso20	wsso19	wsso18	wsso17	wsso16	wsso15
Reset value	0	0	1	1	1	1	1	1

wsso[1:14]: 14 bit WSS/CGMS data information for odd fields

The encoding sequence is **wsso1** first.

wsso[15:20]: 6 bit CRC for odd field in 525-Line WSS/CGMS operation: (not internally computed)

It is ignored during 625-Line WSS/CGMS operation.

REGISTER **WSS_E1, WSS_E2, WSS_E3 :** even field WSS/CGMS data

WSS_E1 : Sub-address = 12H								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	wsse8	wsse7	wsse6	wsse5	wsse4	wsse3	wsse2	wsse1
Reset value	0	0	0	0	0	0	0	0
WSS_E2: Sub-address = 13H								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	0	0	wsse14	wsse13	wsse12	wsse11	wsse10	wsse9
Reset value	0	0	0	0	0	0	0	0
WSS_E3: Sub-address = 14H								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	0	0	wsse20	wsse19	wsse18	wsse17	wsse16	wsse15
Reset value	0	0	1	1	1	1	1	1

wsse[1:14]: 14 bit WSS/CGMS data infomation for the even field

The encoding sequence is **wsse1** first.

wsso[15:20]: 6 bit CRC for the even field in 525-Line WSS/CGMS operation: (not internally computed). It is ignored during 625-Line WSS/CGMS operation.

REGISTER **CHIP_ID** : identification register

Sub-address = 3E H								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	id3	id2	id1	id0	ver3	ver2	ver1	ver0
Reset value	0	0	1	1/0	0	0	0	0

id[3:0] : Chip identity, "0011" for W9953F; "0010" for W9954F

ver[3:0] : Version number; for this revision, **ver[3:0]** = "0000"

This read only register gives the release number of the chip for identification.

REGISTER **STATUS** : status and chip identity

Sub-address = 3F H								
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Content	field2	field1	field0	0	wsse_rdy	wsso_rdy	cce_rdy	cco_rdy
Reset value	0	0	0	0	1	1	1	1

field[2:0] : Indicates the field number

The relationship between phase of sub-carrier burst and the sync pulse is repeated at rate of 4 fields for NTSC-M or PAL-M and at 8 fields for the other formats. When the first field of a sequence is being encoded, **field[2:0]** is "'000".

000 The first field is being encoded

001 The second field is being encoded

:

111 The eighth field is being encoded

wsse_rdy : Ready for new WSS/CGMS data for even fields

wsse_rdy indicates whether the encoder is ready or not for accepting a new set of WSS/CGMS bytes for the even field. This bit is reset after REGISTER **WSS_E3** has been written a new data byte and is set immediately after the data in REGISTER **WSS_E[1:3]** have been encoded. (at the beginning of the horizontal sync of the next line to the one where **WSS_E[1:3]** data is inserted).

0 There are WSS/CGMS data in REGISTERs **WSS_E[1:3]** still not encoded yet.

1 WSS/CGMS data of the even field have been encoded.

wsso_rdy : Ready for new WSS/CGMS data for odd fields

wsso_rdy indicates whether the encoder is ready or not for accepting a new set of WSS/CGMS bytes for the odd field. This bit is reset after register **WSS_O3** has been written a new data byte and is set immediately after the data in register **WSS_O[1:3]** have been encoded. (at the beginning of the horizontal sync of the next line to the one where **WSS_O[1:3]** data is inserted).

0 There are WSS/CGMS data in registers **WSS_O[1:3]** still not encoded yet.

1 WSS/CGMS data of the odd field have been encoded.

cce_rdy : Ready for new closed caption data for even fields

cce_rdy indicates whether the encoder is ready or not for accepting a new couple of closed caption bytes for the odd field. This bit is reset after register **CC_E2** has been written a new data byte and is set immediately after the data in register **CC_E1** and **CC_E2** have been encoded. (at the beginning of the horizontal sync of the next line to the one where closed caption data is inserted).

0 There are closed caption data in registers **CC_E2** and **CC_E1** still not encoded yet.

1 Closed caption data of the even field have been encoded.

cco_rdy : Ready for new closed caption data for odd fields

cco_rdy indicates whether the encoder is ready or not for accepting a new couple of closed caption bytes for the odd field. This bit is reset after register **CC_O2** has been written a new data byte and is set immediately after the data in register **CC_O1** and **CC_O2** have been encoded. (at the beginning of the horizontal sync of the next line to the one where closed caption data is inserted).

0 There are closed caption data in registers **CC_O2** and **CC_O1** still not encoded yet.

1 Closed caption data of the even field have been encoded.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	CONDITION	RATING	UNIT
V_{DDA} and V_{DDD}	V_{DD}		7	V
Voltage on any Signal Pin			-0.5 to V_{DD}+0.5	V
Storage Temperature	T_S		-55 to +150	^oC
Ambient Operation Temperature	T_A		0 to 70	^oC

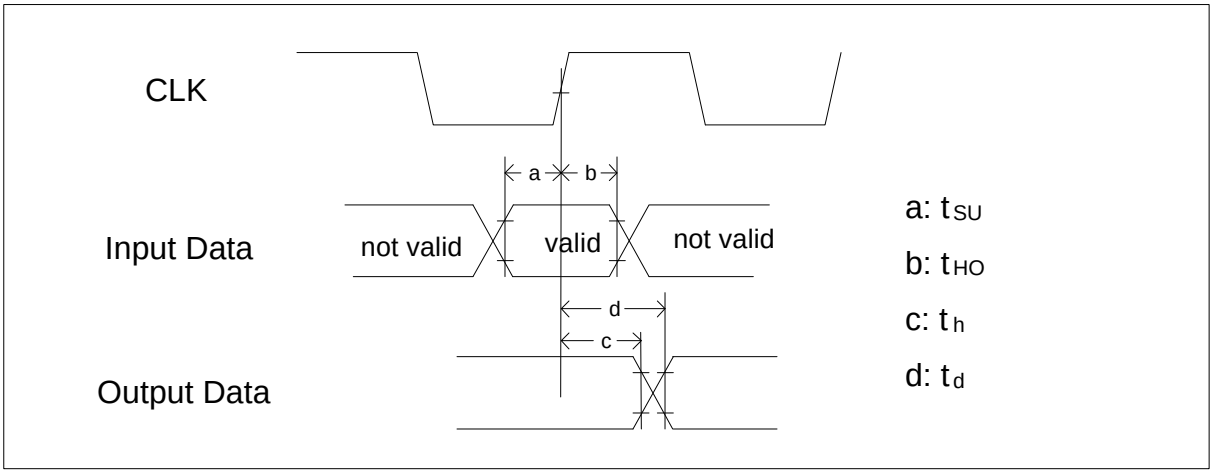
Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

ELECTRICAL CHARACTERISTICS

(V_{DD}= 3.3V, V_{SS}= 0V, Ta= 0 to 70 °C)

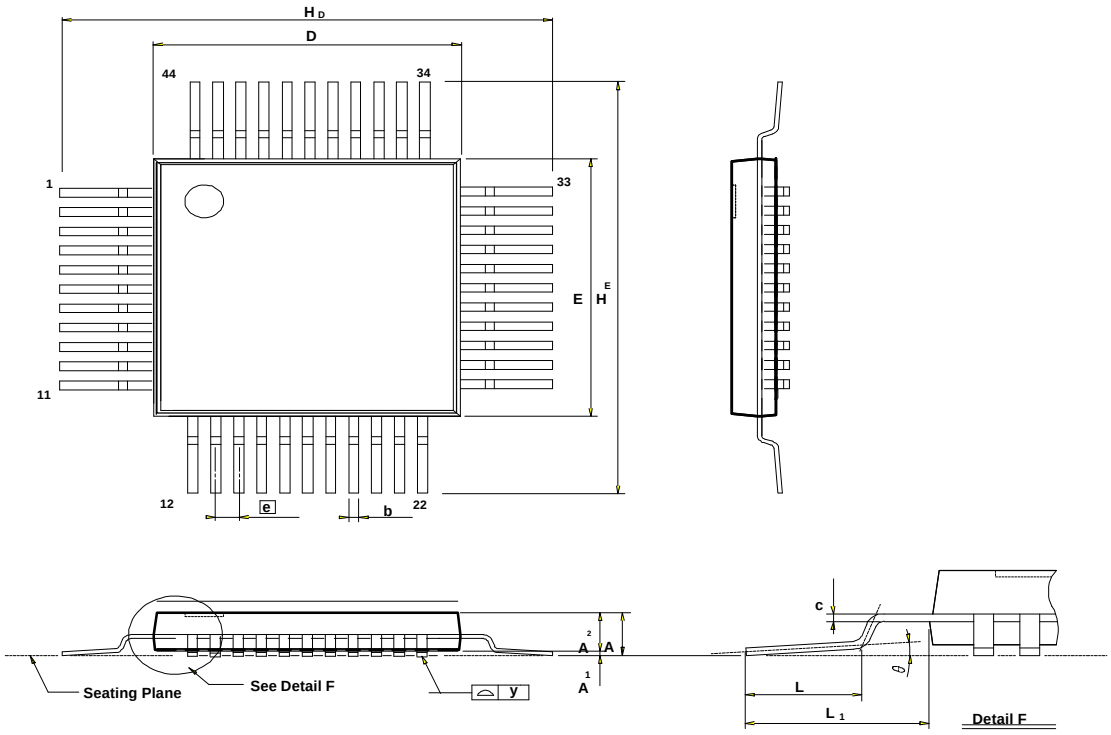
PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			Min.	**Typ.**	**Max.**	
Supply						
analog supply voltage	V_{DDA}		3.1	3.3	5.5	V
digital supply voltage	V_{DDD}		3.1	3.3	5.5	V
analog supply current	I_{DDA}		-	110	-	mA
digital supply current	I_{DDD}		-	22	-	mA
Inputs						
LOW level voltage (except XTALI)	V_{IL}		-0.5	-	0.8	V
HIGH level voltage (except XTALI)	V_{IH}		2.0	-	V_{DD}+0.5	V
Input leakage current	I_{LI}		-1	-	+1	uA
Input capacitance	C_i		-	7	10	pF
Outputs						
LOW level voltage	V_{OL}	I_{OL} = 3.2 mA	-	-	0.4	V
HIGH level voltage	V_{OH}	I_{OH} = -400 uA	V_{DDD}-0.4	-	-	V
SDA output						

LOW level output voltage (SDA)	V_{OL}	I_{OL} = 2mA	-	-	0.4	V
Clock timing (CLK)						
CLK frequency	F_{CLK}		24	27	30	MHz
duty cycle	T_{CLK_D}		-	50	-	%
Input Timing						
set-up time (except SDA and XTALO)	t_{SU}		6	-	-	nS
hold time (except SDA and XTALO)	t_{HO}		3	-	-	nS
Crystal Specification						
load capacitance	C_L		8	-	-	pF
series resistance	R_S		-	-	80	ohms
Digital Outputs Timing						
hold time	t_h		3	-	-	nS
delay time	t_d		-	-	25	nS
D/A converters						
output voltage	V_o	DAC code 1023	-	1.31	-	V
output capacitance	V_C		-	22	-	pF
bandwidth of DAC	B_{-3dB}		10	-	-	MHz
LF integral linearity error	ILE		-	-	+/-3	LSB
LF differential linearity error	DLE		-	-	+/-2	LSB



BONDING PAD DIAGRAM

44L QFP (10x10x2.0mm footprint 3.2mm)



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	-------	-------	-	-------	-------	-
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e		.0315			0.80	
H_D	0.510	0.520	0.530	12.95	13.20	13.45
H_E	0.510	0.520	0.530	12.95	13.20	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1		0.063			1.60	
y	──	──	0.004	──	──	0.10
θ	0 °	──	10 °	0 °	──	10 °

APPENDIX: APPLICATION NOTES

START CONDITION OF I²C BUS ACCESS FOR W9953F/W9954F

Because of the design of I²C reset circuit of W9953F/W9954F, an extra falling edge is needed to make a START condition. Please modify the START condition of I²C access by adding a pulse on SCL signal (see the figure below). This modification is compatible with normal START condition for other I²C chips.

REGISTERS PROGRAMMING

After W9953F/W9954F is reset, the registers are at their default values. To make the chip work, some registers must be programmed properly. The following items should be checked to see whether any modification is needed.

Format

TV standard and Pedestal (**D[7:5]** of **CONFG1**) determine the format of video displayed. Generally speaking, Pedestal is accompanied with NTSC-M or PAL-M mode and no pedestal for PAL-BDGHI or PAL-N_C mode. The default setting is NTSC-M with Pedestal enabled.

Sync

The sync mode (**D[2..0]** of **CONFG1**) and polarity of sync signals (**D[7:6**] of **CONFG2**) must be set properly. The default setting is Slave Mode 1 with both sync signals negative active.

If the frame and line synchronization has been achieved but the color of video pictures are wrong, you may try adjusting the Sync Phase (**D[5:4]** of **CONFG3**).

After the Format and Sync being properly set, normal video signals can be output.

There are many advanced functions (such as Non-interlaced mode, VBI coding, etc.) can be invoked by programming registers. Please refer to the data sheet.

Y-C DELAY ADJUSTMENT

W9953F/W9954F can insert a programmable delay on the luminance path to compensate any chroma/luma delay. This version (**ver[3:0]**="0000") of the W9953F/W9954F has an internal Y path delay which equals about -3 CLK (-105nS), so that if there is no extra delay introduced by off-chip filtering, the luminance path delay adjustment register (**D[2:0]** of **CONFG3**) should be set to +3CLK ("011") to obtain the minimum Y/C delay.

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Note: All data and specifications are subject to change without notice.