

Applications

- Small Cell BTS
- 3G/4G Wireless infrastructure
- Linearized Transmitter
- W-CDMA/ LTE/ CDMA
- Heterogeneous Networks

Product Features

- 2110-2170 MHz
- 2.5 W RMS Output Power
- Integrated Doherty Final Stage
- Three Stage Power Added Efficiency: 35 %
- 50 Ω Input / Output
- Power Gain: 34 dB
- Peak Power: 18 W
- Package Dimensions: 20 x 20 x 1.5 mm
- 100 % DC and RF tested

General Description

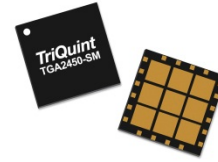
The TGA2450-SM is a fully integrated surface mount 3-stage Power Amplifier Module ideally suited for 3G and 4G small cell base station applications with 1 W RMS at the antenna. The module is 50 Ω input and output and requires minimal external components. The module is also compact and offers a much smaller footprint than traditional discrete component solutions.

The TGA2450-SM incorporates a Doherty final stage delivering high power added efficiency of 35 % for the entire module at 2.5 W average power.

The TGA2450-SM supports multi-mode and multi-carrier signals. The module includes InGaP/GaAs HBT device technology to provide a combination of high efficiency and DPD friendliness.

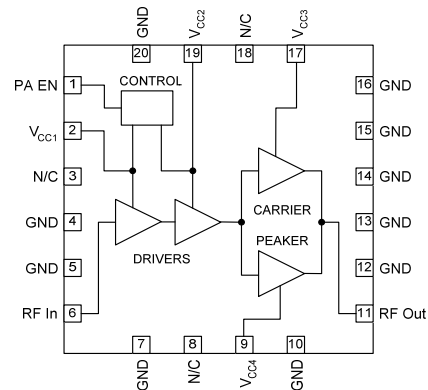
Lead-free and RoHS compliant.

Evaluation Board is available upon request.



20 Pin 20x20 mm Plastic Package

Functional Block Diagram



Pin Configuration

Pin No.	Label
1	PA EN
2	V _{CC1}
3, 8, 18	N/C
4, 5, 7, 10, 12-16, 20	GND
6	RF IN
9	V _{CC4}
11	RF OUT
17	V _{CC3}
19	V _{CC2}
Backside Paddle	RF/DC GND

Ordering Information

Part No.	Description
TGA2450-SM	Small Cell PAM
TGA2450-SM-PCB	2110-2170 MHz Eval Board

Absolute Maximum Ratings

Parameter	Rating
Collector Voltage (V_{CC1})	6 V
Collector Voltage (V_{CC2} , V_{CC3} , V_{CC4})	19 V
RF Input Power Over Drive above P_{IN} at 34 dBm P_{OUT} , 50 Ω , $T = 25^{\circ}\text{C}$	8 dB
VSWR at P_{OUT} with 1 dB PAR compression with WCDMA signal	5:1
Storage Temperature	-65°C to 150°C
Case Temperature (Backside Pads)	120°C

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Temperature	-40	+25	+90	$^{\circ}\text{C}$
V_{CC1}		5		V
V_{CC2} , V_{CC3} , V_{CC4}		18		V
PA Enable On	1.15	1.2-5.5	6	V
PA Enable Off		0	0.6	V
I_{CQ1} (at V_{CC1})		60		mA
I_{CQ2} (at V_{CC2})		25		mA
I_{CQ3} (at V_{CC3})		90		mA
T_j for $> 10^6$ hours MTTF			200	$^{\circ}\text{C}$

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications at $T_{CASE} = 25^{\circ}\text{C}$

Test conditions unless otherwise noted: $V_{CC1} = 5\text{ V}$, $V_{CC2} = 18\text{ V}$, $V_{CC3} = 18\text{ V}$, $V_{CC4} = 18\text{ V}$, $I_{CQ1} = 60\text{ mA}$, $I_{CQ2} = 25\text{ mA}$, $I_{CQ3} = 90\text{ mA}$, $P_{OUT} = 34\text{ dBm}$, System impedance = 50 Ω

Parameter	Conditions	Min	Typ	Max	Units
RF Frequency Range		2110		2170	MHz
I_{CQ1}	$V_{CC1} = 5\text{ V}$	35	60	80	mA
$I_{CQ2} + I_{CQ3}$	$V_{CC2} = V_{CC3} = 18\text{ V}$	90	115	140	mA
Power Gain	$P_{OUT} = 34\text{ dBm}$ average	32.2	34.4		
Gain flatness across any 40 MHz in-band	$P_{OUT} = 34\text{ dBm}$ average		1	2	dB
Average Output Power			+34		dBm
P3dB	Pulsed, 10 μsec width, 1 msec period	+41.9	+42.6		dBm
Power Added Efficiency	$P_{OUT} = 34\text{ dBm}$ average	33.2	35.4		%
ACLR DPD corrected	5-20 MHz SBW UMTS/LTE		-55		dBc
Input/Output Impedance			50		ohm
Input Return Loss	$P_{OUT} = 34\text{ dBm}$ average		13	11	dB
Group delay				5	nS
Group delay ripple				750	pS
Noise Figure				3	dB

Electrical Specifications at $T_{CASE} = -40^{\circ}C$ to $+90^{\circ}C$

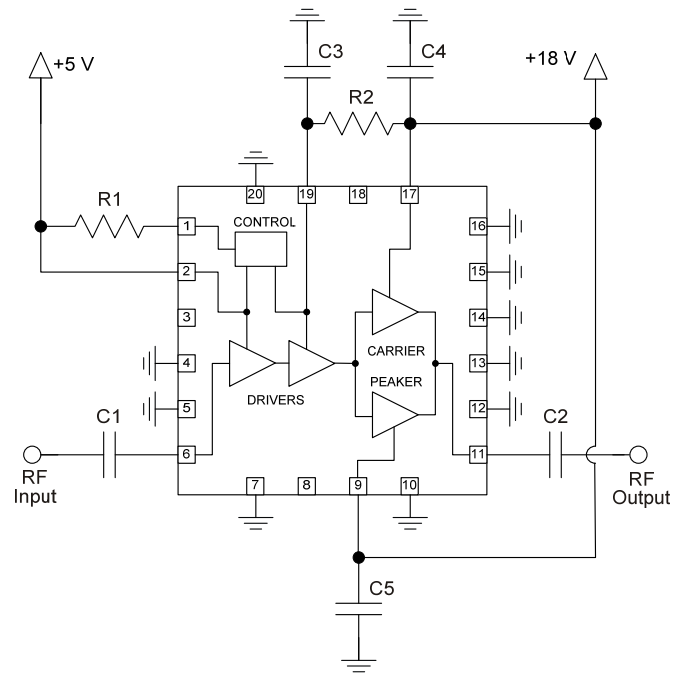
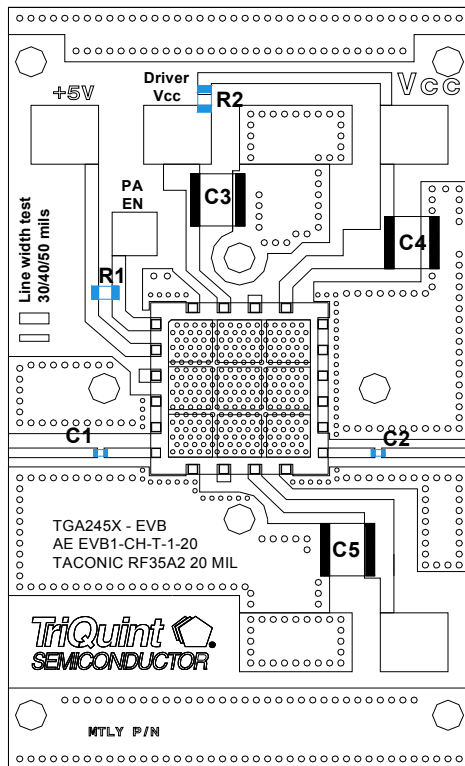
Test conditions unless otherwise noted: $V_{CC1} = 5 V$, $V_{CC2} = 18 V$, $V_{CC3} = 18 V$, $V_{CC4} = 18 V$, $I_{CQ1} = 60 mA$, $I_{CQ2} = 25 mA$, $I_{CQ3} = 90 mA$, $P_{OUT} = 34 dBm$, System impedance = 50Ω

Parameter	Conditions	Min	Typ	Max	Units
Power Gain	$P_{OUT} = 34 dBm$ average	29.9		38.6	dB
I_{CQ1}	$V_{CC1} = 5 V$	29	60	86	mA
$I_{CQ2}+I_{CQ3}$	$V_{CC2} = V_{CC3} = 18 V$	84	115	146	mA
I_{CC1}	$V_{CC1} = 5 V$, $P_{out} = 34 dBm$ average			95	mA
Gain flatness across any 40 MHz in-band	$P_{OUT} = 34 dBm$ average		1	2	dB
P3dB	Pulsed, 10 μ sec width, 1 msec period	41			dBm
Power Added Efficiency	$P_{OUT} = 34 dBm$ average	30			%
Input Return Loss	$P_{OUT} = 34 dBm$ average		13	11	dB
Second Harmonic	$P_{OUT} = 34 dBm$ at f_0 with WCDMA, 3.84 MHz IBW			-43	dBc
Third Harmonic	$P_{OUT} = 34 dBm$ at f_0 with WCDMA, 3.84 MHz IBW			-37	dBc
Group delay				5	nS
Group delay ripple				750	pS
$ S_{12} - S_{21} $		15			dB
Thermal Resistance, $\theta_{jc}^{(1)}$	(junction to case), $T_{CASE} = 90^{\circ}C$		14.8		$^{\circ}C/W$

Notes:

1. Measured carrier amplifier junction to package backside.

PC Board Layout and Evaluation Board Diagram



Bill of Material – TGA2450-SM-PCB Evaluation Board

Reference Des.	Value	Description	Manuf.	Part Number
Connector	n/a	N-type Connector	Huber+Suhner	23_N-50-0-16/133_NE
R2	0 Ω	Jumper		1206 0 ohm resistor
R1	10 k Ω	Resistor		1206 10K resistor
C1, C2	33 pF	Capacitor	ATC	0603 600S 33pF capacitor
C3, C4, C5 ⁽¹⁾	10 μ F	Capacitor	TDK	2220 X7R 10uF 50V
PCB	n/a	Taconic RF35 A2 20 mils		AE EVB1 CH-T-1-20

Notes:

1. C3, C4, C5 can be replaced by 10 μ F 50 V Electrolytic capacitor if it is needed.

Bias-up Procedure

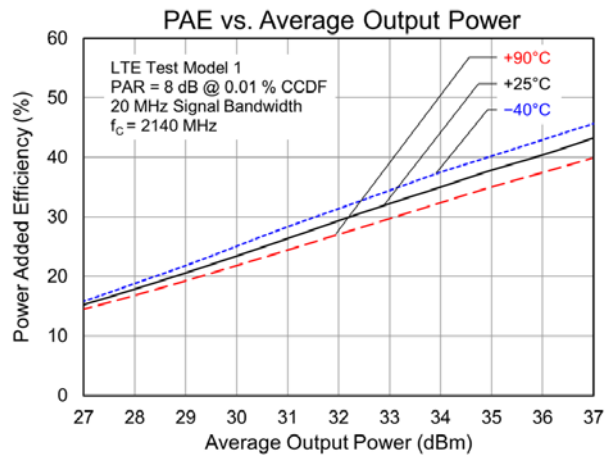
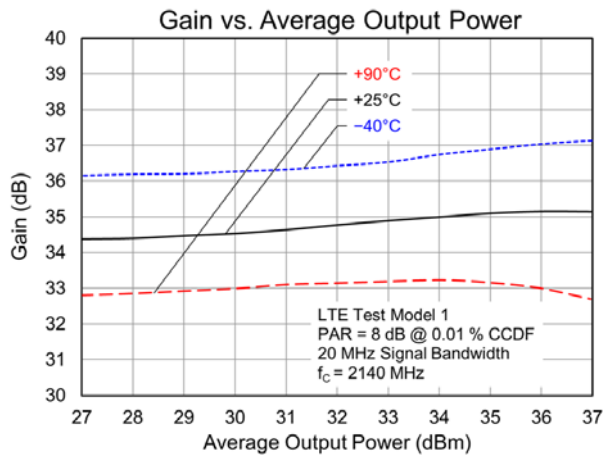
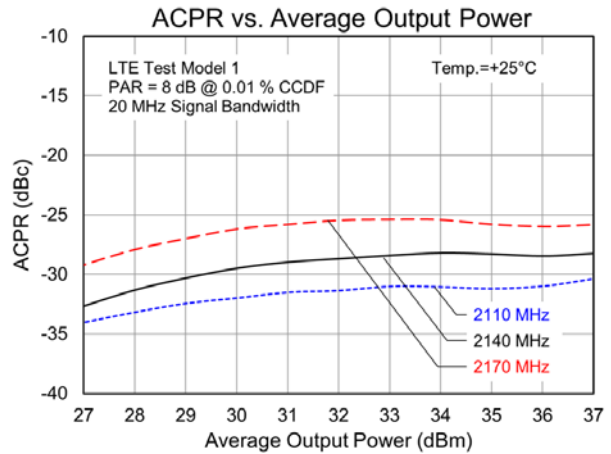
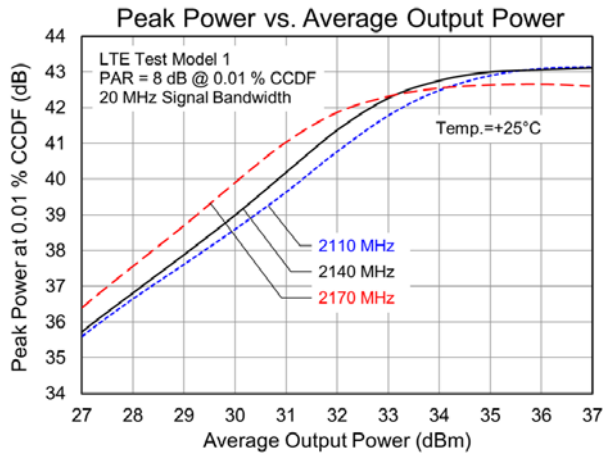
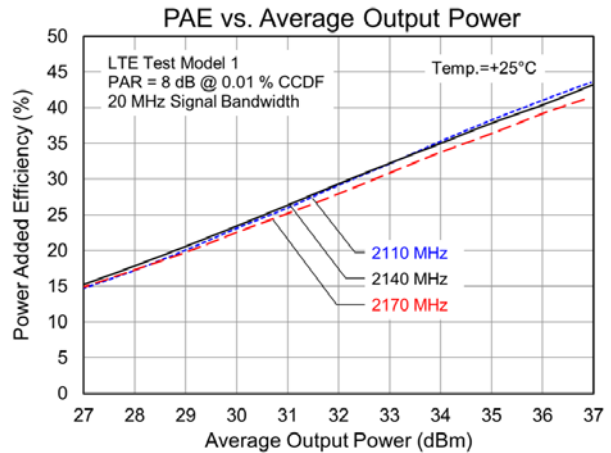
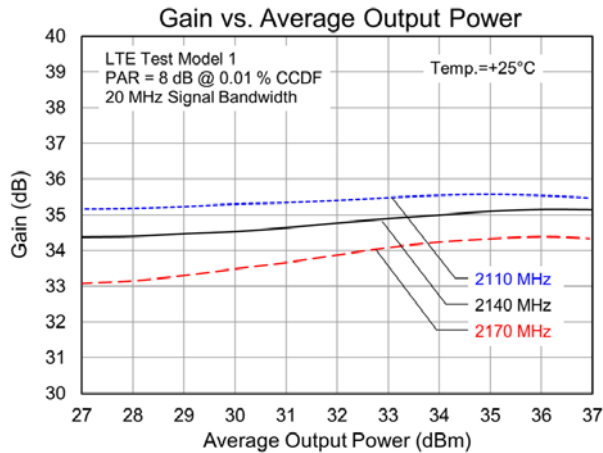
1. Attach input and output loads onto evaluation board.
2. Turn on 18 V power supply V_{CC2} , V_{CC3} , V_{CC4} .
3. Turn on 5 V power supply V_{CC1} .
4. Apply RF signal.
5. Turn on RF power.

Bias-down Procedure

1. Turn off RF power.
2. Turn off PA EN.
3. Turn off 5 V power supply V_{CC1} .
4. Turn off 18 V power supply V_{CC2} , V_{CC3} , V_{CC4} .

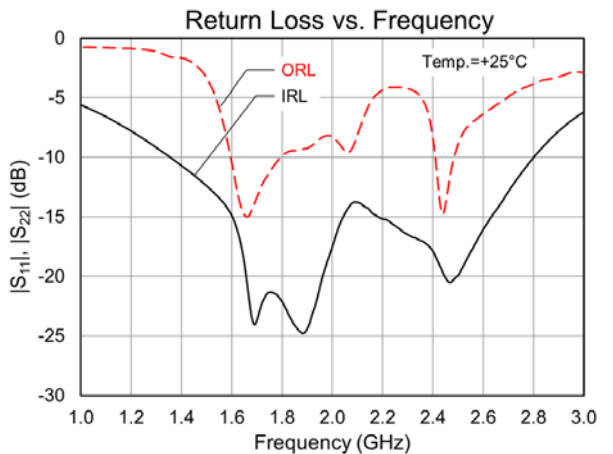
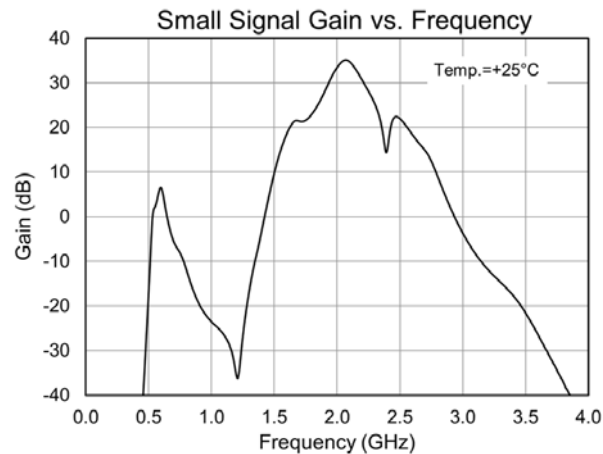
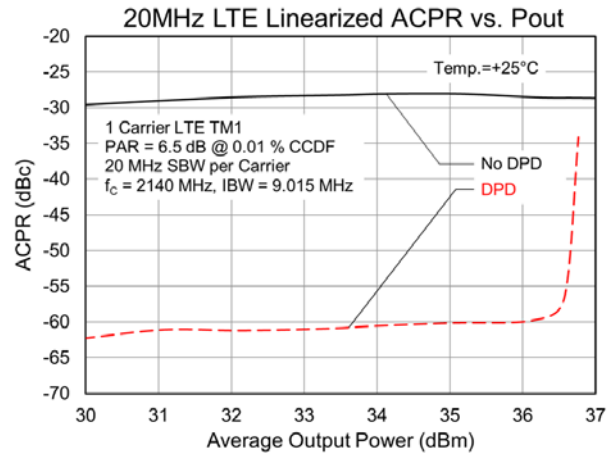
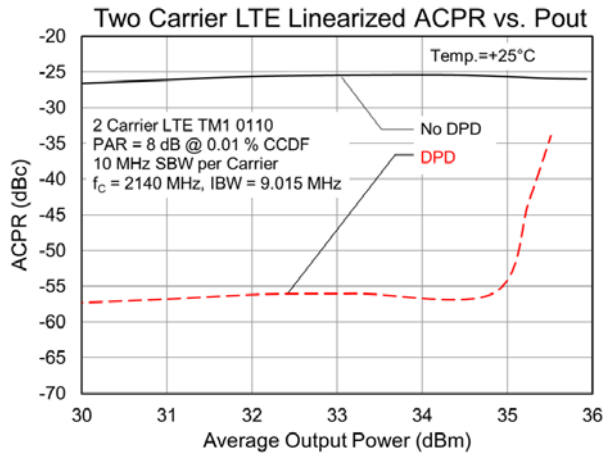
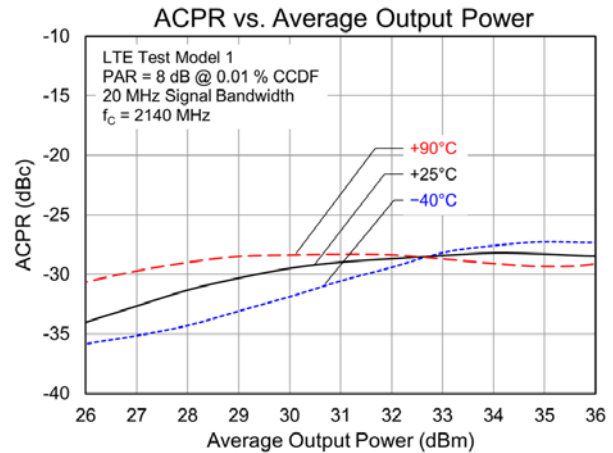
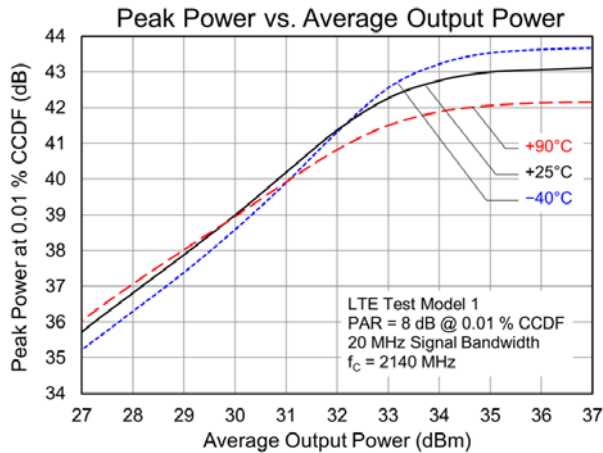
Performance Plots

Test conditions unless otherwise noted: $V_{CC1} = 5\text{ V}$, $V_{CC2} = 18\text{ V}$, $V_{CC3} = 18\text{ V}$, $V_{CC4} = 18\text{ V}$, $I_{CQ1} = 60\text{ mA}$, $I_{CQ2} = 25\text{ mA}$, $I_{CQ3} = 90\text{ mA}$



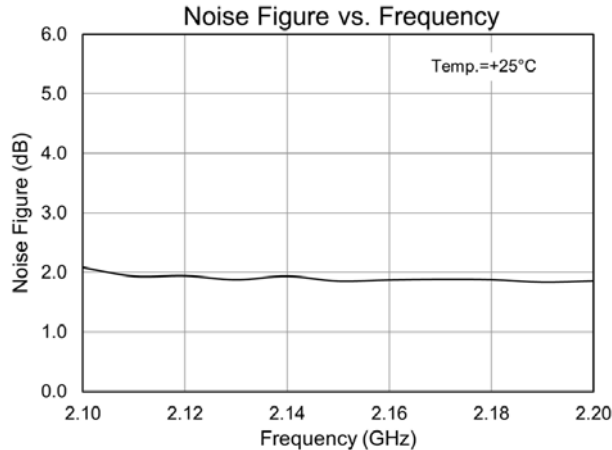
Performance Plots

Test conditions unless otherwise noted: $V_{CC1} = 5\text{ V}$, $V_{CC2} = 18\text{ V}$, $V_{CC3} = 18\text{ V}$, $V_{CC4} = 18\text{ V}$, $I_{CQ1} = 60\text{ mA}$, $I_{CQ2} = 25\text{ mA}$, $I_{CQ3} = 90\text{ mA}$

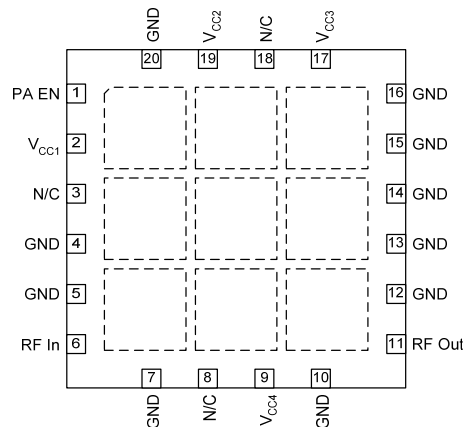


Performance Plots

Test conditions unless otherwise noted: $V_{CC1} = 5\text{ V}$, $V_{CC2} = 18\text{ V}$, $V_{CC3} = 18\text{ V}$, $V_{CC4} = 18\text{ V}$, $I_{CQ1} = 60\text{ mA}$, $I_{CQ2} = 25\text{ mA}$, $I_{CQ3} = 90\text{ mA}$



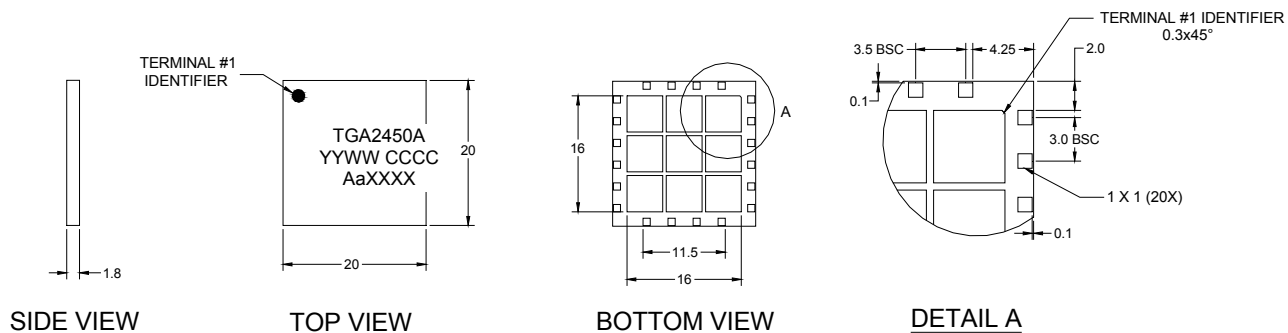
Pin Configuration and Description



Pin No.	Label	Description
1	PA EN	Control Voltage. See Recommended Operating Conditions on page 2.
2	V_{CC1}	Bias Voltage for pre-driver stage.
3, 8, 18	N/C	No electrical connection. Provide grounded land pads for PCB mounting integrity.
4, 5, 7, 10, 12-16, 20	GND	Internal grounding; must be grounded on PCB.
6	RF In	RF Output matched to 50 Ω .
9	V_{CC4}	Bias Voltage for output stage.
11	RF Out	RF Output matched to 50 Ω .
17	V_{CC3}	Bias Voltage for output stage.
19	V_{CC2}	Bias Voltage for driver stage.

Package Marking and Dimensions

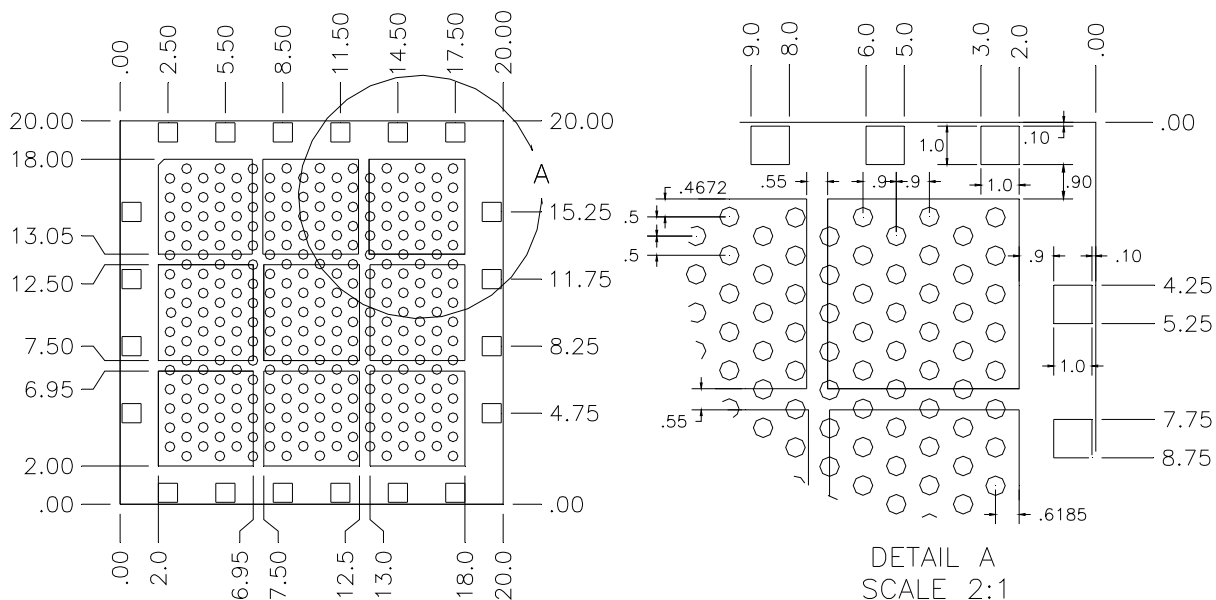
Marking: Part number – TGA2450A
 Year/week/country code – YYWW CCCC
 Lot code – AaXXXX



Notes:

1. All dimensions are in millimeters. Angles are in degrees.

PCB Mounting Pattern



Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.
3. Ground / thermal vias are critical for the proper performance of this device. Vias should use a 0.508 mm diameter drill and have a final plated thru diameter of 0.35 mm.

Product Compliance Information

ESD Sensitivity Ratings



Caution! ESD-Sensitive Device

ESD Rating: Class 1C
Value: Passes ≥ 1000 V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

MSL Rating

MSL Rating: Level 3
Test: 260°C convection reflow
Standard: JEDEC Standard IPC/JEDEC J-STD-020

Solderability

Compatible with both lead-free (260°C maximum reflow temperature) and tin/lead (245°C maximum reflow temperature) soldering processes.

Contact plating: NiPdAu

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

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