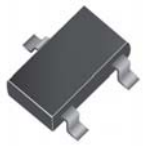
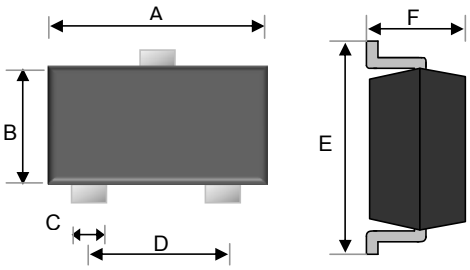
TAIWAN SEMICONDUCTOR

TESDF5V0AU
ESD Protection Array

Small Signal Diode



SOT-23



Dimensions	Unit (mm)		Unit (inch)	
	Min	Max	Min	Max
A	2.80	3.00	0.110	0.118
B	1.20	1.40	0.047	0.055
C	0.30	0.50	0.012	0.020
D	1.80	2.00	0.071	0.079
E	2.25	2.55	0.089	0.100
F	0.90	1.20	0.035	0.043

Features

- ✧Meet IEC61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
- ✧Meet IEC61000-4-4 (EFT) rating. 40A (5/50ήs)
- ✧Meet IEC61000-4-5 (Lightning) rating. 12A (8/20μs)
- ✧Protects two directional I/O lines
- ✧Working Voltage : 5V
- ✧Pb free version, RoHS compliant, and Halogen free

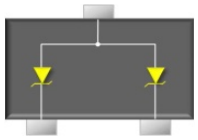
Mechanical Data

- ✧Case :SOT-23 standard package, molded plastic
- ✧Terminal: Matte tin plated, lead free., solderable per MIL-STD-202, Method 202 guaranteed
- ✧High temperature soldering guaranteed: 260°C/10s
- ✧Weight : 0.008gram (approximately)
- ✧Marking Code : M05

Applications

- ✧Cell Phone Handsets and Accessories
- ✧Microprocessor based equipment
- ✧Industrial Controls
- ✧Notebooks, Desktops, and Servers
- ✧Set-Top Box

Pin Configutation



rdering Information

Part No.	Package	Packing	Packing Code	Marking
TESDF5V0AU	SOT-23	3K / 7" Reel	RFG	M05

Maximum Ratings and Electrical Characteristics

Rating at 25°C ambient temperature unless otherwise specified.

Maximum Ratings

Type Number	Symbol	Value	Units
Peak Pulse Power (tp=8/20μs waveform)	P_{PP}	300	W
Peak Pulse Current (tp = 8/20μs)	I_{PP}	5	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	±15 ± 8	KV
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to + 150	°C

Electrical Characteristics

Type Number		Symbol	Min	Max	Units
Reverse Stand-Off Voltage		V_{RWM}	-	5	V
Reverse Breakdown Volta	I_R= 1mA	$V_{(BR)}$	6	-	V
Reverse Leakage Current	V_R= 5V	I_R	-	10	uA
Clamping Voltage	I_{PP}= 1A	Vc	-	9.8	V
	I_{PP}= 5A		-	15	
Junction Capacitance	V_R=0V, f=1.0MHz	C_J	350(Typ.)		pF

Small Signal Diode

Rating and Characteristic Curves

FIG 1 Non-Repetitive Peak Pulse Power vs. Pulse Time

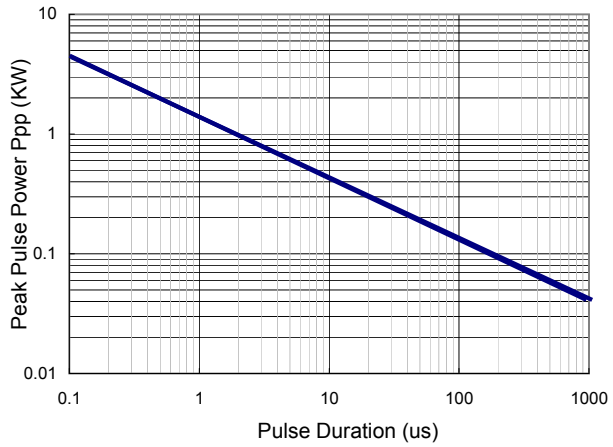


FIG 2 Pulse Waveform

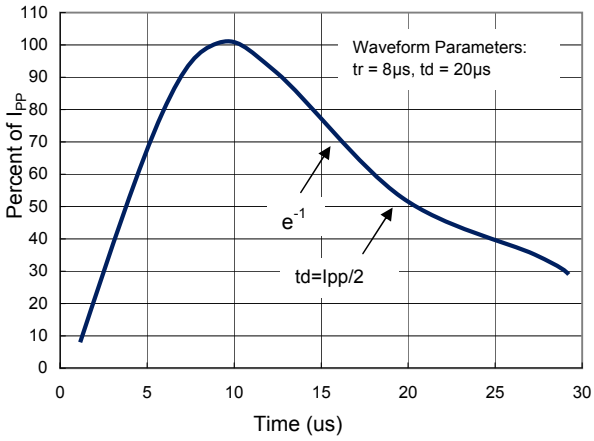


FIG 3 Admissible Power Dissipation Curve

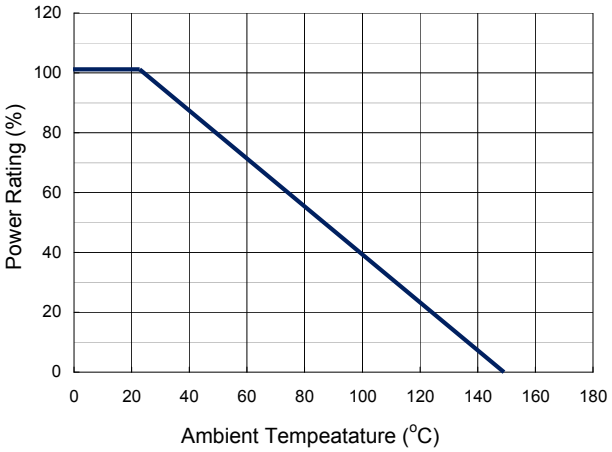


FIG 4 Typical Junction Capacitance

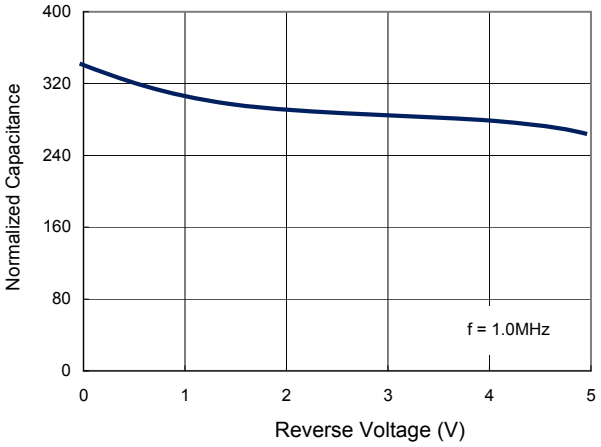
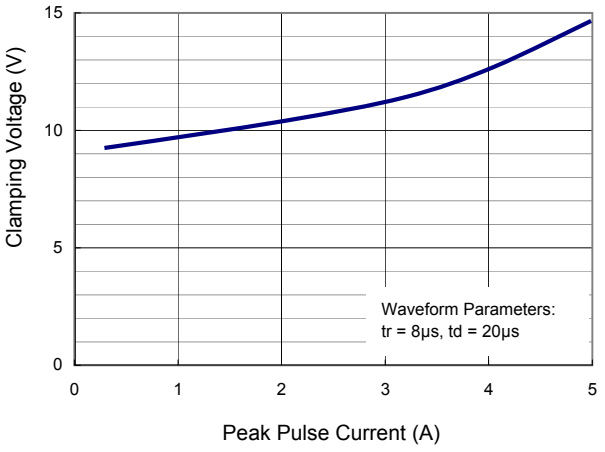


FIG 5 Clamping Voltage vs. Peak Pulse Current



TAIWAN SEMICONDUCTOR

TESDF5V0AU
ESD Protection Array

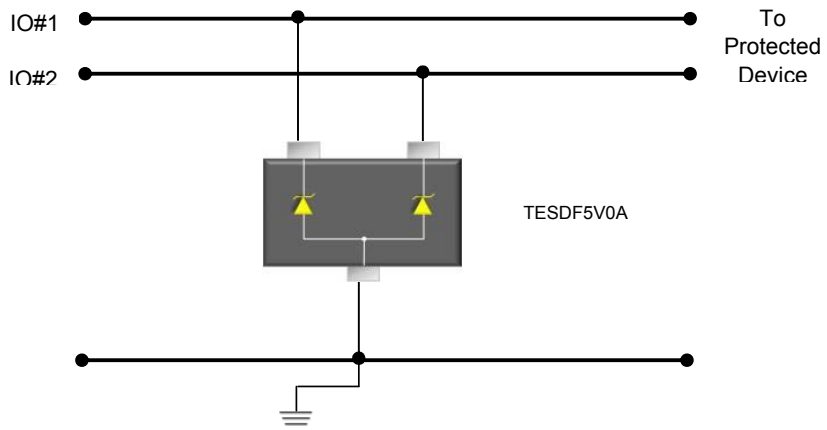
Small Signal Diode

Applications Information

✧Designed for the Uni-directional protection of 2 lines from the damage caused by Electro Static Discharge (ESD) and surge pulses
✧Be used on lines where the signal polarities are above and below ground
✧Provides a surge capability of 300 Watts peak Ppp per line for an 8/20 ms waveform.

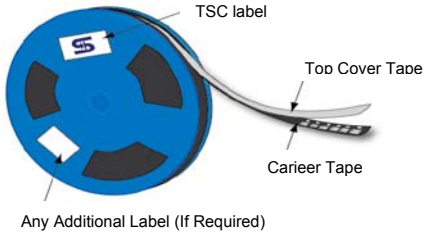
Circuit Board Layout Recommendations

✧Place the ESD protection array as close to the input terminal or connector as possible
✧Keep parallel signal paths to a minimum
✧Minimize all printed-circuit board conductive loops including power and group loops
✧Avoid using shared transient return paths to a common ground point
✧Ground planes should be used. For multilayer printed-circuit boards, use ground vias
✧Below picture is the typical application for bi-directional protection of two lines

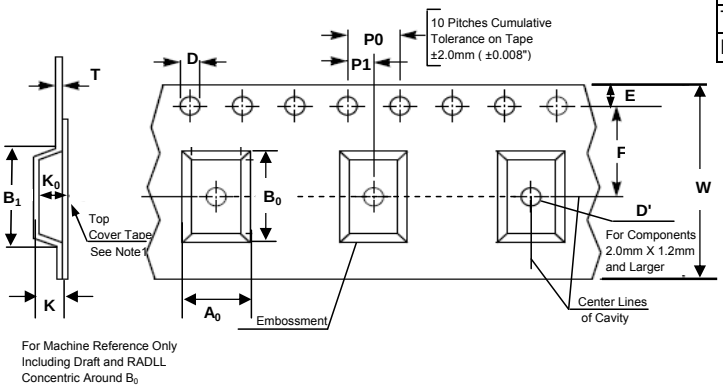


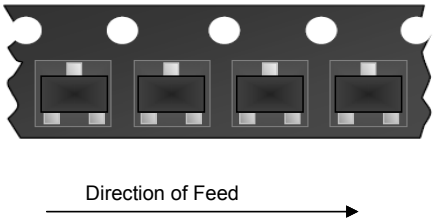
Small Signal Diode

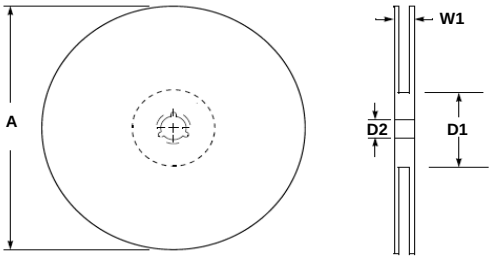
Tape & Reel specification



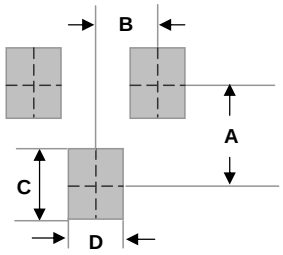
Item	Symbol	Dimension (mm)
Carrier depth	K	1.22 Max.
Sprocket hole	D	1.50 +0.10
Reel outside diameter	A	180 ± 1
Reel inner diameter	D1	50 Min.
Feed hole width	D2	13.0 ± 0.5
Sprocke hole position	E	1.75 ±0.10
Sprocke hole pitch	P0	4.00 ±0.10
Embossment center	P1	2.00 ±0.10
Overall tape thickness	T	0.6 Max.
Tape width	W	8.30 Max.
Reel width	W1	14.4 Max.







Suggested PAD Layout



Dimensions	Unit (inch)	Unit (mm)
A	0.079	2.00
B	0.037	0.95
C	0.035	0.90
D	0.031	0.80

Note 1: A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min. to 0.5 mm max. The component cannot rote more than 10 ^{o} within the determined cavity.
Note 2: If B_1 exceeds 4.2 mm(0.165") for 8 mm embossed tape, the tape may not feed through all tape feeders.
Note 3: The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary despending on application.