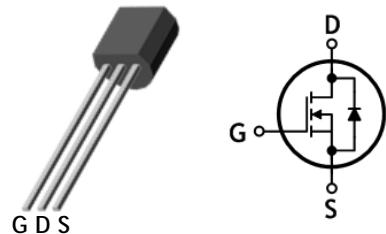


## SWITCHING REGULATOR APPLICATION

### Features

- High voltage:  $BV_{DSS}=700V$  (Min.)
- Low gate charge:  $Q_g=4nC$  (Typ.)
- Low drain-source On resistance:  $R_{DS(on)}=12.5\Omega$  (Max.)
- Low  $C_{rss}$ :  $C_{rss}=2.5pF$  (Typ.)
- RoHS compliant device

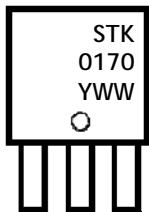


### Ordering Information

Part Number	Marking	Package
STK0170	STK0170	TO-92

TO-92

### Marking Information



Column 1, 2: Device Code  
Column 3: Production Information  
e.g.) YWW  
-. YWW: Date Code (year, week)

### Absolute maximum ratings ( $T_a=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	700	V
Gate-source voltage	$V_{GSS}$	$\pm 30$	V
Drain current (DC) *	$I_D$	0.3	A
Drain current (Pulsed) *	$I_{DP}$	1.2	A
Avalanche current	$I_{AS}$	0.3	A
Single pulsed avalanche energy <sup>(Note 2)</sup>	$E_{AS}$	25	mJ
Repetitive avalanche current <sup>(Note 1)</sup>	$I_{AR}$	0.3	A
Repetitive avalanche energy <sup>(Note 1)</sup>	$E_{AR}$	0.5	mJ
Power dissipation	$P_D$	625	mW
Junction temperature	$T_J$	150	$^\circ C$
Storage temperature range	$T_{stg}$	-55~150	$^\circ C$

\* Limited only maximum junction temperature

**Thermal Characteristics**

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 200	°C/W

**Electrical Characteristics ( $T_a=25^\circ C$  unless otherwise noted)**

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	$BV_{DSS}$	$I_D=250\mu A, V_{GS}=0$	700	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu A, V_{DS}=V_{GS}$	2.5	2	4.5	V
Drain-source cut-off current	$I_{DSS}$	$V_{DS}=700V, V_{GS}=0V$	-	-	1	$\mu A$
Gate leakage current	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 30V$	-	-	$\pm 100$	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=150mA$	-	12.5	15	$\Omega$
Input capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V, f=1MHz$		163	211	pF
Output capacitance	$C_{oss}$			19	25	
Reverse transfer capacitance	$C_{rss}$			2.5	3.5	
Turn-on delay time <sup>(Note 3,4)</sup>	$t_{d(on)}$	$V_{DD}=300V, I_D=0.8A$ $R_G=25\Omega$		12	30	ns
Rise time <sup>(Note 3,4)</sup>	$t_r$			50	150	
Turn-off delay time <sup>(Note 3,4)</sup>	$t_{d(off)}$			20	50	
Fall time <sup>(Note 3,4)</sup>	$t_f$			30	80	
Total gate charge <sup>(Note 3,4)</sup>	$Q_g$	$V_{DS}=560V, V_{GS}=10V$ $I_D=0.8A$		4	6	nC
Gate-source charge <sup>(Note 3,4)</sup>	$Q_{gs}$			1.2	3	
Gate-drain charge <sup>(Note 3,4)</sup>	$Q_{gd}$			1.5	4.5	

**Source-Drain Diode Ratings and Characteristics ( $T_a=25^\circ C$  unless otherwise noted)**

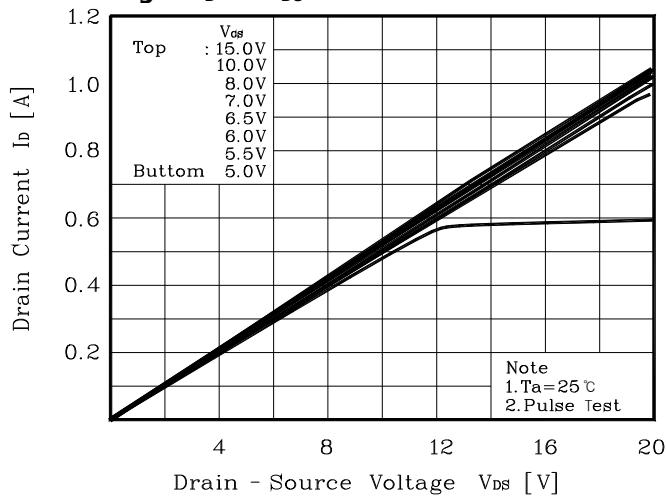
Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	$I_s$	Integral reverse diode in the MOSFET	-	-	0.3	A
Source current (Pulsed)	$I_{SM}$		-	-	1.2	A
Forward voltage	$V_{SD}$	$V_{GS}=0V, I_s=0.3A$	-	-	1.4	V
Reverse recovery time <sup>(Note 3,4)</sup>	$t_{rr}$	$I_s=0.8A, V_{GS}=0V$ $dI_F/dt=100A/us$	-	200	-	ns
Reverse recovery charge <sup>(Note 3,4)</sup>	$Q_{rr}$		-	0.31	-	$\mu C$

Note:

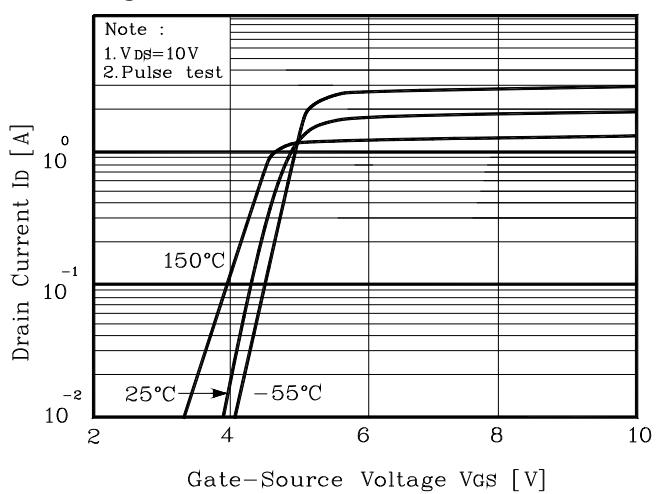
1. Repeated rating: Pulse width limited by safe operating area
2. L=94.7mH,  $I_{AS}=0.7A$ ,  $V_{DD}=50V$ ,  $R_G=25\Omega$ , Starting  $T_J=25^\circ C$
3. Pulse test: Pulse width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

## Electrical Characteristic Curves

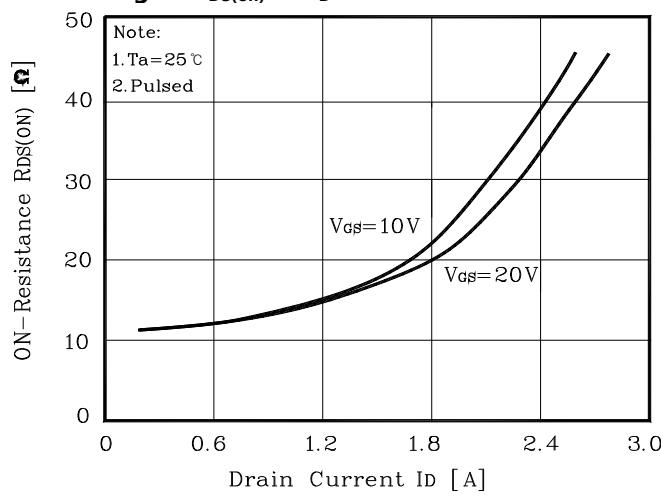
**Fig. 1  $I_D$  -  $V_{DS}$**



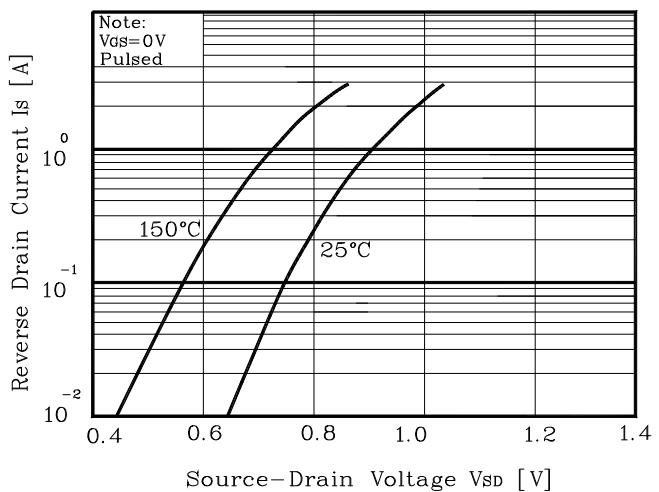
**Fig. 2  $I_D$  -  $V_{GS}$**



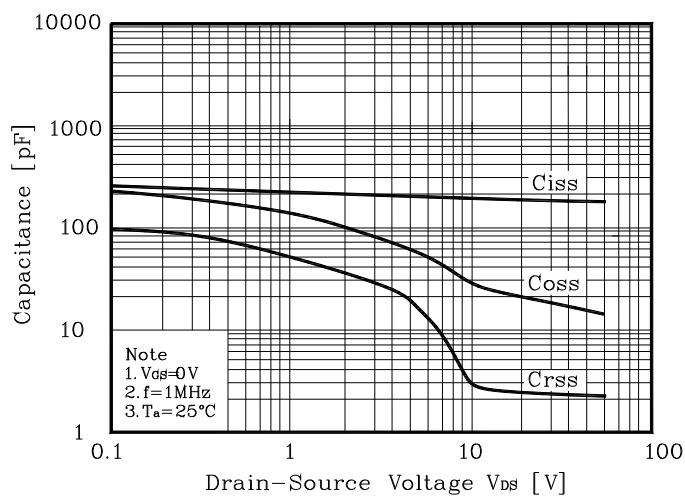
**Fig. 3  $R_{DS(on)}$  -  $I_D$**



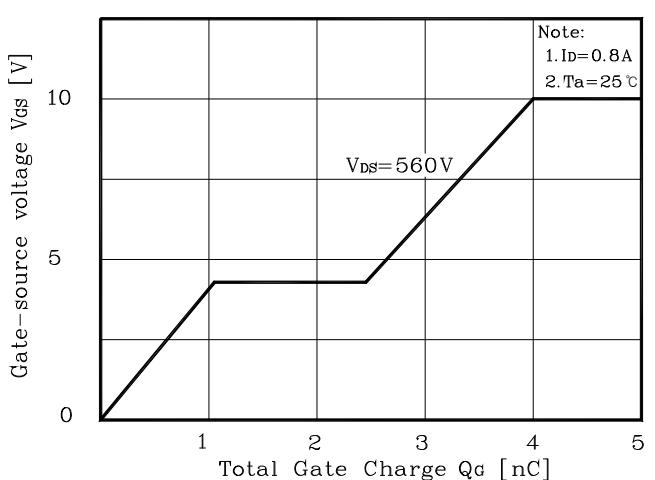
**Fig. 4  $I_S$  -  $V_{SD}$**



**Fig. 5 Capacitance -  $V_{DS}$**

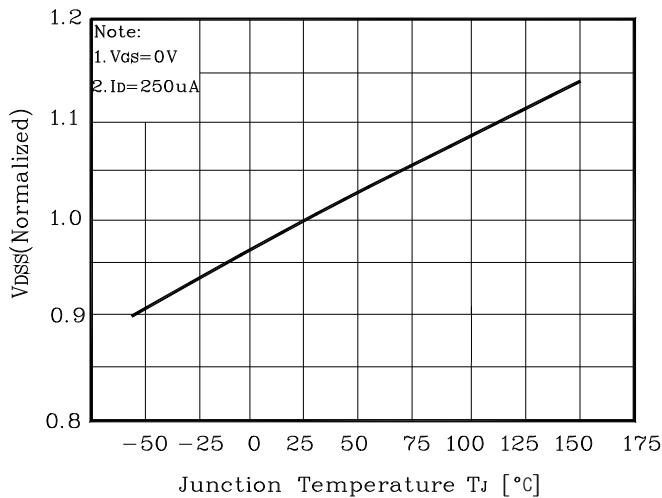


**Fig. 6  $V_{GS}$  -  $Q_G$**

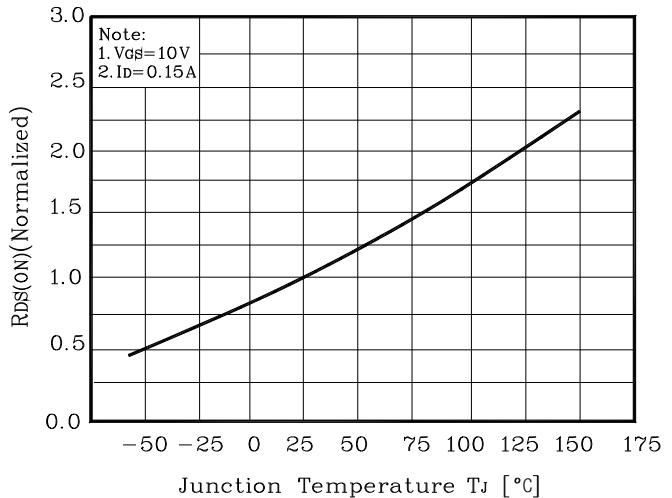


## Electrical Characteristic Curves (Continue)

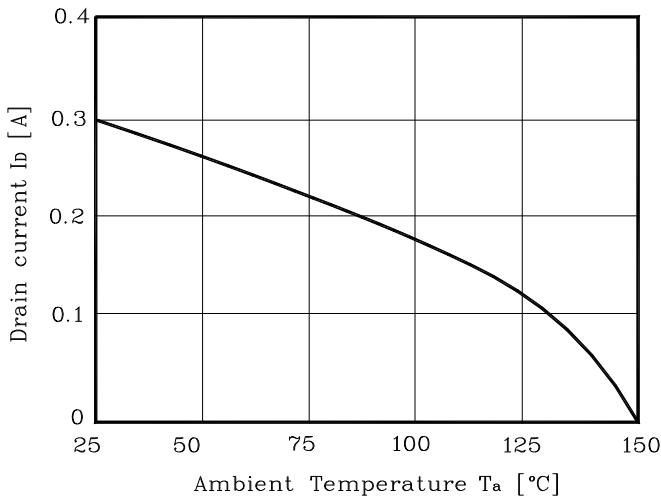
**Fig. 7  $V_{DSS}$  -  $T_J$**



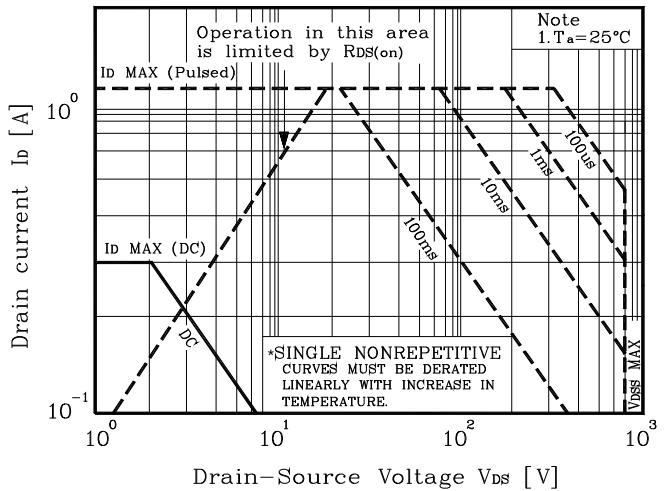
**Fig. 8  $R_{DS(on)}$  -  $T_J$**



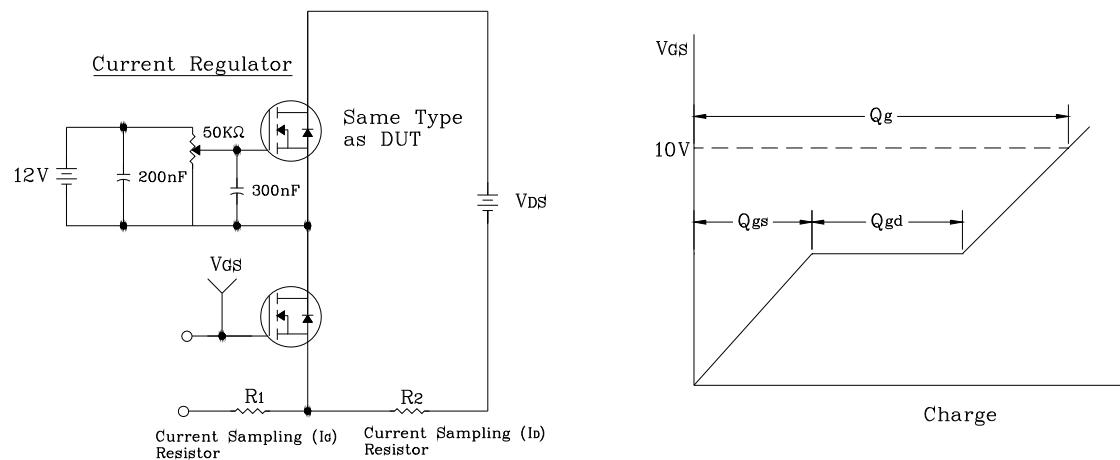
**Fig. 9  $I_D$  -  $T_a$**



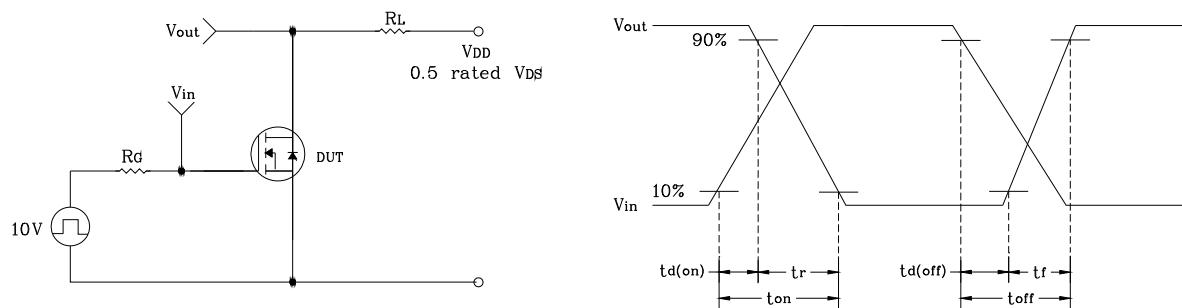
**Fig. 10 Safe Operating Area**



**Fig. 11 Gate Charge Test Circuit & Waveform**



**Fig. 12 Resistive Switching Test Circuit & Waveform**



**Fig. 13  $E_{AS}$  Test Circuit & Waveform**

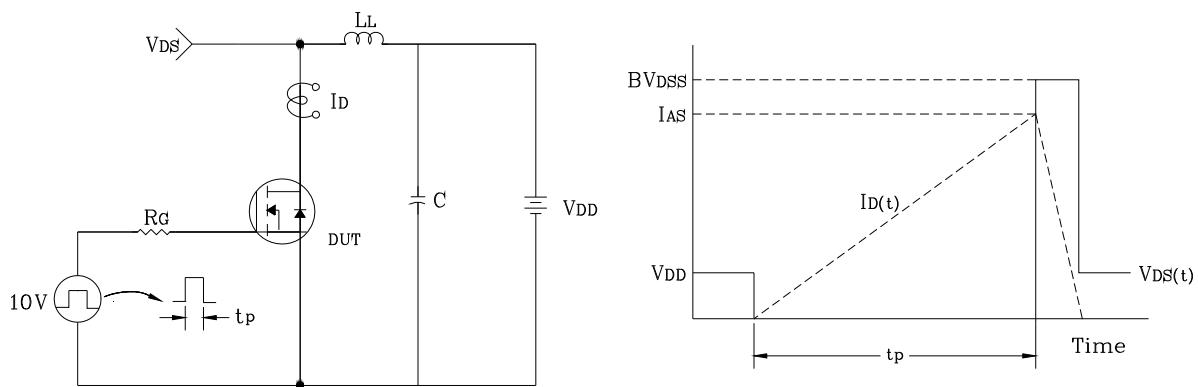
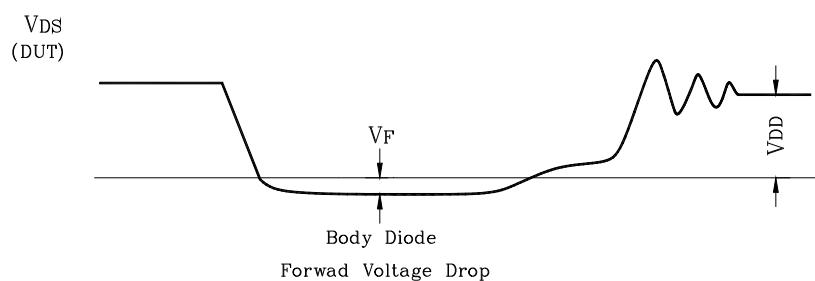
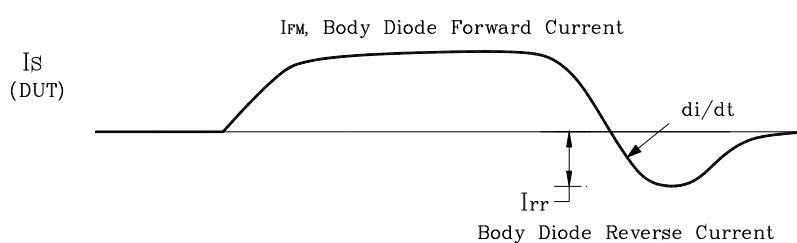
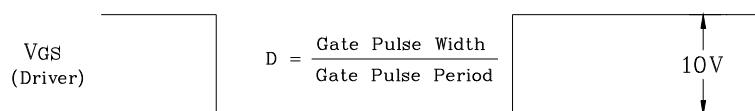
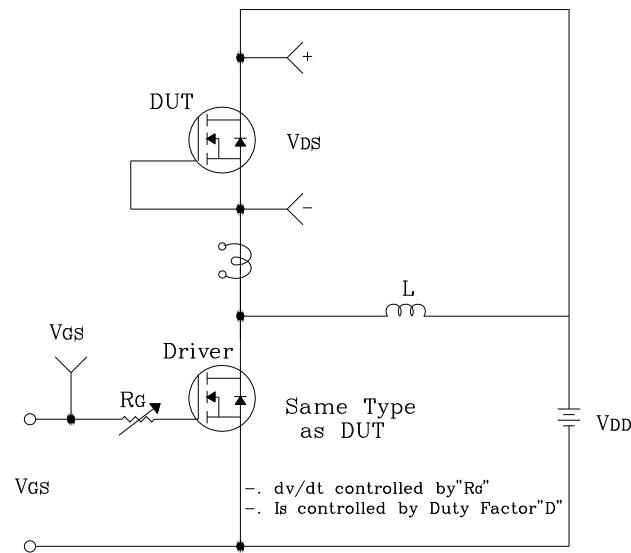
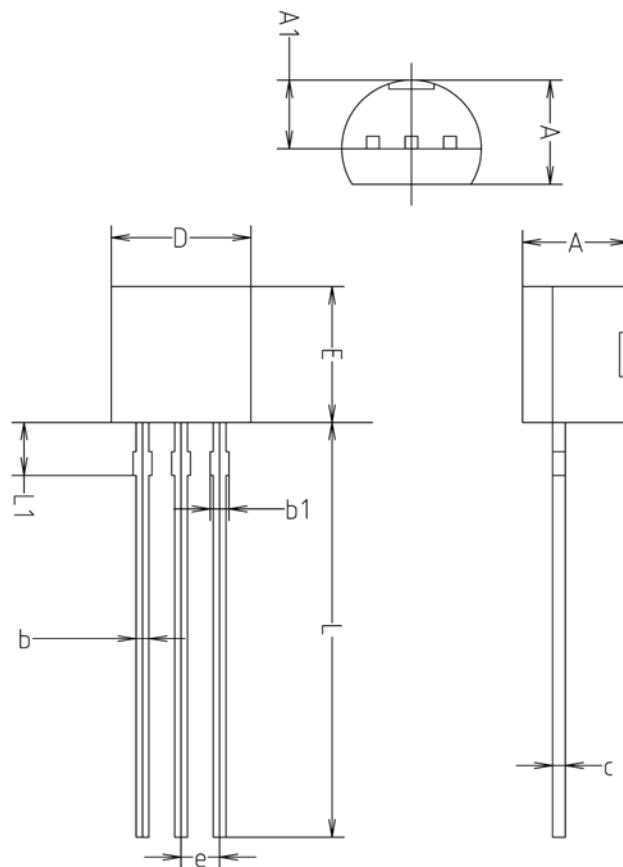


Fig. 14 Diode Reverse Recovery Time Test Circuit &amp; Waveform



**Package Outline Dimensions**

SYMBOL	MILLIMETERS(mm)		
	MINIMUM	NOMINAL	MAXIMUM
A	3.40	3.50	3.66
A1	2.46	2.51	2.59
b	0.39	0.44	0.53
b1	0.39	—	0.63
c	0.35	0.42	0.47
D	4.48	4.60	4.70
E	4.48	4.60	4.70
e	1.17	1.27	1.37
L	13.70	14.00	14.77
L1	1.55	1.70	2.15

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