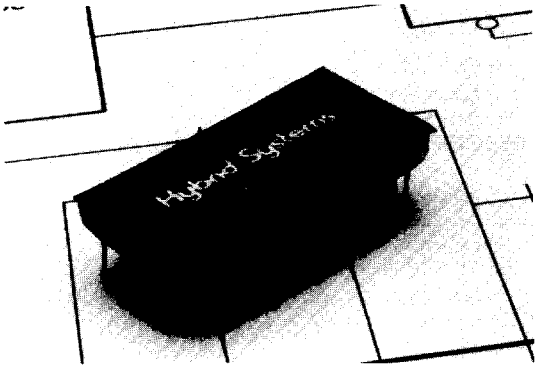
8-BIT 25 MSPS A/D CONVERTER

FEATURES

- Complete analog front-end and 25MHz ADC in a single package
- Low power consumption, 1W
- DC stabilized input amplifier
- Pin selectable RS170/RS343 gains

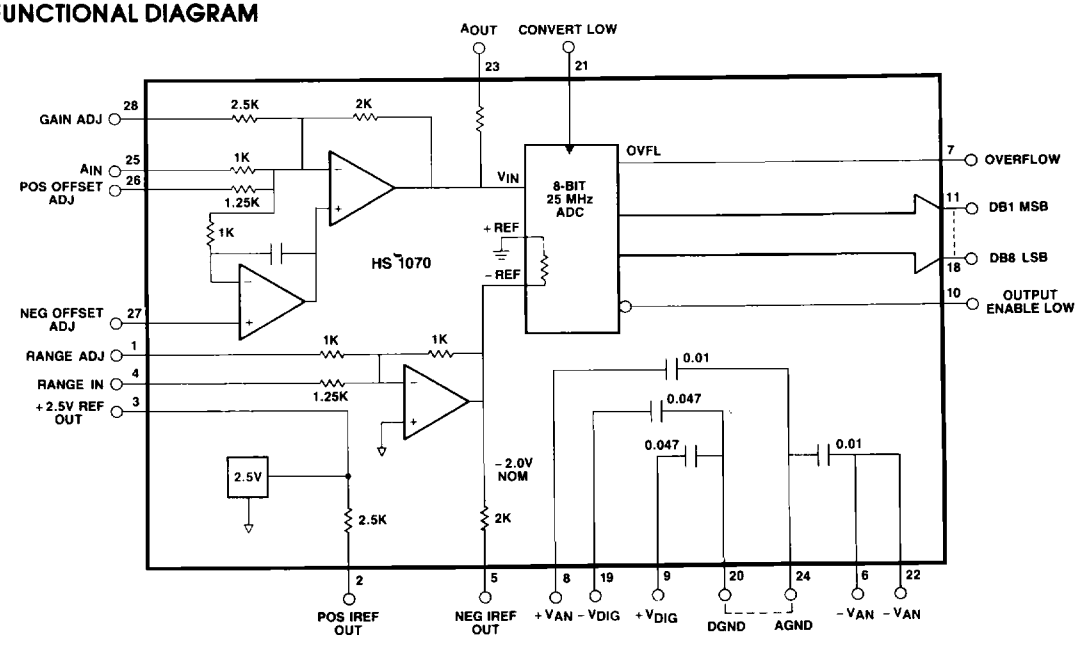


DESCRIPTION

The SP1070 is a complete flash analog to digital converter that includes all the circuitry necessary to convert video frequency analog signals into 8-bit digital data at rates up to 25 mega samples per second. The SP1070 is completely self contained providing a low power, 8-bit, 25MHz, flash A/D; a DC-stabilized wideband input amplifier; overload protection/recovery circuitry and 2.5 volt bootstrapped reference in a single 28-pin package.

The combination of all this circuitry into a single hermetic 28-pin DIP offers significant savings in board space; it also saves on component, assembly and design costs, while offereing tremendous flexibility in application circuits. Operation over the full military temperature range (−55°C to +125°C) and full compliance with MIL-STD-883C is available.

FUNCTIONAL DIAGRAM



SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNITS
Supply Voltage	V_{CC}	7.0	V
	$+V_A$	17.5	V
	V_{EE}	−7.0	V
	$-V_A$	−17.5	V
Digital Input Voltage	$V_{IN(D)}$	5.5	V
Analog Input Voltage	$V_{IN(A)}$	±5.5	V
Reference Voltage Span	$(A_{GND} - V_{pin\ 5})$	2.2	V
Applied Output Voltage	—	5.5	V
Junction Temperature	T_j	150	°C
Storage Temperature	T_{stg}	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEMPERATURE RANGE						UNITS
		0°C to +70°C			−55°C to +125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Digital Supply Voltage (Positive)	V_{CC}	4.75	5.0	5.25	4.5	5.0	5.5	V
Analog Supply Voltage (Positive)	$+V_A$	4.75	5.0	15.0	4.75	5.0	15.0	V
Digital Supply Voltage (Negative)	V_{EE}	−3.0	−5.0	−6.0	−3.0	−5.0	−6.0	V
Analog Supply Voltage (Negative)	$-V_A$	−4.75	−5.0	−15.0	−4.75	−5.0	−15.0	V
Analog Ground	(AGND-DGND)	−0.1	0	+0.1	−0.1	0	+0.1	V
Analog Input, Range ADJ and OFFSET ADJ Open	$V_{IN(A)}$	0.0		+1.0	0.0		+1.0	V
Digital Input Voltage, HIGH	$V_{IN(D)}$	2.0			2.0			V
Digital Input Voltage, LOW				0.8			0.8	V
Applied Output Voltage	V_o	0.0		V_{CC}	0.0		V_{CC}	V
CONV Pulse Width, LOW	t_{PWL}	15			15			nS
CONV Pulse Width, HIGH	t_{PWH}	5			5			nS
Clock Frequency, Max	f_{CLK}	25			25			MHz
Operating Ambient Temperature	T_A	0		70				°C
Operating Case Temperature	T_C				−55		+125	°C

PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS (F_{Sample} = 20 MHz)	TEMPERATURE RANGE						UNITS
			0°C to +70°C			−55°C to +125°C			
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution	N				8.0			8.0	Bits
Integral Linearity Error	E_{LI}	DC. Best Straight Line		±0.5	±1.0		±0.5	±1.0	LSB
Differential Linearity Error	E_{DI}	DC		±0.4	±0.85		±0.4	±0.75	LSB
RMS Signal/RMS Noise + Distortion	SNR	1.123 MHz Input	45	47		44	47		dB
		2.234 MHz Input	44	45		43	45		dB
		4.456 MHz Input	38	40		36	40		dB
Differential Phase	DP	F_S = 4 x NTSC Carrier		1			1		Degree
Differential Gain	DC	F_S = 4 x NTSC Carrier		1			1		%
Aperture Error	E_{AP}	Aperture Jitter		±300			±300		pS
Full Power Bandwidth	BW	No Missing Code	4	6		4	6		MHz
Input Amplifier Full Power Bandwidth	ABW	Freq −3 dB		20			20		MHz
Settling Time (to 0.1%)	t_S	Full Scale Transition		60	100		60	150	nS
Amplifier Overshoot	O_S			0			0		%
Overload Recovery	t_{REC}	±500 mV Overdrive		10			10		nS
Input Amplifier Noise		10 MHz Bandwidth[2]		200			200		μVRMS
Range AMP Bandwidth			5	8		5	8		MHz
Range AMP Settling		One Volt Step at R_{BOT}		0.5	1.0		0.5	1.0	μSec

SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE 0°C to +70°C MIN	TYP	MAX	−55°C to +125°C MIN	TYP	MAX	UNITS
Maximum Conversion Rate	F_S	V_{CC}, V_{EE} = MIN	25	30		20	25	30	MHz
Sampling Time Offset	t_{STO}	V_{CC}, V_{EE} = MIN	0	10		0	10		nS
Digital Output Delay	t_D	V_{CC} = MIN	15	19		15	19		nS
Digital Output Enable	t_{PZL}	V_{CC} = MIN		20			20		nS
Digital Output Disable	t_{PHZ}	V_{CC} = MIN		15			15		nS
Overflow	t_{OVF}	V_{CC} = MIN		20			20		nS
CONV Pulse Width, LOW	t_{PWL}	V_{CC} = MIN	15			15			nS
CONV Pulse Width, HIGH	t_{PWH}	V_{CC} = MIN	5			5			nS

INPUTS

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE 0°C to +70°C MIN	TYP	MAX	−55°C to +125°C MIN	TYP	MAX	UNITS
Input Current, Logic LOW	I_{IL}								
		OE @0.4V		−0.1	−0.4		−0.1	−0.8	mA
		CONV @0.4V		−0.1	−0.4		−0.1	−0.8	mA
Input Current, Logic HIGH	I_{IH}	OE @2.7V			20			40	μA
		CONV		0	100		0	100	μA
Input Voltage, Logic LOW	V_{IL}				0.8			0.8	V
Input Voltage, Logic HIGH	V_{IH}		2.0			2.0			V
Analog Input Resistance	R_{IN}		0.99K	1K	1.01K	0.99K	1K	1.01K	
Analog Input Capacitance	C_{IN}			3			3		pF
Input Offset Current	I_B	$I_B = V_{OS}$/1K Ohm		0.1			0.1		mA
Gain Error	E_G			±0.1			±0.1		%
Bipolar Offset Error				±0.5			±0.1		LSB
Unipolar Offset Error				±0.5			±0.1		LSB
Bipolar Offset Error Tempco	T_{CB}	LSB s/°C Case temp rise		±0.01			+0.005		LSB/°C
Unipolar Offset Error Tempco	T_{CU}	LSB s/°C Case temp rise		±0.01			+0.005		LSB/°C

DIGITAL OUTPUTS

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE 0°C to +70°C MIN	TYP	MAX	−55°C to +125°C MIN	TYP	MAX	UNITS
Output Leakage Current, Logic LOW	I_{LOL}	V_O = 0.4V (3-State)			−50			−50	μA
Output Leakage Current, Logic HIGH	I_{LOH}	V_O = 2.4V (3-State)			50			50	μA
Output Voltage, Logic LOW	V_{OL}	I_{OL} = 4 mA		0.35	0.4		0.35	0.4	V
Output Voltage, Logic HIGH	V_{OH}	I_{OH} = −0.4mA	2.4	3.0		2.4	3.0		V
Short Circuit Output Current	I_{OS}	V_{CC} = MAX, Output HIGH, 1 sec		35			35		mA
Output Capacitance	C_{OUT}	(3-State)		9			9		pF

REFERENCE

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE 0°C to +70°C MIN	TYP	MAX	−55°C to +125°C MIN	TYP	MAX	UNITS
Reference Voltage	V_{REF}	V_{REF} OUT	2.49	2.500	2.51	2.48	2.500	2.52	V
Reference Current, Sourced	I_{REF}	V_{REF} to GND	8			8			mA
Reference Adjustment Range	R_{ADJ}	Recommended Range[4]	−1.0		−2.0	−1.0		−2.0	V

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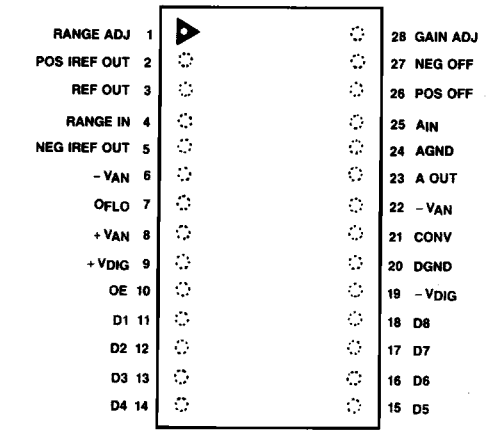
POWER SUPPLIES

PARAMETER	SYMBOL	TEST CONDITIONS	TEMPERATURE RANGE 0°C to +70°C MIN	TYP	MAX	−55°C to +125°C MIN	TYP	MAX	UNITS
Positive Digital Supply Current	I_{CC}	V_{DIG} = 5.0V		114			114		mA
		V_{DIG} = 5.5V					123		mA
Negative Digital Supply Current	I_{EE}	$-V_{DIG}$ = 5.0V		10			10		mA
		$-V_{DIG}$ = 6.0V		10			10		mA
Positive Analog Supply Current	$+I_{AN}$	$+V_{AN}$ = 5.0V		26			26		mA
		$+V_{AN}$ = 5.5V					26.5		mA
Negative Analog Supply Current	$-I_{AN}$	$-V_{AN}$ = 5.0V		43			43		mA
		$-V_{AN}$ = 5.5V					43.5		mA
Power Dissipation		V_{DIG} = V_{AN} = Nominal		0.965			0.965		W
Fs = 20 MHz		$-V_{DIG}$ = $-V_{AN}$ = 10% High					1.117		W

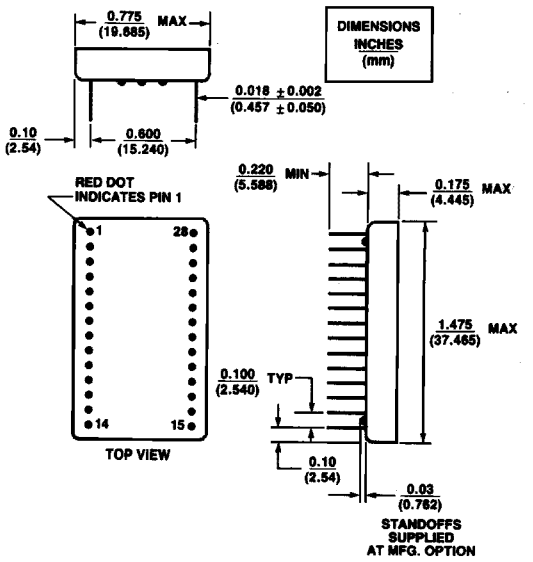
PIN ASSIGNMENTS

PIN	SYMBOL	FUNCTION
1	RANGE ADJ	Range Adjust
2	POS I_{REF} OUT	Isolated Reference Out, Positive, 2.5V
3	REF OUT	Reference Out, 2.5V
4	RANGE IN	Full Scale Range Adjust
5	NEG I_{REF} OUT	Isolated Reference Out, Negative, 2.05V
6	$-V_{AN}$	Negative Analog Supply Voltage
7	O_{FLO}	Overflow Detector, Active High
8	$+V_{AN}$	Positive Analog Supply Voltage
9	$+V_{DIG}$	Positive Digial Supply Voltage, +5V
10	OE	Output Enable Low
11	D1	Data Bit 1
12	D2	Data Bit 2
13	D3	Data Bit 3
14	D4	Data Bit 4
15	D5	Data Bit 5
16	D6	Data Bit 6
17	D7	Data Bit 7
18	D8	Data Bit 8
19	$-V_{DIG}$	Negative Digital Supply Voltage
20	D_{GND}	Digital Ground
21	CONV	Convert Low
22	$-V_{AN}$	Negative Analog Supply Voltage
23	A_{OUT}	Test Point (Amplifier Output, Flash Input)
24	A_{GND}	Analog Ground
25	A_{IN}	Analog Signal Input
26	POS OFF	Positive Offset Adjust
27	NEG OFF	Negative Offset Adjust
28	GAIN ADJ	Gain Adjust

PIN ASSIGNMENTS



PACKAGE OUTLINE



ORDERING INFORMATION

MODEL	TEMPERATURE RANGE	DESCRIPTION
SP 1070C	−0°C to +70°C	8-Bit, 25 MHz ADC
SP 1070B	−55°C to +125°C	8-Bit, 25 MHz ADC, MIL-STD-883C Screening

THEORY OF OPERATION

The SP 1070 consists of four circuit blocks: the input amplifier, the fullscale range amplifier, the 2.5 Volt reference, and the flash converter and its control logic. The analog and digital grounds are separated to provide flexibility in system grounding and decoupling. The additional isolation of the amplifier supplies from the flash supplies allows a wide range of supply voltages or decoupling schemes to be utilized.

The input amplifier is a DC stabilized feedforward design which overcomes the DC drift and warmup problems of a single stage design. It features two summing inputs which may be pin strapped together for 0.714 Volt (RS343) fullscale or used separately for 1 Volt (RS170) or 2.5 Volt fullscale nominal levels. A third summing input can provide a 1.25 Volt input range. Any of these pins which are not used as signal inputs may be used as offset adjustment points. Unused inputs should be left unconnected to maintain maximum amplifier bandwidth.

Typical sources can drive the 714-to-2.5K Ohm input impedance. External resistors to ground can be used to terminate 50 or 75 Ohm cabling. Higher input fullscale voltages can be applied by constructing an external "Tee" attenuator of the desired impedance.

The feedforward configuration provides two modes of adjusting system offset. Offset voltages may be applied to any of the unused summing inputs or to the amplifier non-inverting terminal at NEG OFF ADJ. Note that the operation of these two points is complementary — a positive voltage on a summing input will offset the amplfier output negatively, while the same voltage on the NEG OFF ADJ pin will force the amplfier in the positive direction. The NEG OFF ADJ pin is a high impedance point and is therefore preferred for use with trimpots or E2POTS. An external current output DAC can be used with any of the summing inputs to provide a current mode (high speed) programmable amplifier offset. The positive offset adjust pin can be used for this purpose when either of the video standard gains is chosen, and requires a DAC voltage compliance of only 1.25 Volts for a full-scale offset change (+1mA).

When the 1 Volt range is chosen, the normal factory trimmed ranges may be chosen by:

a) 0 to 1V — ground NEG OFF ADJ, POS OFF ADJ = unconnected
b) −0.5 to +0.5 — ground NEG OFF ADJ, connect POS IREF to GAIN ADJ
c) −1 to 0V — ground NEG OFF ADJ, connect VREF to GAIN ADJ

A resistor isolated (500 Ohm) analog output testpoint is brought out for debugging or application circuit use. Note that it will show any offsets necessary for proper operation over the −25mV to −2.025V (nominal) input range at the flash input. Amplifier settling time is optimized at the factory by an internal variable capacitor.

The 2.5 Volt reference is a fixed positive reference used to generate tracking outputs for pin strap offset and gain options. V_{REF} is normally tied to the inverting range amplifier input to generate the −2.025V nominal reference to the bottom of the flash resistor ladder. User adjustment of system gain is normally done at the range amplifier adjust input. The V_{REF} output is buffered and up to 8mA is available for use in application circuits. The second output, POS I_{REF}, provides a 2.5K Ohm series resistor to generate 1mA nominal into a virtual ground. This pin is especially useful for supplying a reference current to an external DAC for programmable gains or offsets.

The range amplifier is an inverting amplifier with a power buffer used to generate the large currents needed to drive the flash resistor ladder. It directly sets the fullscale range at the flash converter. Any gain adjustment should be done here at the range adjust pin (normally grounded for factory laser trimmed nominal gains). The settling time to 0.1% of this amplifier is less than 1 s. By use of an external current mode DAC, the fullscale range of the converter may be updated very quickly, during one horizontal flyback interval, for example. A DAC drawing 0 to 1mA from the RANGE ADJ pin can program an effective two-to-one gain increase at the expense of some loss of differential linearity at the highest gains. Gain decreases are best accomplished by attenuating at the input.

The input amplifier, range amplifier and reference all share the isolated supplies $+V_{AN}$ and $-V_{AN}$. For minimal power dissipation the best choice for these supplies is +5V, −5.2V, but any values up to ±15V are possible, allowing the system designer to choose the "cleanest" supplies available. The flash converter requires +5V nominal and a negative supply of −3 to −6 Volts (−5 Volts nominal if tied to $-V_{AN}$) at V_{CC} and V_{EE} pins respectively. Only 53mA of current is necessary from a single −5.2 Volt supply when V_{EE} is tied to $-V_{AN}$.

The flash converter requires a TTL convert clock from DC to 25 MHz. The outputs are enabled when OUT EN is at TTL low. The OVERFLOW output is not three-stateable, and is not affected by the OUT EN control.

OUTPUT CODING OF SP 1070

The SP 1070 outputs are in complement binary form. The table below gives the input voltage at pin 25 for both 0 to 1V fullscale operation (pins 26, 28 open) and for ±0.5V fullscale (pin 3 to pin 28). For a negative input voltage range (−1 to 0V) tie pin 3 to pin 26. Operation at other ranges will be similar to the complement binary and offset complement binary ranges shown. Binary coding requires external inverters at outputs.

+ Unipolar	Bipolar (V_{IN} at Code Centers)	− Unipolar	Code Output	Overflow Output
−0.0039	−0.5039	−1.0039	1111 1111	1
0.0000	−0.5000	−1.0000	1111 1111	0
+0.0039	−0.4960	−0.9960	1111 1110	0
+0.4960	−0.0039	−0.5039	0111 1111	0
+0.5000	0.0000	−0.5000	1000 0000	0
+0.992	+0.4920	−0.0080	0000 0001	0
+0.996	+0.4960	−0.0039	0000 0000	0
+1.000*	+0.5000*	0.0000*	0000 0000*	0*

Denotes underflow not detected at overflow output

CALIBRATION

The SP 1070 is laser trimmed for unipoar and bipolar gains and offsets utilizing the 1 Volt fullscale range input (pin 25). The other input resistors are passively trimmed to correctly ratio the input resistor at pin 25. Normal room temperature operation will require no external trimming. Offset and gain errors arising from earlier stages of the system, or the utilization of the programmable gain and offset pins for more sophisticated applications may require external gain or offset trimming. Pins 2 and 3 provide positive voltages and pin 5 provides a negative reference voltage which exhibit excellent power supply rejection and should be used to drive any external trimpots or current mode D/A converters used for trimming.

One simple offset adjustment circuit is shown below. This circuit utilizes the internal resistors at pins 2 and 5 to minimize the ratio drift that external resistors will exhibit. No input pins are "used up" by this circuit, allowing it to be used for all unipolar input ranges. Note that the resistor at pin 2 will show some variation from the absolute 2.5K Ohm value shown, as it has been laser trimmed when connected to pin 28 for bipolar offset adjustment. This circuit uses pin 28 and thus cannot easily be used to trim bipolar mode offset — the circuit of Figure 2 will trim both unipolar and bipolar offsets. Note that now pin 28 is "used up", and is unavailable for use in setting the fullscale input range, as in the ±0.357 Volt fullscale input range. Figure 3 shows a circuit which does not need pin 28 and allows independent adjustment of unipolar and bipolar offsets. Unipolar offset should be adjusted first, as this trimpot will affect both unipolar and bipolar offsets. Note that for bipolar operation only, pin 27 can be grounded and the 200 Ohm trimpot is unnecessary.

The gain of the SP 1070 is adjusted by sinking or sourcing current into the RANGE ADJ (pin 1). This operation will cause the −2.05 Volts at the flash converter reference to change, thus directly setting the fullscale range. The voltage at NEG I_{REF} (pin 5) will change correspondingly. When NEG I_{REF} is used to drive external offset adjustment rimpots in fixed gain applications the gain should be adjusted as early in the trim procedure as possible. This will minimize the interaction between the gain and offset trims.

Note that external trim circuits which use the NEG I_{REF} pin to set the reference of a multiplying DAC (such as a DAC-08) will exhibit a very useful feature: the offset can be set to any percentage of fullscale which is desired, than as the gain is changed over the allowed 2 to 1 range, the offset will track accordingly.

Some useful, although complex to analyze, circuits can be used for gain increases. For example, after tying pin 3 to pin 4 for normal operation, pin 5 can be tied to pin 1 for a 25% gain increase (−1.52 Volts fullscale at the flash). If an external resistor is added, as in Figure 4, infinitely adjustable gains of 0 to 10% can be achieved, although temperature stability will be determined by the temperature stability of the ratio of external to internal resistors.

Gain reduction (setting the flash reference more negative than the −2.05V nominal) is discouraged, as the range amplifier headroom from the NEG V_{AN} supply is limited at minimum NEG V_{AN} values. The reference voltage at the flash can safely be brought to −2.2 Volts only if the NEG V_{AN} supply is more negative than −4.9 Volts. Gain reduction is easily done by resistor padding at the inputs or by choice of an appropriate input pin.

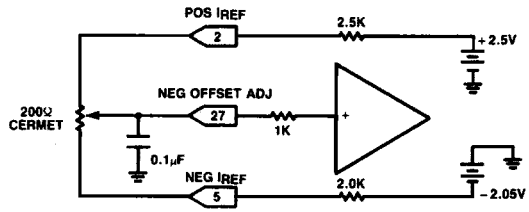


Figure 1. Simple Unipolar Range Offset Adjustment Circuit

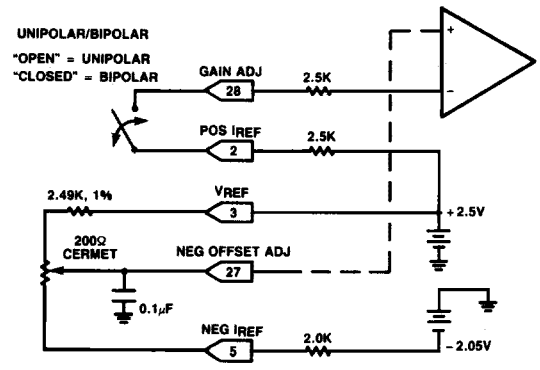


Figure 2. Unipolar/Bipolar Range Offset Adjustment Circuit

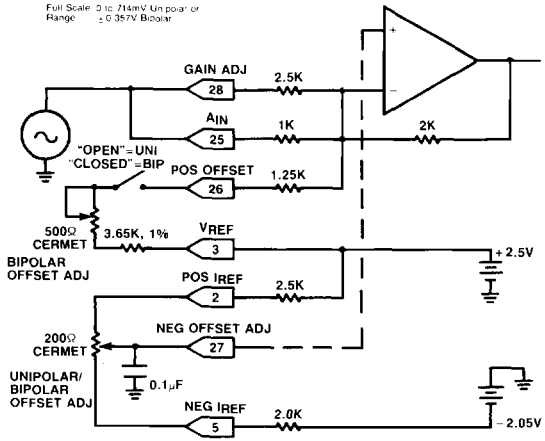


Figure 3. Offset Adjustment Circuit for Bipolar Range When Pin 28 is Used in Pin Strapped Gain Selection

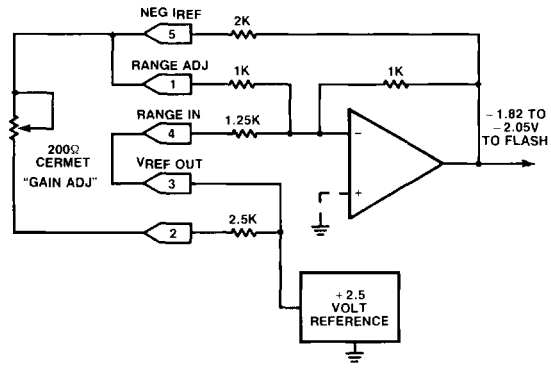
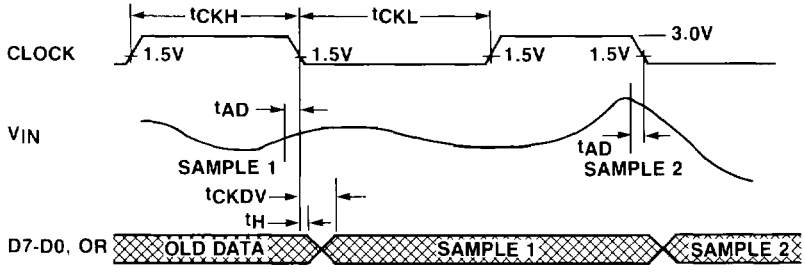
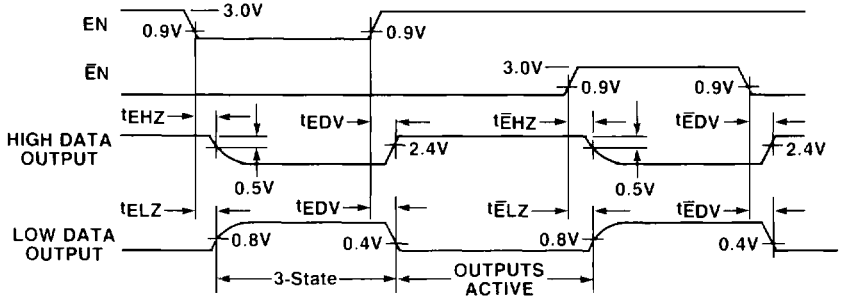


Figure 4. Gain Adjustment Circuit for 0 to 10% Gain Increase

System Timing Diagrams

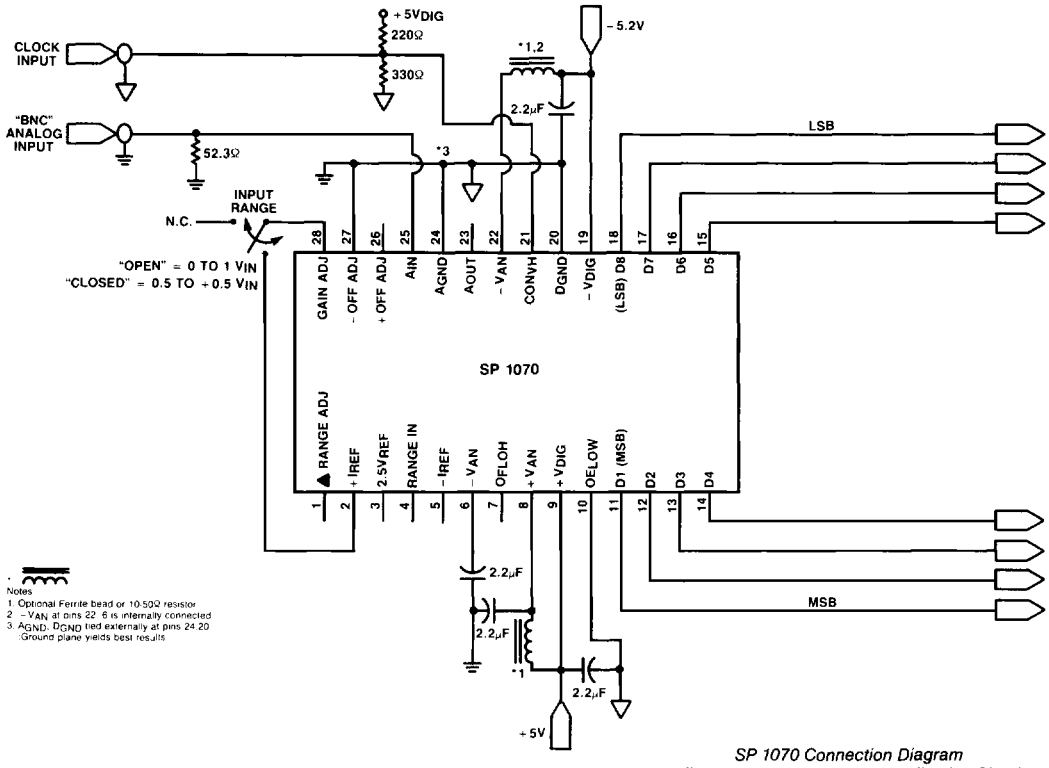


tCKDV and tH measured at output levels of 0.8 and 2.4 volts.



TIMING CHARACTERISTICS (T_A = 25°C, V_{CC} = +5.0V, V_{EE} = 5.2V. See System Timing Diagram.)

Parameter	Symbol	Min	Typ	Max	Unit
INPUTS					
Min Clock Pulse Width — High	t_{CKH}	—	5.0	—	ns
Min Clock Pulse Width — Low	t_{CKL}	—	15	—	ns
Max Clock Rise, Fall Time	$t_{R,F}$	—	100	—	ns
Clock Frequency	f_{CLK}	0	30	25	MHz
OUTPUTS					
New Data Valid from Clock Low	t_{CKDV}	—	19	—	ns
Aperture Delay	t_{AD}	—	4.0	—	ns
Hold Time	t_H	—	6.0	—	ns
Data High to 3-State from Enable Low*	t_{EHZ}	—	27	—	ns
Data Low to 3-State from Enable Low*	t_{ELZ}	—	18	—	ns
Data High to 3-State from Enable High*	t_{EHZ}	—	32	—	ns
Data Low to 3-State from Enable High*	t_{ELZ}	—	18	—	ns
Valid Data from Enable High (Pin 20 = 0V)*	t_{EDV}	—	15	—	ns
Valid Data from Enable Low (Pin 19 = 5.0V)*	t_{EDV}	—	16	—	ns
Output Transition Time* (10%-90%)	t_{tr}	—	8.0	—	ns



SP 1070 Connection Diagram
Minimal Power Dissipation Application Circuit

DYNAMIC TESTING OF THE SP 1070

The SP 1070 has been designed and characterized upon a high speed dynamic test system developed at Hybrid Systems. It's wide bandwidth amplifier and Gray scale encoded flash converter provide excellent dynamic performance at sampling frequencies to 25 MHz.

All dynamic performance characteristics as well as all DC trimming and linearity specifications are 100% tested at a sample rate of 20 MHz. Note that the DC linearity specifications become even better as the sample rate is lowered. SP 1070 "B" grade parts are tested at 20 MHz over the full military temperature range. The parts are also characterized here at room temperature at 25 MHz.

Figures (A) and (B) shown an FFT and a signal-to-noise + distortion number at each frequency input. Any harmonics of the fundamental which show in the graphs are due to integral nonlinearity in either the input amplifier or the flash converter transfer curve. Any noise in the hybrid or any dynamic differential linearity errors will raise the noise floor of the graph above that generated by 8-Bit quantization noise floor of an ideal converter. Note that higher order harmonics will alias back down into the FFT spectrums shown. The SNR number as defined here represents a figure of merit representing the total dynamic error of the converter. Integral non-linearity will usually be the error which limits this number, as any harmonic spectral lines will rapidly degrade this number. However, this method of measurement insures that all potential sources of "spectral noise" have been accounted for, including potential oscillations of the reference, sub-harmonics of the clock frequency due to crosstalk, code dependent ground currents or any other error not related to absolute gain or offset. A SINAD of 47.1 dB at 1.12 MHz can be converted to 7.53 effective bits. The dominant error source is the two harmonic lines evident in the graph. Thus the integral linearity error at 1.12 MHz input can be seen to be better than 1/2 LSB.

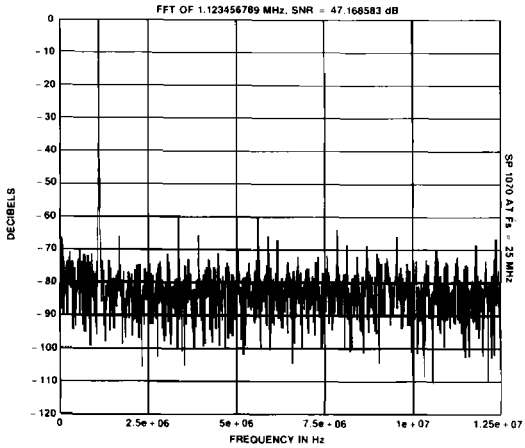
At 4.45 MHz input the FFT plot shows significant lines, aliased by the sampling process, at the second, third, fifth, seventh and ninth harmonics. While none of these harmonics are greater than 50 dB below the fundamental, the rms sum of these lines is primarily responsible for the SNR decrease from the ideal 49.96 dB to the 41.6 dB shown. The 4K point FFT's done here at Hybrid Systems are four times the length of those done by many manufacturers. This results in a plotted quantization noise floor 12 dB below that of other manufacturer's graphs. The advantage is that the cause of any SNR decrease can be identified — here the integral linearity of the amplifier/flash combination can be identified as the limiting factor to the SNR number. It can be said with confidence that no "spurious codes" or extremes in differential linearity error have raised the noise floor and limited the SNR measurement. Note that shorter length FFT's with the resulting raised plotted noise floor might not show these lines at all — they could be "buried" in the noise floor, and no such judgment would be possible.

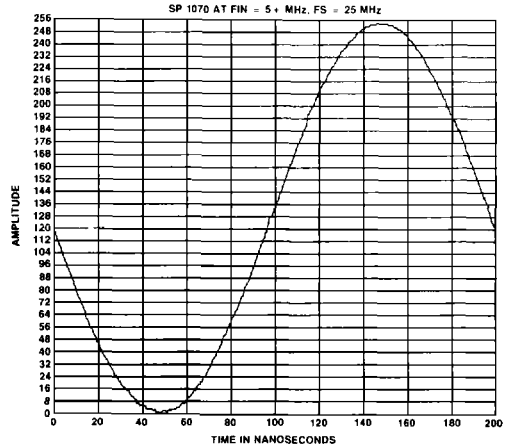
In addition, the SNR number as measured here at Hybrid is actually the average of 10 SNR computations. If a non-Gray scaled flash is run near its power bandwidth limit, a finite probability exists that the converter can "make a mistake" in assigning a binary number to a voltage which was rapidly changing. This "mistake" would show up on an FFT as the raised noise floor, as described above. By measuring the variation in the 10 SNRs which are averaged, it is possible to detect this kind of spurious code. The Gray scaled flash converters used in the SP 1070 do not exhibit this type of catastrophic error. Some degradation with increasing input slew rate is unavoidable — it can only be helped by the use of an extremely fast sample/hold in front of the analog input. However, the use of an internal Gray scale as a minimum distance code will have a useful effect upon the severity of any errors: even when the comparator determining the MSB is in error, the binary number which is output will be only a few LSB's away from the correct code. Thus the relative accuracy of the SP 1070 will be seen to degrade with increasing slew rate in a gradual and graceful manner — no "sparkle codes" will show up in the reconstructed video output, and at most the output will exhibit a dither-like noise, which the eye would average out if displayed upon a screen. The new problem is how to accurately specify the dynamic performance of such a device.

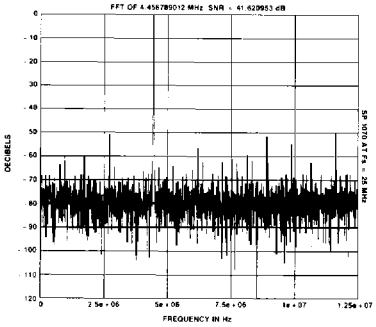
The dynamic testing and specifications of this part were designed to give a true indication of its performance. A new specification, dynamic differential linearity, is used to quantify the degradation in accuracy inherent in flash converters as the input signal slew rate is increased. It can be shown from histogram testing of Gray scale error-corrected flash converters, that the first DC specification which begins to get worse as input signal slew rate increases is the width of each code. Normally the code widths are measured with a DC voltage reference and are shown in units of differential linearity error, which is the difference, in fractional LSB's, of each code width from the ideal code width. Dynamic differential linearity error is a measure of the width of each code when a pure sine wave of known frequency and amplitude (and hence one of defined maximum slew rate) is applied to the flash converter.

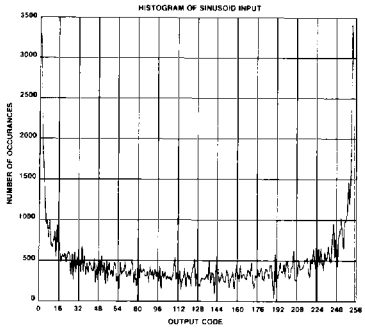
Histograms of pure sine waves are used to compute the code widths. Figure (C) shows the reconstruction of a sine wave of just over 5 MHz applied to the input of an SP 1070. Thirty buffers of 4K points each of these sine waves are stored, then used to generate the histogram of Figure (D). A curve fitting algorithm is then run to compute the "best fit ideal sinusoidal histogram" of Figure (E). The ideal histogram is used to calculate the number of times each code should have occurred. The number of actual occurrences of each code is ratioed to this ideal number. Codes which occurred fewer times than expected exhibited small code widths. The difference between the actual and the expected code widths can be normalized into units of differential linearity error in fractional LSB's. A plot of this "dynamic differential linearity error" is shown in Figures (F) and (G). The first was run with an extremely low frequency input, the second at 5+ MHz, and both were run at a sampling frequency of 25 MHz. An error of −1 LSB would indicate a missing code. Operation at lower sampling frequencies will yield even better dynamic differential linearity than the plots at 25 MHz show.

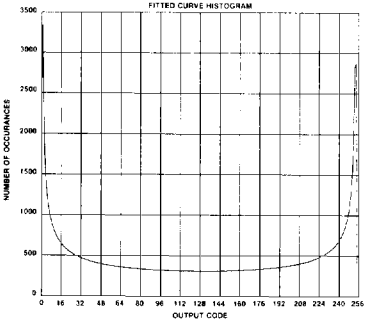
The specifications show an "input power bandwidth" number. This number is not related to the amplifier frequency response — typically the amplifier is only 2 dB down at 20 MHz fullscale inputs. What this number is meant to indicate is that for signals exhibiting slew rates equivalent to the slew rate of a fullscale input of this frequency (or lower), the code widths are guranteed to be greater than zero — no missing codes. Signals of greater slew rate may begin to show the effects of the Gray scale error minimization — appearing slightly noisy, especially near major transitions. If the application requires absolute fidelity in the reconstruction of fullscale signals of comparable slew rates, the use of a properly timed sample/hold in front of the analog input is recommended. An example would be where a system was attempting to demodulate a fullscale 10 MHz intermediate frequency. Note that most bandwidth limited signals, such as broadcast quality video, or signals limited by an external anti-aliasing filter, exhibit only small amounts of high frequency energy, and that 1/2 scale inputs at twice the 6 MHz input power bandwidth exhibit the same slew rate as fullscale inputs at 6 MHz, and are thus subject to only minimal degradation.






FFT OF 4.456789012 MHz SNR = 41.620953 dB
DECIBELS
FREQUENCY IN Hz
SP 1070 AT Fs = 25 MHz


HISTOGRAM OF SINUSOID INPUT
NUMBER OF OCCURANCES
OUTPUT CODE


FITTED CURVE HISTOGRAM
NUMBER OF OCCURANCES
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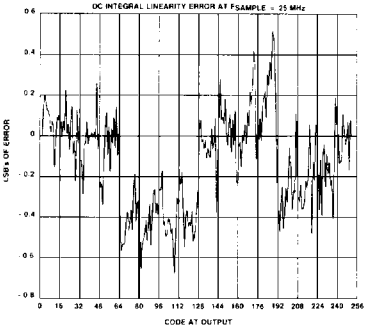
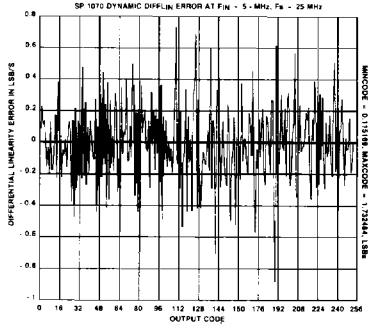
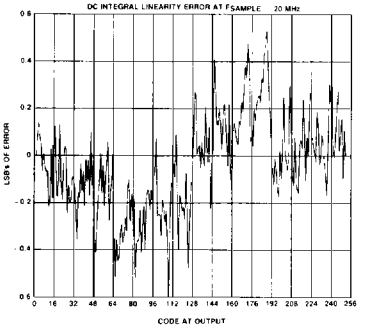

DC INTEGRAL LINEARITY ERROR AT FSAMPLE = 25 MHz
LSB's OF ERROR
CODE AT OUTPUT


SP 1070 DYNAMIC DIFFLIN ERROR AT FIN = 5 MHz, Fs = 25 MHz
DIFFERENTIAL LINEARITY ERROR IN LSB'S
OUTPUT CODE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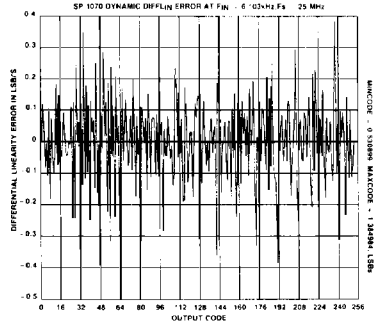
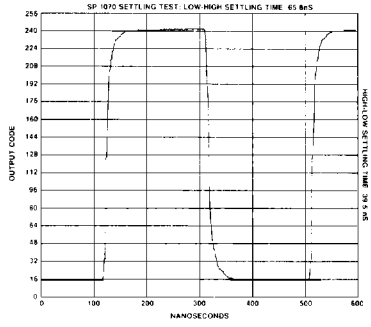
LSB's OF ERROR
CODE AT OUTPUT


SP 1070 DYNAMIC DIFFLIN ERROR AT FIN = 6.703Hz Fs = 25 MHz
DIFFERENTIAL LINEARITY ERROR IN LSB'S
OUTPUT CODE


SP 1070 SETTLING TEST: LOW-HIGH SETTLING TIME 65 ns
OUTPUT CODE
NANOSECONDS