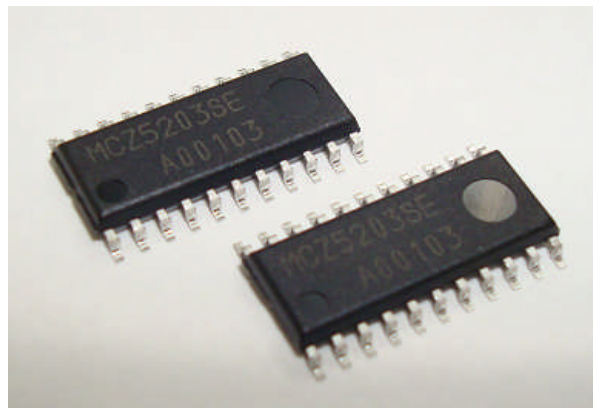




新電元

LLC
Current Resonant
Mode Controller for
Bridge Converter

MCZ5203SE



Application Note (ver.1.0en)

新電元工業株式会社



MCZ5203SE
Standard
Power Supply








Cautions for Use

Thank you for purchasing our products. This manual contains important information on the safe use of our products. Your safety is of the utmost importance to us.

Please read these instructions carefully before using our products.

The following symbols mean:

	Warning	Improper use of the products can result in death, serious injury, or expensive damage to equipment.
	Caution	Improper use of the products can result in minor injuries or damage to equipment.

	Warning	Although we are constantly making every effort to improve the quality and reliability of our products, there nevertheless remains a certain probability that the semiconductor products may occasionally fail or malfunction. Please take careful precautions against product failures or malfunctions to avoid any injuries, fire accidents or social loss by implementing safety designs such as redundancy designs, designs for fire spread prevention, and designs for preventing malfunctions.
	Warning	<p>Our semiconductor products listed in this document are not designed or manufactured to be used in devices or systems requiring extremely high levels of quality and reliability, or the failure or malfunction of which may directly threaten human lives or cause injury.</p> <p>In the cases where the products are to be used in devices or systems for special applications or devices or systems for specialized applications shown below, always make sure to consult us in advance.</p> <p>Special Applications Transportation devices (automotive, marine, etc.), communication devices for core network, traffic signal devices, fire prevention/anticrime devices, various safety devices, medical devices, etc.</p> <p>Specialized Applications Nuclear power control systems, aircraft and aerospace devices, submarine relay devices, and systems for preserving life, etc.</p> <p>Even if it is not for a special or specialized application, when IC products are to be used for devices or systems that are desired to last for a long period under continuous operation, please make sure to consult us in advance.</p>
	Caution	Do not attempt under any conditions to repair or modify IC products by yourself. Doing so could result in electric shock, device breakage, fire, and malfunction.
	Caution	When an abnormal condition occurs, an excessive voltage or under voltage may be generated across the output terminals of the circuit. Install preventative measures (e.g. over-voltage protection, over-current protection) for the device by considering the possibility of a malfunction and/or breakage of a load in an abnormal condition.
	Caution	Do not switch on the circuit before confirming the proper connection and polarity of input and output terminals as an erroneous connection may cause breakage of the protection device or smoke/fire.
	Caution	Do not use the circuit beyond the rated input voltage and install a protection device on the input rail to prevent smoke/fire that may be caused from an abnormal condition.
	Caution	If a breakdown or other abnormal condition occurs during the use of the device, immediately stop power to the device and consult us at your earliest possible convenience.

- We reserve the right to make any changes to the contents of this manual without prior notice in accordance with modifications to IC products.
- Details of specifications should be exchanged at the adoption of the IC products.
- All information included in this manual is believed to be accurate and reliable. However, our company takes no responsibility for any injury or damage incurred when using the IC products as described in this manual. Neither do we take any responsibility for issues arising from infringement of patent or other rights caused by using this manual.
- The provision of this manual does not guarantee the right to use any third party's patent or other rights, or grant permission to use the patent or other rights of our company.
- No part of this manual may be reproduced or copied without the specific written consent of Shindengen Electric Mfg. Co., Ltd.

We are happy to provide circuit design support for safe use of the IC. Please consult our sales representative .

1 : General description	
1.1: Features	4
1.2: Block diagram (SOP22)	4
1.3: Pin assignment	5
1.4: Functions	5
1.5: Application circuits	6
2 : Symmetric LLC converter Operating description	
2.1: Features	7
2.2: Fundamental circuitry	7
2.3: Operating waveform example	7
2.4: Control characteristics	8
2.5: Major parameters and components	8
2.6: IC operation	9 - 10
3 : Selecting peripheral components	
3.1: Oscillator (Rt)	11
3.2: Vsense brown-out protection (RvsenseL)	12
3.3: Soft start (Css)	12-13
3.4: OCP (Rocpdet/RocpL)	13-14
3.5: di/dt protection	14
3.6: Timer latch protection (CTimer)	15
3.7: High side floating Vcc (VB)	16
3.8: Gate driver	16
4 : Circuit diagram	
4.1: Typical circuit example	17
5 : Dimensions	
5.1: SOP22 (MCZ5203SE)	18

1 General description

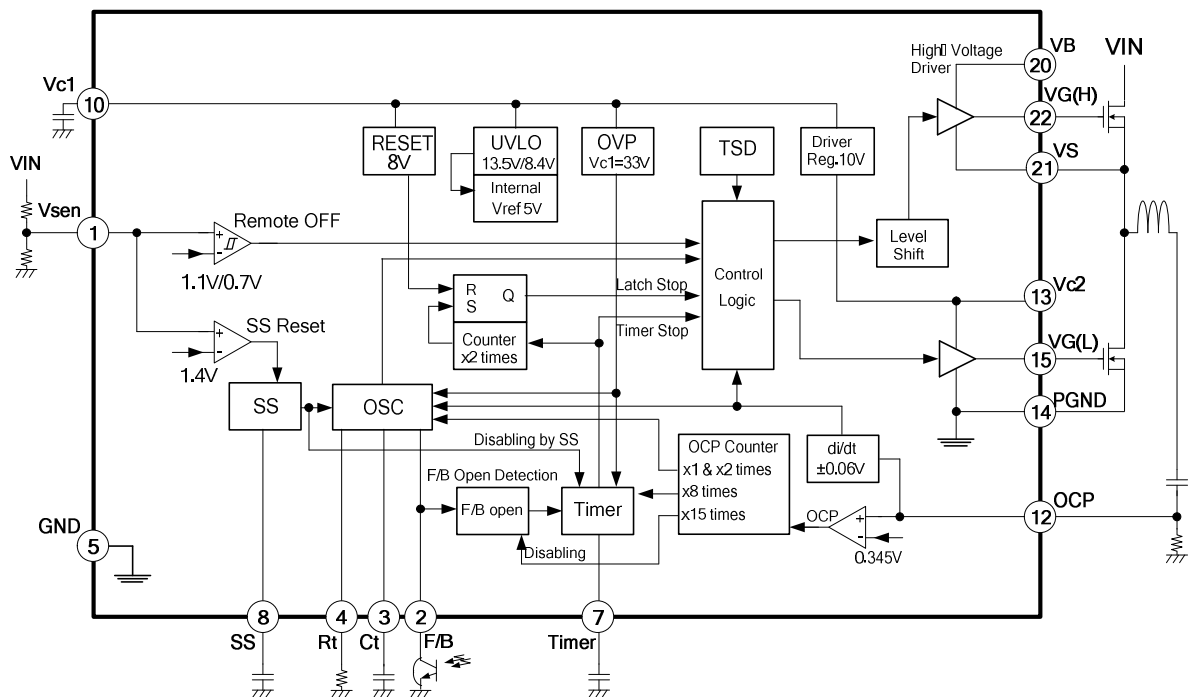
MCZ5203 is an advanced symmetric LLC current resonant mode controller for bridge converter. Built-in high voltage direct gate drivers, control circuit and optimized protections allow simplified and space/cost-saving design of power supplies for :

- Large screen flat panel TVs (PDP / LCD) PSU
- Laser printer PSU
- High power adapters

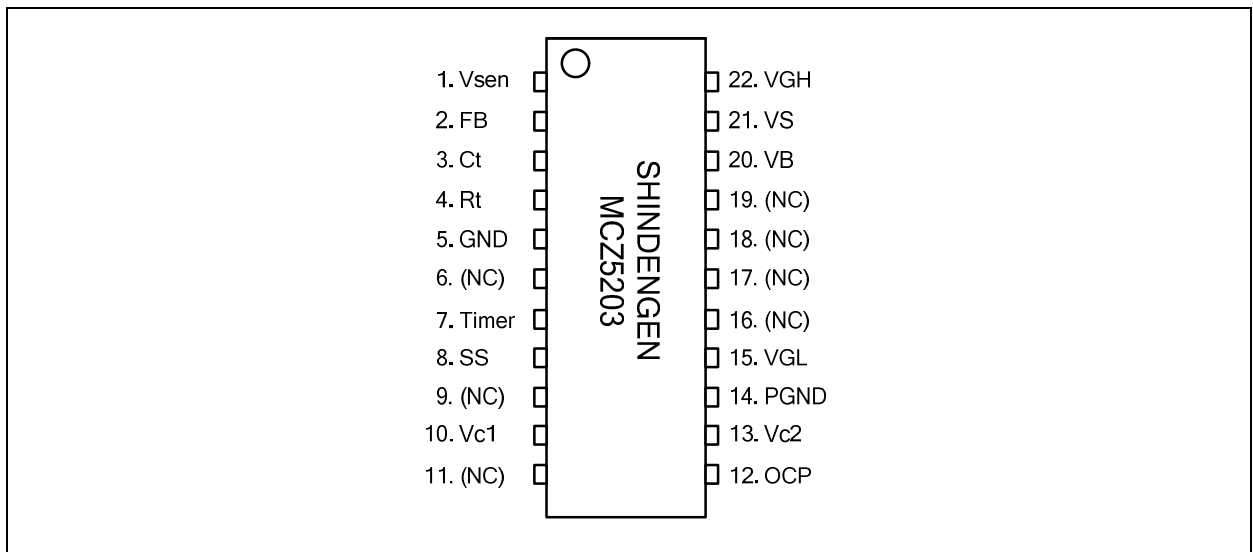
1.1 Features

1. Robust 600V gate driver directly drives high side Switch.
2. Optimized gate drive capability minimizes the number of components for gate drive circuit.
3. Optimized protective functions (OCP/burst/Timer delayed latch/Thermal) for LLC converter
4. Advanced **ZVS boundary chaser** (capacitive mode protection) eliminates below resonant (capacitive di/dt) operation.
5. OCP operates by detecting peak primary current with 0.345V / threshold.
6. Vcc supplies up to 35V with 13.5V/8.4V UVLO
7. Built-in voltage regulator of 10V for gate driver
8. Independent high side / low side Gate driver UVLO with hysteresis
9. Adjustable soft starting function
10. Anti-di/dt startup function eliminates improper startup of Non ZVS operation
11. Optimized brown out protection

1.2 Block diagram (SOP22)



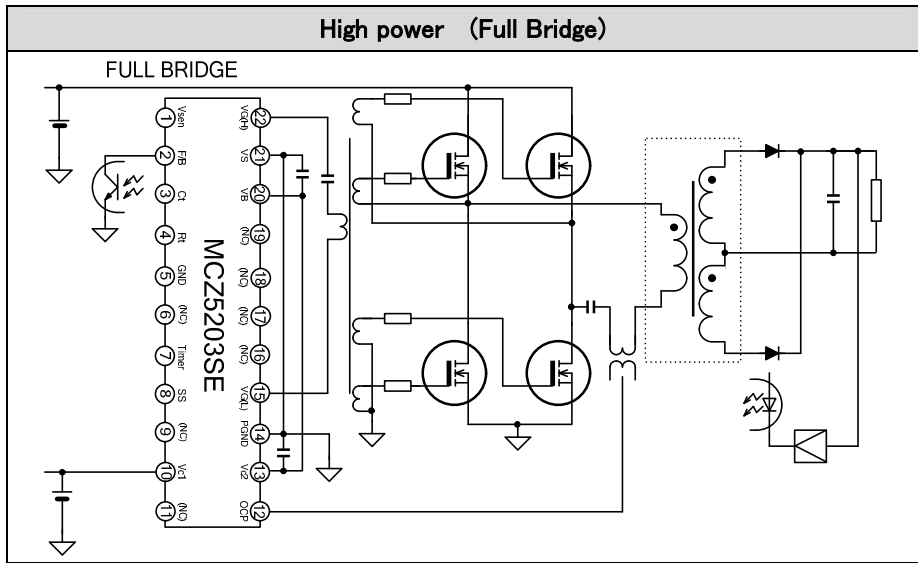
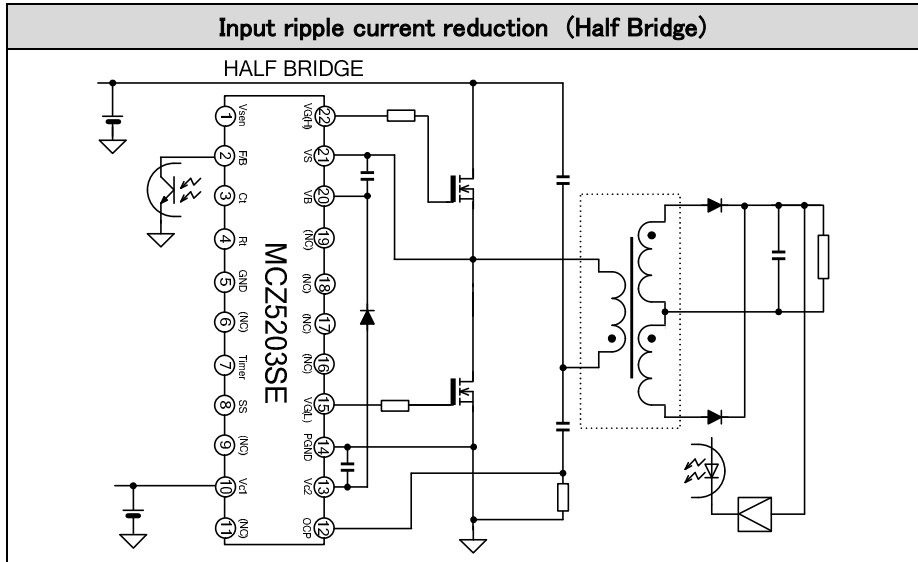
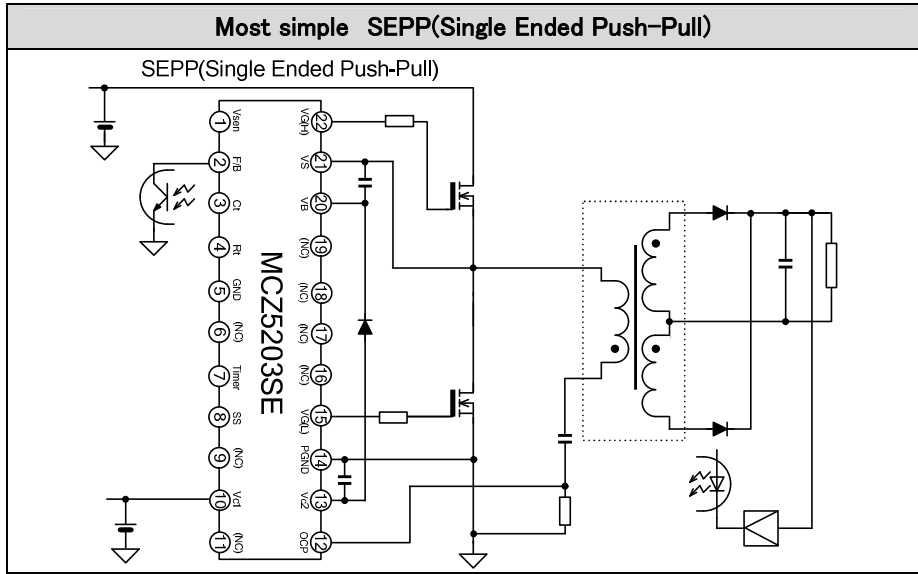
1.3 Pin assignment



1.4 Functions

Pin number SOP22	name	function
1	Vsen	DC input voltage monitoring
2	FB	Feedback signal input with Feedback loop open detection
3	Ct	Timing capacitor Ct determines Dead time and fmin (minimum operating frequency) and also fss(startup frequency)
4	Rt	Timing resistor Rt determines fmin
5	GND	Signal ground. This pin should be connected to PGND directly.
7	TIMER	CTimer determines the time period of burst mode in OCP or another abnormal operation.
8	SS	Startup timing capacitor C _{ss} determines the soft-starting time
10	Vc1	Voltage supply input for control circuit with 13.5V/8.4V UVLO Maximum rated voltage is 35V
12	OCP	Main resonant current sensing with +0.345V threshold for peak current limiting , +/- 60mV for didt protection
13	Vc2	Voltage regulator output for Gate driver Vc2=10V.
14	PGND	Power ground This pin should be connected to low side MOSFET source directly
15	VGL	Low side gate driver output
6,9,11,16, 17,18,19	(NC)	No connection
20	VB	Voltage source of High side gate driver supplied from Vc2 through bootstrap circuit
21	VS	Floating driver reference voltage (= Source pin of high side MOSFET)
22	VGH	High side gate driver output

1.5 Applicable circuits



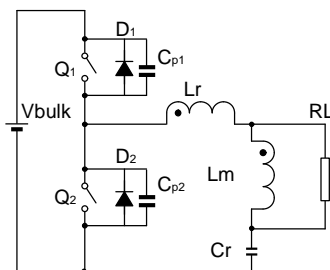
2 Symmetric LLC converter Operating Description

2.1 Features

Symmetric LLC resonant converter application is expanding widely due to its extremely high power conversion efficiency and low noise characteristics. It's resonant tank consists of L/L/C connected in series. ZVS/ZCS operation minimizes switching loss and voltage spike.

- The voltage applied to main switch is clamped to input voltage (V_{bulk}), consequently no spike voltage is generated.
- Main switch turn-off current can be kept to constant and low level independent of load condition.
- Transformer is excited symmetrically, thus magnetics size can be minimized.
- Sinusoidal resonant current waveform results in extremely low EMI characteristics.
- Output rectified current is also partially sinusoidal, and Trr loss and switching noise can be minimized.
- The voltage applied to output diode is clamped to the output voltage (or x2) independent of load condition or input voltage.
- Excellent cross regulation characteristics for multiple output converters due to symmetric bridge operation.
- No requirement of auxiliary 3rd winding helps to optimize resonant condition and transformer design

2.2 Fundamental circuitry(SEPP)



- L_r :1st resonant inductance
- L_m :2nd resonant inductance (magnetizing inductance)
- C_r :resonant capacitance
- $C_{p1/2}$:ZVS resonant capacitance
- $Q1/Q2$:Main switch
- $D1/D2$:Commutating diode
- R_L :Equivalent Load resistance

Fig.1 LLC configuration

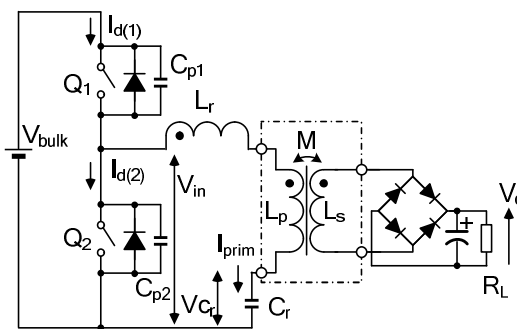


Fig.2 simplified dc/dc converter

2.3 Operating waveform example

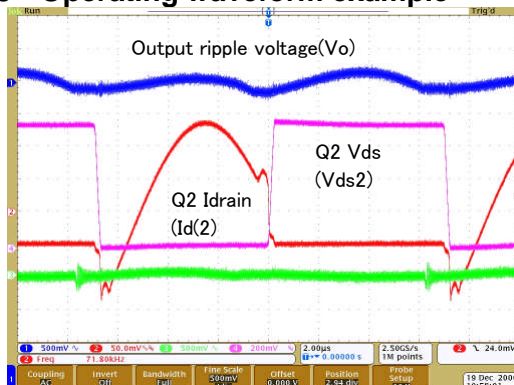


Fig.3 Vds / Idrain / Vo ripple

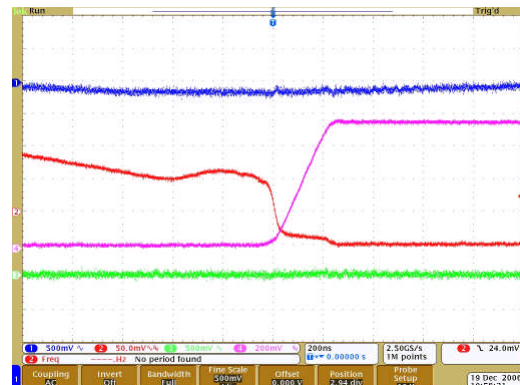


Fig.4 Zoom of turn off period

2.4 Control characteristics

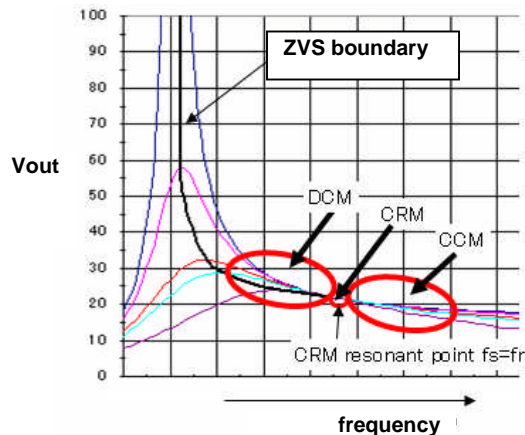


Fig.5 Output voltage vs operating frequency characteristics

Voltage vs. frequency characteristics are shown in Fig.5. LLC converter operates in above-resonance region. (above ZVS boundary)
Output voltage can be stabilized by varying operating frequency, decreasing the operating frequency when input voltage becomes lower or load becomes larger, and increasing when higher or smaller respectively.

2.5 Major parameters and components

Table 1. Major parameters

Vc1	IC Vcc supply	15-22Vdc is recommended.(min.14.0V for startup in worst case)
Vbulkreset	Brown-out detection voltage threshold	Brown-out protection operating voltage. The threshold value is determined considering resonant condition and hold-up time.
fmin	Minimum frequency	Fmin is determined considering resonant frequency at Vin min / Po max condition.
fmax	Maximum frequency	Fmax is determined considering controllable area at Vbulk max with min load and ZVS condition.
fss	Startup frequency	Fss is determined considering MOSFET Vds,output diode inrush current and Vout rise timing during startup
tss	Soft starting time	Required soft starting time
tTIMER	Burst mode operation interval	Especially important for short circuit condition and feedback loop open condition. See section 3.6

Table 2 .Recommended components

RvsenseH	Vbulk divider high side	Isense=1uA required High voltage assured type is recommended.
Ct	Timing capacitor	Ct determines fmin / fmax / fss / DT.Stable temperature characteristics type is recommended. In case of MLCC, type CH or COG.
RocpH	Current sensing filtering resistor	Primary current sensing filtering resistor. Around 10 ohm is recommended.
CocpL	Current sensing filtering capacitor	Primary current sensing filtering capacitor.1000pF-10000pF.
Rfb	I(F/B) limitation resistor	Limiting I(F/B) and setting fmax. Normally a few k ohms. Refer to characteristic diagrams.

Table 3. Circuit constants obtained from the formulas

RvsenseL	Vbulk divider low side	Obtained from Vbulkreset and RvsenseH.
Rt	Timing resistor	Obtained from fmin and Ct
Rocpdet	Sensing resistor	Primary resonant current sensing
RocpL	OCP sensing divider	Primary current sensing voltage divider
Css	Soft start timing capacitor	Obtained from tss.
Ctimer	Burst operation timing capacitor	Obtained from ttimer

2.6 IC operation

Power ON(mode A):

Under the condition of input bulk voltage V_{bulk} is applied ($V_{sense} > 1.4V$), operation starts when V_{c1} terminal voltage reaches 13.5V. After soft starting period (t_{ss}), the frequency is stabilized at nominal operating frequency depending on resonant tank and input/output condition.

Power ON(mode B):

When V_{bulk} is applied after V_{c1} is supplied, gate drive pulse is generated at $V_{sense} > 1.1V$ with fixed fss operation. Then normal soft starting operation begins when V_{sense} reaches 1.4V and operation is stabilized in normal operating frequency after the soft starting period as mode A.

Power OFF(mode A):

Under the condition of input bulk voltage V_{bulk} is applied ($V_{sense} > 1.4V$), IC operation stops when V_{c1} reaches the threshold of V_{c1} UVLO OFF (8.4V).

Power OFF(mode B):

When V_{bulk} decreases under the condition of continuous V_{c1} supplied, operating frequency decreases toward f_{min} . The frequency starts increasing to f_{ss} level soon after V_{sense} decreases to 1.4V. Gate drive stops when V_{sense} voltage decreases to 0.7V.

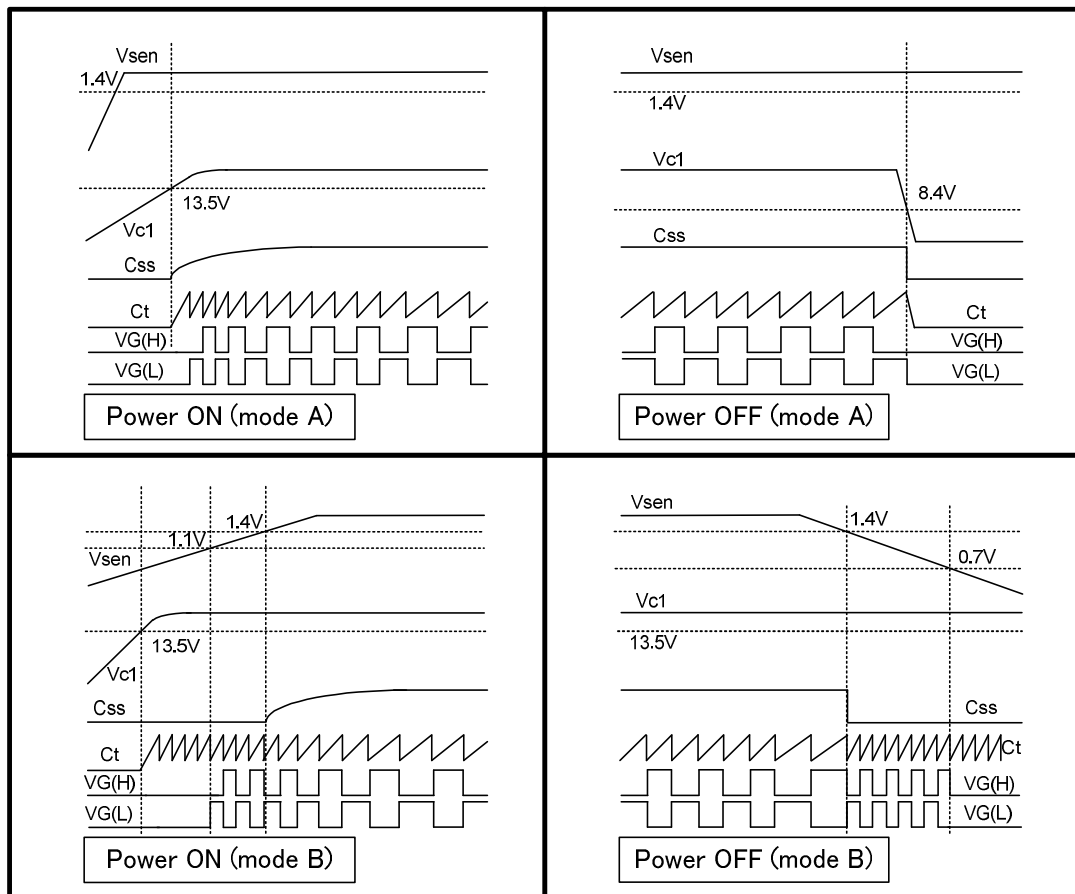


Fig 6. Power ON / OFF timing diagram

Under Abnormal condition:

a) Feedback loop open:

When operation is out of control due to input/output conditions beyond the controllable operating area, the frequency becomes to minimum (**fmin**). F/B loop open detector then will be activated and the gate output stops after the period of **tTimer** set by timing capacitor (**CTimer**). After the time period set by the burst mode(**tb**), the output restarts and is latched off in the case where this timer-latch protection operating cycle repeats twice. Restart **Vc1** to release latching.

b) OCP / OLP :

When the voltage applied to OCP terminal exceeds **Vocpth** (0.345V typ), the frequency increases instantaneously and when this condition is retained, the operation follows same as above.

c) Di/dt Timerection :

In close to below resonant condition, di/dt Timerection activates by detecting the threshold of **Vdidt** (+/- 60mV), limits the frequency to decrease and restrains the output voltage. See section 3.5 for detail.

d) Thermal Timerection :

If IC internal temperature exceeds 140°C , output will be stopped with 40°C temperature hysteresis.

Remarks:

When **Vbulk** keeps low level, the converter is unable to stay in normal operation due to the F/B loop open Timerection and **Vsense**, even if **Vc1** exceeds 14V. If starting the operation with **Vbulk** slow-up is required, adding external components as described below and in **Fig.7** is recommended.

- 1) connect **Rsen1** between **Vc1** and **Vsense** to apply 1.5V or more to Vsense terminal, and
- 2) connect **Rtimer1** between **TIMER** and **SGND** to disable F/B loop open protection.

Please note this circuit is for investigation only. Do not switch on/off the **Vbulk** when using **Rsen1** as 1) to protect MOSFETs from undesired heavy switching stress especially in mid-heavy load condition.

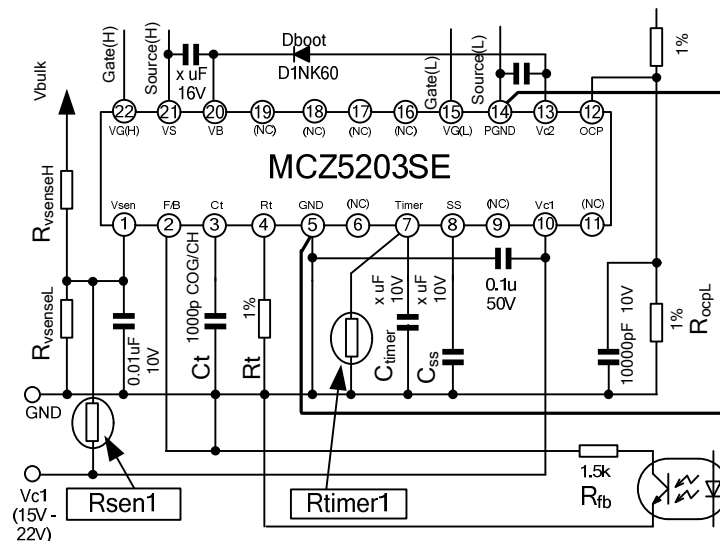


Fig.7 additional components

Selecting the Components of Peripheral Circuit

3.1 Oscillator (selecting Rt)

The timing of gate drive pulse **VG(L)** and **VG(H)** is determined by charging and discharging time of timing capacitor **Ct**. **VG(L)** and **VG(H)** drive main switches alternately and shoot through current of main switches is prohibited by dead time (**DT**) that is equal to discharging time of **Ct** +140ns as shown in **Fig.8**. The IC adopts non-constant dead time architecture, and the frequency and ON-duty varies according to F/B terminal current and frequency increases respectively as shown in **Fig.9**. Larger dead time in light load condition secures ZVS over a wide frequency range. Minimum frequency (**fmin**) is determined by **Ct** and **Rt**. Less than 300kHz for **fmax** is recommended in continuous operation considering power consumption.

fss depends on **Ct**,
for example 185kHz with **Ct**=1000pF typically
See characteristic diagram sheet for detail.

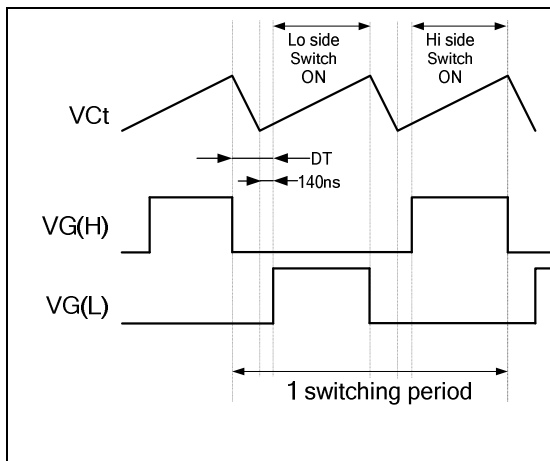


Fig.8 Gate drive pulse timing diagram

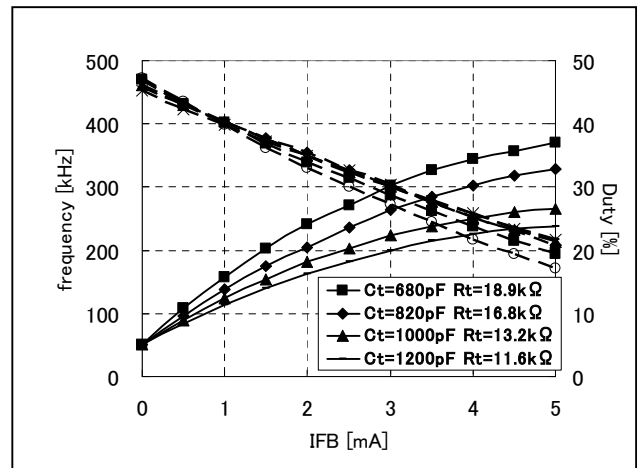


Fig.9 frequency/duty vs I(F/B)

The value of tentative **Rt**, **Rt(init)**, will be obtained from formula(1) using **fmin** and **Ct** value.

Approximate value of **fmin** will be obtained from formula(2) using actual value of **Rt**. (**Ct**=680pF, **Rt**=18.9kohm)

Refer to characteristic curves to confirm **Ct/Rt** condition.

$$R_{t(init)} = \left(\frac{1}{2 \times f_{min}} - \frac{C_t \times 1.88}{4.2 \times 10^{-3}} \right) \times \frac{2.52}{C_t \times 1.88} \quad [\text{ohm}] \quad \text{---(1)}$$

$$f_{min} = \frac{1}{2 \times \left(\frac{1.88 \times C_t \times R_t}{2.52} + \frac{C_t \times 1.88}{4.2 \times 10^{-3} - 2.52 / R_t} \right)} \quad [\text{Hz}] \quad \text{---(2)}$$

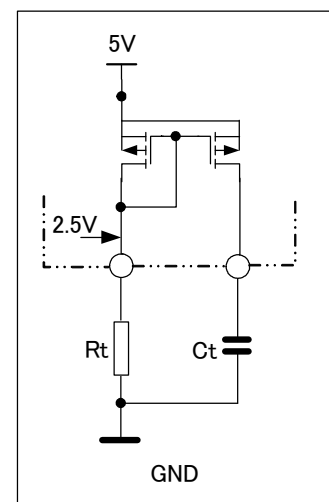


Fig.10 Ct / Rt internal block

3.2 Brown-out protection (selecting RvsenseL)

Vsense terminal monitors the input voltage for halting gate drive pulse and varying the frequency. UVLO function avoids below-resonant state caused by supplying **Vbulk** remaining Vc1 is applied, brown-out (quick decrease of input voltage) or black-out (instantaneous interruption). Timing diagram of brown-out protection is shown in **Fig.12**. High side resistor of voltage divider is **RvsenseH** :greater than 3Mohm is recommended. Required minimum sink current of Vsense terminal is 1uA. Low side resistor, **RvsenseL**(init) is obtained from formula(3) and correct value of **Vbulkreset** threshold is obtained from formula(4) by using actual value of **RvsenseL**. This 1.4V threshold is for **Css** resetting without hysteresis, and 1.1V is for ON/OFF with 0.4V hysteresis. Vsense pin can be simply used for ON/OFF function.

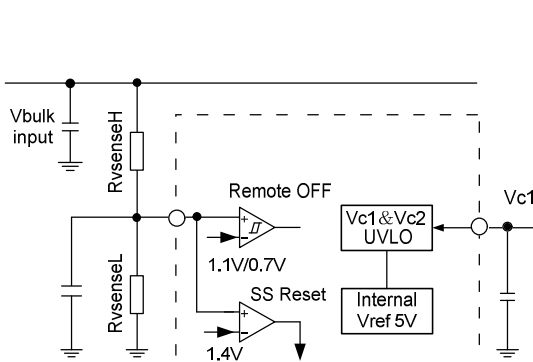


Fig.11 Vsense internal block

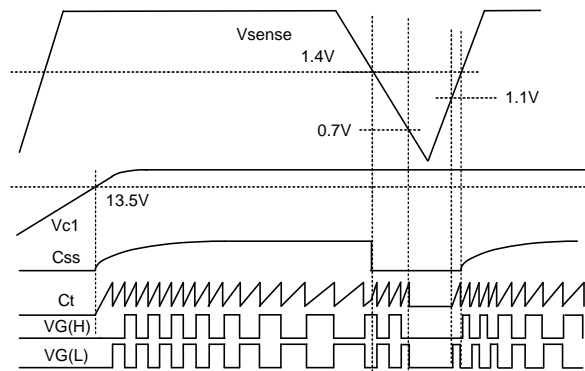


Fig.12 Vsense brown out timing diagram

$$R_{vsenseL (init)} = \frac{1.4 \times R_{vsenseH}}{V_{bulkreset} - 1.4} \quad [\text{ohm}] \quad \text{---(3)}$$

$$V_{bulkreset} = \frac{R_{vsenseH} + R_{vsenseL}}{R_{vsenseL}} \times 1.4 \quad [\text{Vdc}] \quad \text{---(4)}$$

RvsenseH of 3Mohm as an example consumes 40mW constantly at AC240V (without PFC operating). In the case where PFC converter with independent OVP function is installed, the voltage divider (associated power consumption) can be eliminated by obtaining **Vsense** voltage from OVP detector of the PFC converter. Connect filtering capacitor of around 3.3-10nF between Vsense terminal and GND.

3.3 Soft start (selecting Ccss)

Tentative value of soft start timing capacitor **Ccss**(init) is obtained from approximate formula(5). **tss** is the time period of which the frequency stabilizes at fmin after VCcss reaches around 0.8V. Correct value of tss, soft start time period, is obtained from formula(6) using actual value of Ccss. Characteristics of **Ccss** voltage vs operating frequency at **Ccss** = 4.7uF (**tss** = 200ms) is shown in Fig.13.

$$C_{ss(init)} = t_{ss} \times 23 \times 10^{-6} \quad [\text{F}] \quad \text{---(5)}$$

$$t_{ss} = \frac{C_{ss}}{23 \times 10^{-6}} \quad [\text{sec}] \quad \text{---(6)}$$

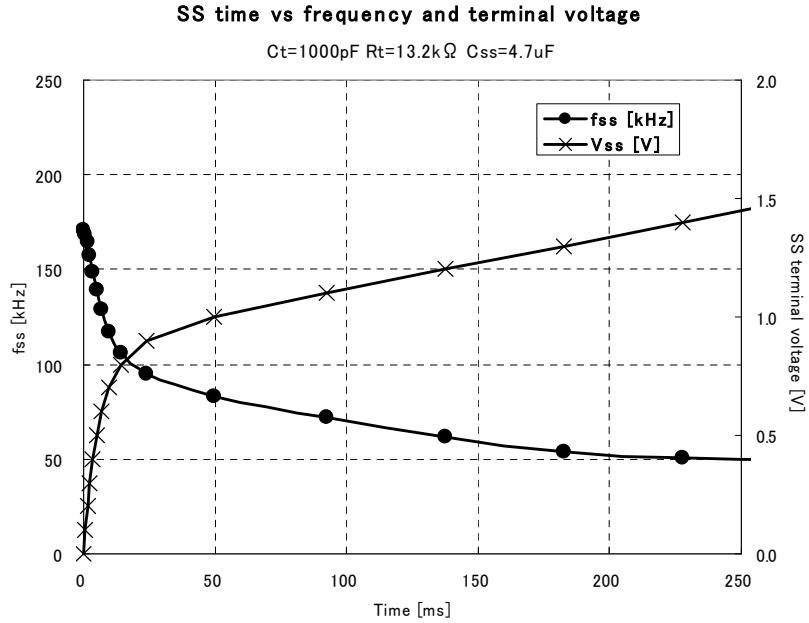


Fig.13. fss characteristics

3.4 Over-current Protection (selecting Rocpdet / RocpL)

OCP (over current protection) operates by detecting positive peak current of resonant tank (drain current of high-side MOSFET) beyond the threshold of +0.345V. The current is detected by sensing resistor **Rocpdet** and its detected voltage is applied to OCP terminal through R/C filter. When the voltage applied to OCP terminal reaches +0.345V, timing capacitor **Ct** is charged rapidly and consequently the frequency is increased to limit the current / MOSFET drain current. Threshold level is low enough to minimize ineffective power loss of sensing resistor. Filter capacitor is connected between OCP and SGND to eliminate the influence of parasitic inductance of sensing resistor or parasitic inductance. The capacitance value of 1000pF to 10000pF is recommended.

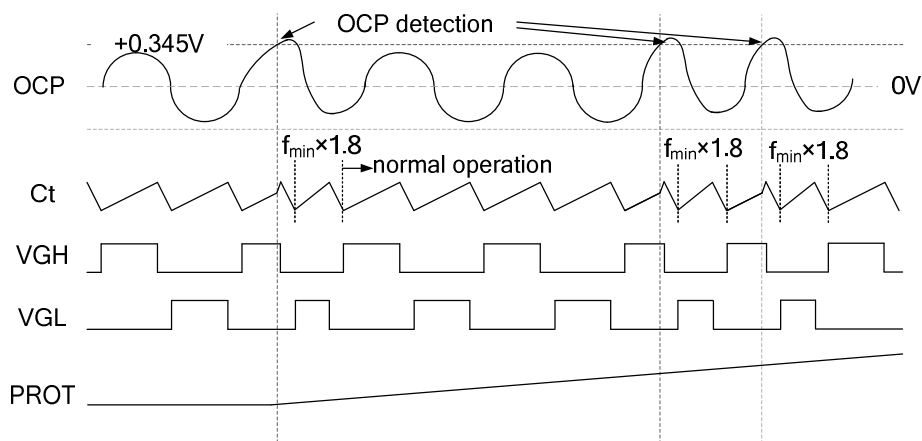


Fig.14. OCP Timing diagram

Rocpdet is obtained from formula(7) with desired OCP threshold **Ip_{pk}**. Tentative value of **RocpL_(init)** is obtained from formula(8) and correct value of **Ip_{pk(th)}** is calculated from formula(9) using actual value of **RocpL**.

10-47 ohm is recommended as **RocpH** considering OCP terminal sourcing current (180uA typ.). **Ip_{pk(th)}** value should be determined carefully to have enough margins in low input voltage / Pomax or switching load condition.

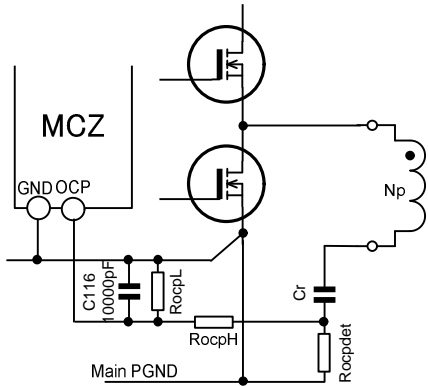


Fig.15. Main resonant current detecting configuration

$$R_{ocp\ det} > \frac{0.345}{I_{pk}} \quad [ohm] \text{-----(7)}$$

$$R_{ocpL\ (init)} = \frac{0.345 \times 10}{I_{pk} \times R_{ocp\ det} - 0.345} \quad [ohm] \text{-----(8)}$$

$$I_{pk\ (th)} = \frac{10 + R_{ocpL}}{R_{ocpL} \times R_{ocp\ det}} \times 0.345 \quad [A] \text{-----(9)}$$

OCP function of MCZ5203 activates by detecting positive current (drain current of high-side MOSFET) so keep suitable winding direction if half-wave rectification is applied in multiple output converter usage.

If OCP activates (in the period of high-side driven), succeeding period of low-side driven is limited to 1/ (2 x fmin x 1.8).

Large negative voltage applied to OCP terminal may cause OCP malfunction. If OCP terminal negative voltage is greater than -0.8V , add 40V 1A SBD to clamp the negative voltage.

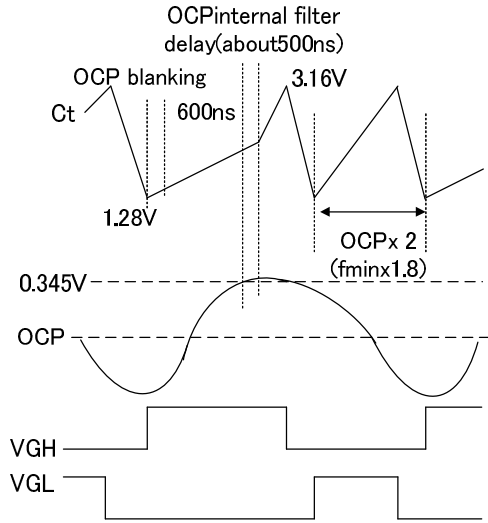


Fig.16. OCP protection

3.5 di/dt mode protection

MCZ5203 adopts pulse by pulse bidirectional didt protection to avoid below resonant mode operation. This function helps to avoid hard switching of main switches in below ZVS boundary operation.

When OCP terminal voltage (**Vocp**) exceeds 60mV during the period of **Ct** voltage going bottom to 2.1V (**Ct** masking period), didt protection is ready to activate. In identical **Ct** saw tooth period, **Vocp** decreasing to 60mV again results in instantaneous **Ct** discharging and gate drive turns off. In negative current direction, threshold voltage is -60mV. During didt protection is operating , **CTimer** is not charged.

Please note didt threshold is about 1/6 of OCP threshold.

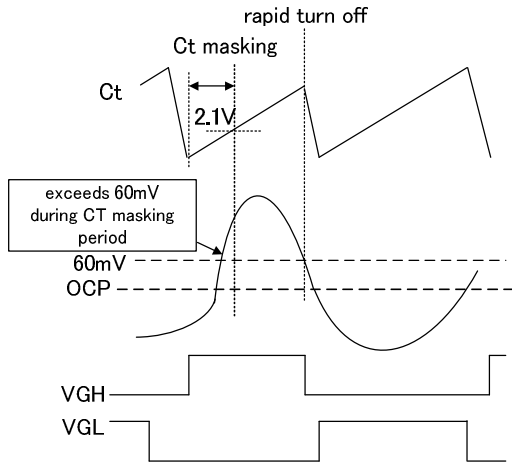


Fig.17. di/dt protection

3.6 Timer Protection (selecting C_{Timer})

TIMER terminal has 2 threshold, 3V and 0.3V. When OCP or F/B loop open protection operates, **CTimer** charging starts and continuous abnormal condition keeps charging **CTimer** with constant 215uA until **V(CTimer)** reaches 3.0V. Once **V(CTimer)** reached 3V, gate output stops and **CTimer** discharging with constant 10uA sinking starts and continues until **V(CTimer)** decreases to 0.3V. At the moment **V(CTimer)** reaches 0.3V, **CTimer** 215uA charging restarts and Gate output also restarts with soft starting function. TIMER counter counts the number of times of 3V charging. If count is twice, output will be latched off. When abnormal condition is eliminated and converter enters in normal operation before abnormal 2 counts, **CTIMER** is rapidly discharged with 2mA sinking and the counting result is reset.

To release latching , restart with supplying Vc1 of less than 8V

Timing chart is shown in **Fig.18**.

$$CTIMER = \frac{tTIMER \times 215}{3} \times 10^{-6} \text{ [F]} \quad \text{---(10)}$$

TIMER burst timing ratio is **tTimer1 : tb = 1 : (20+tss)**,
 In case of **CTimer=4.7uF / C_{ss}=2.2uF, tTimer=70msec , tb=1.5sec.**

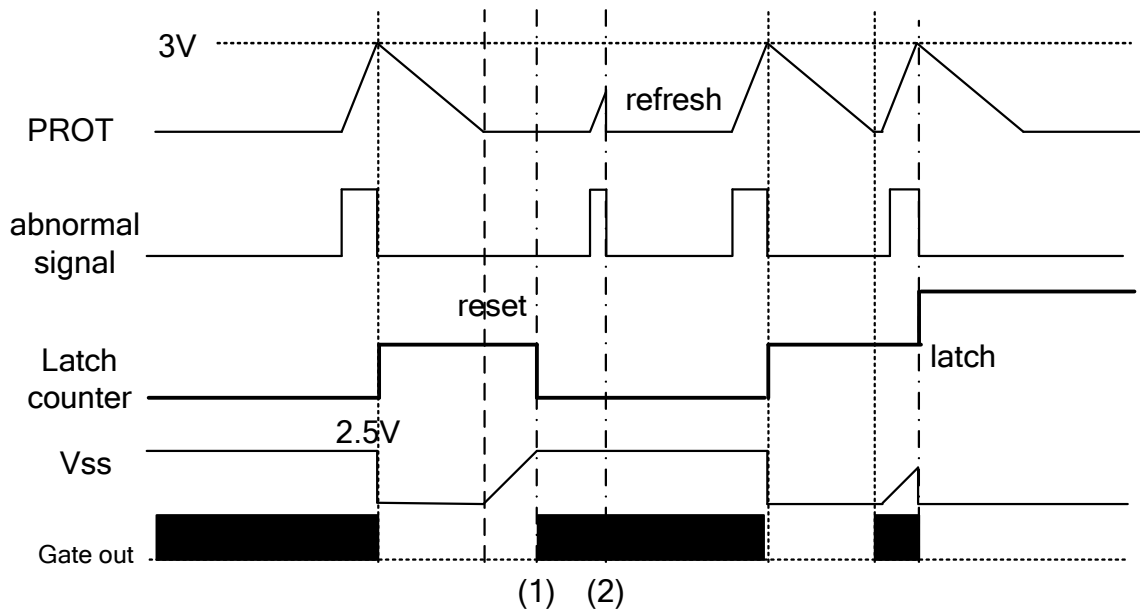


Fig.18. Timer delayed burst and latching timing chart

3.7 High side floating Vcc (VB)

Floating High side gate drive voltage source (**VB**) is produced by bootstrapping configuration from stabilized **Vc2** 10V. 600V soft recovery type UFRD (ultra fast recovery diode) is recommended like D1NK60 (Shindengen). $VB = Vc2 - Vf$ (Dboot)

VS terminal is the reference potential for **VB**, so if negative spike voltage due to turn off current of low side switch and pattern parasitic inductance is too large, **VB** will be over charged. In case of **VB** max exceeds 15V , zener diode clamping is recommended to avoid high side logic malfunction.

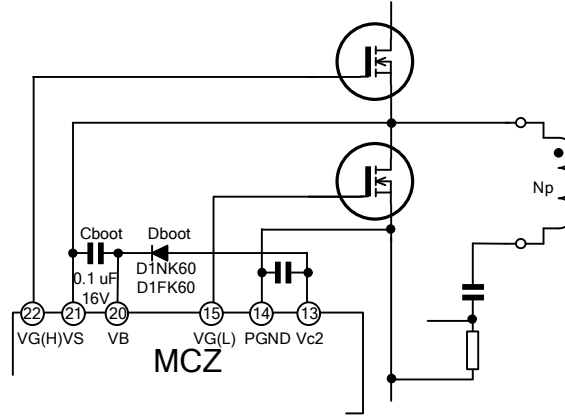


Fig.19. Boot Strapping configuration

3.8 Gate driver

The gate drivers have 0.18A sourcing and 0.53A sinking current capability at **Vc2=10V**. Typical configurations are shown in Fig.20a) b). If using small low Qg MOSFET like 30nC or less, R122/125 and D112/113 will not be required like Fig.20 C) due to optimized unbalanced drive capability of MCZ5203.

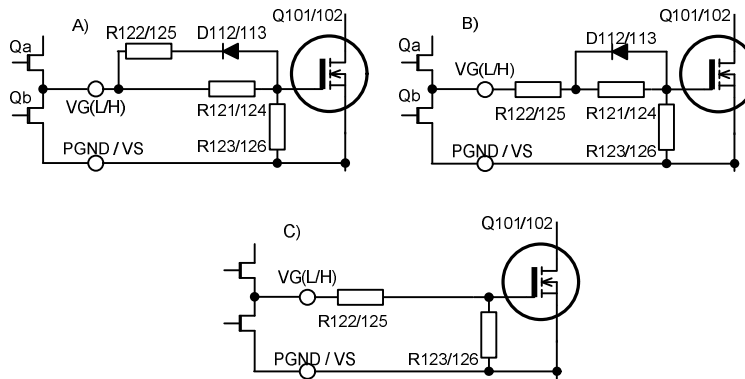


Fig.20. Gate driving configuration

4 Circuit diagram

4.1 circuit example

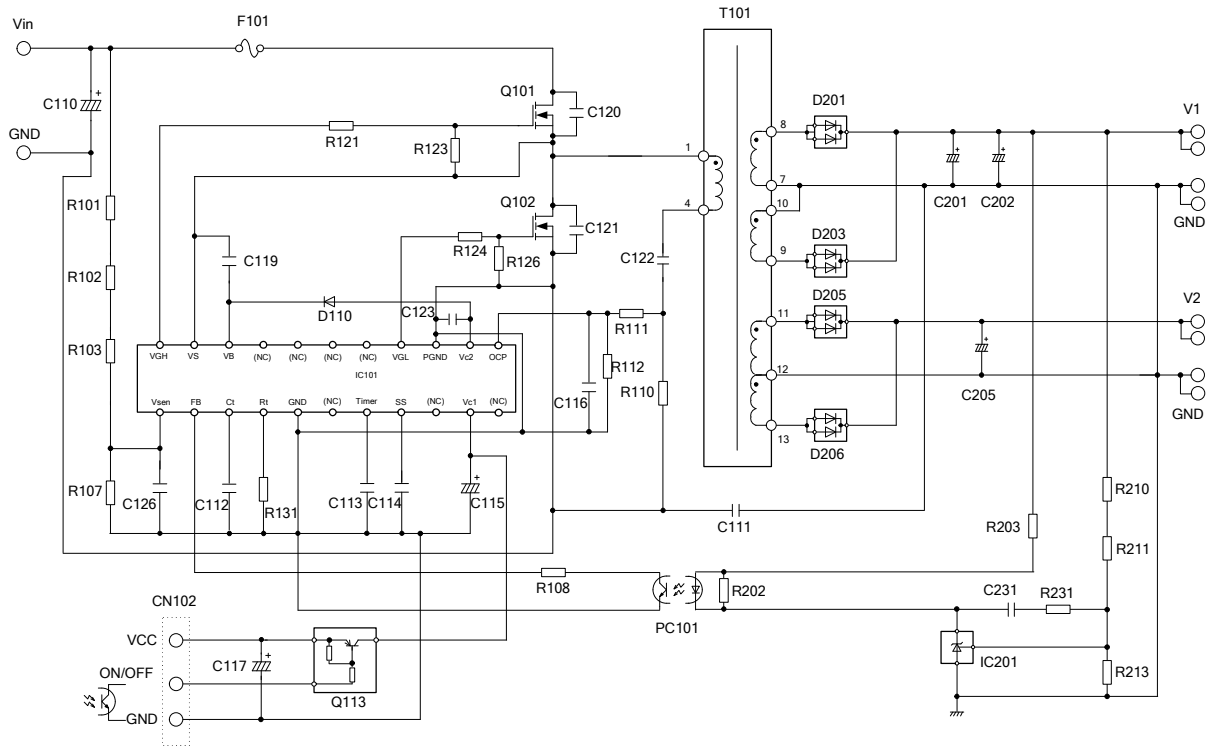
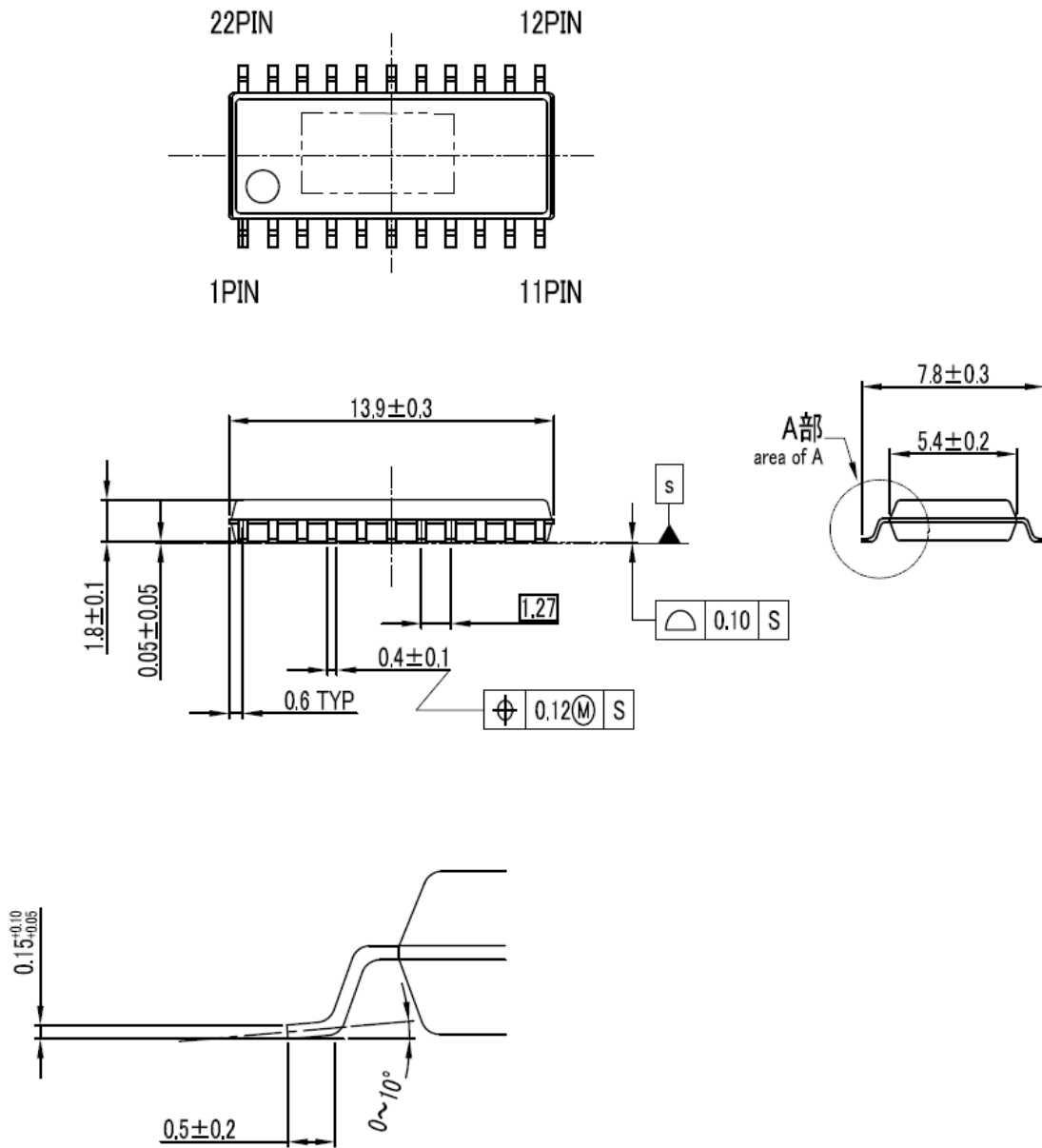


Fig.21. dual output LLC

5 Dimensions

5.1 SOP22 (MCZ5203SE)



A部詳細図
Detail area of A

Units : mm