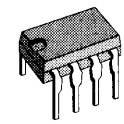
SGS-THOMSON MICROELECTRONICS

M8716B

CLOCK/CALENDAR WITH SERIAL I^2C BUS

- CLOCK/CALENDAR WITH SERIAL I^2C BUS
- 32kHZ QUARTZ TIMEBASE
- COUNTERS FOR SEC ; MIN ; HRS ; DAY ; MONTH OR SEC ; MIN ; HRS ; DAY OF WEEK
- EXTREMELY LOW POWER CONSUMPTION IN STANDBY OPERATION (Typ. 5µA)
- 8 PIN DIP PACKAGE
- INTEGRATED POWER FAIL DETECTION AND POWER-ON RESET
- PULSE OUTPUT FOR SECONDS
- CMOS PROCESS



DIP8
(Plastic Package)

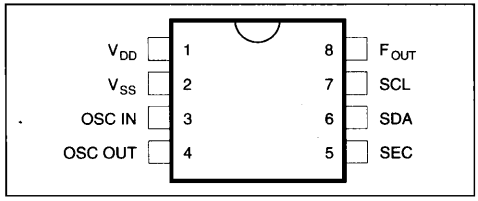
ORDER CODE : M8716AB1

DESCRIPTION

The integrated circuit M8716B contains a digital clock with a 32kHz quartz oscillator and a serial bus interface (I^2C Bus). The circuit is programmable to count seconds, minutes, hours, days and month or seconds, minutes, hours and day of the week.
This circuit is intended for use within a microcomputer system.

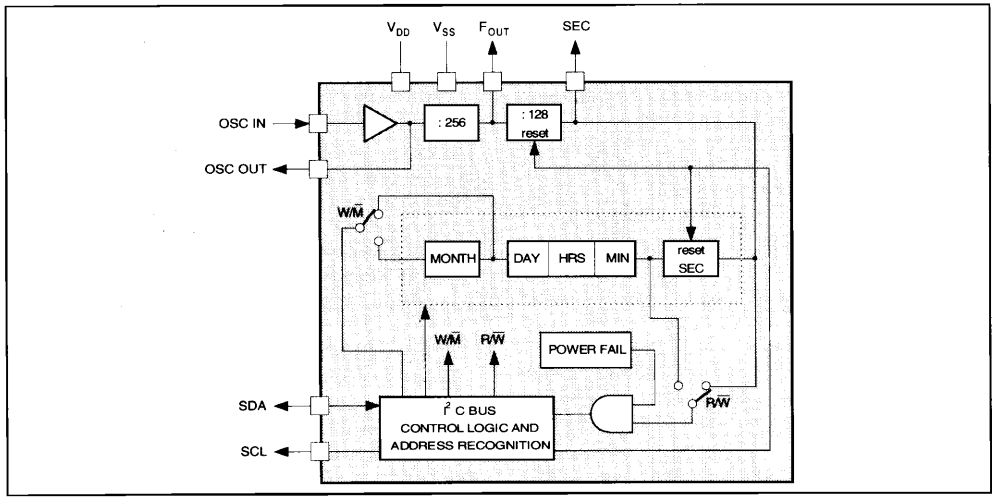
The M8716B is available in a 8 lead dual in-line plas-tic package.

PIN CONNECTIONS



8716B-01.EPS

BLOCK DIAGRAM



87168-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}-V_{SS}	Supply Voltage	– 0.3 to + 10	V
V_I/V_O	Input Voltage, Output Voltage	V_{SS} – 0.3 to V_{DD} + 0.3	V
P_D	Total Package Power Dissipation	300	mW
T_{stg}	Storage Temperature	– 55, + 125	°C
T_A	Operating Temperature	0, + 70	°C

87168-01.TBL

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C : V_{DD} = 5V ; F_{OSC} = 32.768kHz if not otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
I_{DD}	Supply Current				1	mA
V_{BAT}	Supply Voltage (standby operation)	No Data Transfer	2.0	2.4		V
I_{BAT}	Supply Current (standby operation)	Test Circuit, V_{BAT} = 2.4V		5	15	µA
I_{IN}	Input Current SDA ; SCL	$V_{IN} = V_{DD}$ $V_{IN} = V_{SS}$			5 –5	µA µA
I_{OUT}	Output Current SDA	V_{OL} = 0.4V	4			mA
I_{OUT}	Output Current F_{OUT}, SEC	V_{OUT} = 1V V_{OUT} = 4V	0.1 -0.1			mA mA
C_{OUT}	Oscillator Output-capacitance		16	20	24	pF

87168-02.TBL

GENERAL DESCRIPTION

The integrated circuit M8716B contains a digital clock counting seconds, minutes, hours, days and months or seconds, minutes, hours and days of the week as an option. A 32.768kHz quartz oscillator serves as time-base. This circuit is intended for use within a microcomputer system.

Writing (time setting) and reading of the counters is done via a serial interface (I^2C Bus). The microcomputer is used for controlling the data transfer and for generating the signals to drive a (7 segment) display. If a data transfer takes place between the M8716B and the microprocessor, a 5V supply voltage has to be provided. During standby the circuit is supplied by two NiCd-cells at a very low power consumption.

FUNCTIONAL DESCRIPTION

Dividers and Counters

The oscillator frequency of 32.768kHz is first divided by 256 and then again by 128. The resulting output frequency of 1Hz then serves as clock pulse for the time counters.

The content of the counters for sec, min, hr, day and month of sec, min, hr, and day of week can be read or modified (written) via the I^2C Bus interface. During a "write" cycle only the content of the counters starting from the minutes counter is modified : the seconds counter and the seconds divider block are reset to zero.

Selection between "calendar" operation (display of day and month) and "day of week" operation (display of day of week 1 to 7) is done as follows :

If the second bit in the first data byte is "1" during a "write" operation, the counters are set for the mode "day of week".

If this bit remains at "0" during a "write" operation the calendar mode is selected. In this case, carry of the "day" counter is performed automatically at positions 28, 30 or 31, depending on the month. In case of a leap year the day 29 (of February) can be set by a "write" operation.

In this case, carry takes place on 3-1 (March 1st).

I^2C Bus Interface General Description

Data transfer from the circuit M8716B to the microcomputer (reading) and vice versa (writing) takes place via the two lines SDA and SCL. Address and data are transmitted on SDA while at the same time clock pulses have to be provided on SCL for synchronization by the microcomputer.

I²C Bus Interface Addressing (see Fig. 1, 2, 3)

A data transfer (reading or writing) is initiated by a start condition ("1" – > "0" transition on SDA while SCL remains at "1") and a subsequent address byte. By assigning a unique address to each circuit, several circuits may be connected to the I²C Bus without interfering each other.

If the M8716B recognizes an address transmitted on the bus as its own address, the data transfer starts. The least significant bit of the address word controls the direction of data transfer (R/W-control). If it is set to "0", data is transferred from the microcomputer to the circuit, i.e. the content of the time counters is modified. If it is set to "1" the time information is read out by the microcomputer. A data transmission between the microprocessor and M8716B must always be completed otherwise the clock content may be lost. This means that the "master" can't use the possibility to stop the transmission after a certain byte by not sending the acknowledge bit.

Even 2f M8716B can work at the frequency four DC UP to 100kHz, it is tested at a frequency of 30kHz. If a carry of the time counter should take place during a data transfer, the carry will be stored and made after the data transfer. As only one carry can be stored, the whole data transfer must not take a time longer than one second.

Synchronization

For easy of synchronization with an external time reference in case of small deviations (< ± 30sec), only the address (with R/W = "0") has to be transmitted, followed immediately by a stop condition. No data is transmitted (see fig. 4). The second divider block (128Hz to 1Hz) and the seconds counter are reset. If the seconds counter was at position 30 ... 59, a carry to the minutes counter takes place in addition to the reset.

Figure 1 : Complete Timing for an Address/-read ; Resp. Address/-write Cycle

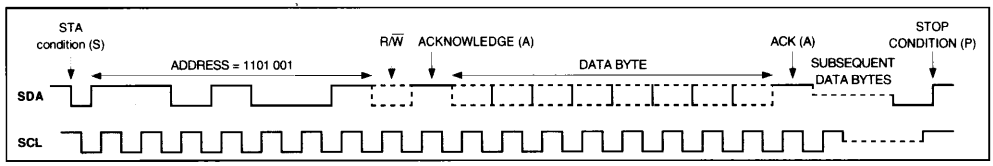


Figure 2a : Data Format for One Cycle Address/-read (with calendar)

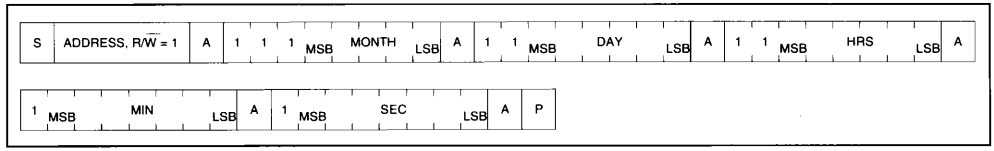


Figure 2b : Data Format for One Cycle Address/-write (with calendar)

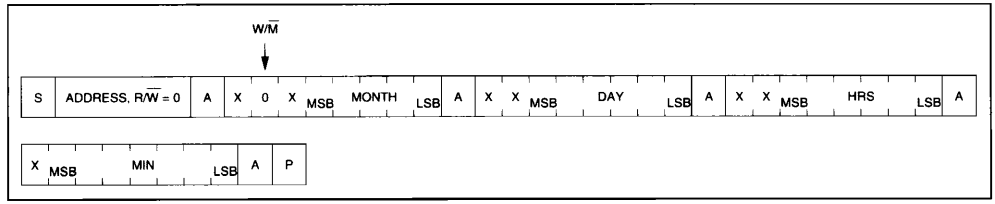


Figure 3a : Data Format for One Cycle Address/-read (with day of week indication)

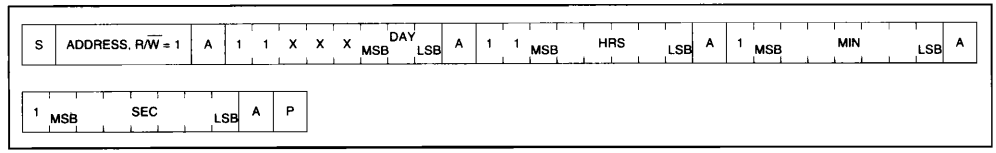


Figure 3b : Data Format for One Cycle Address/-write (with day of week indication)

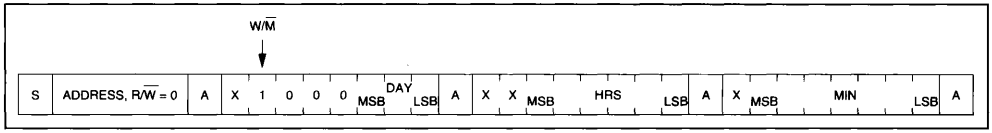
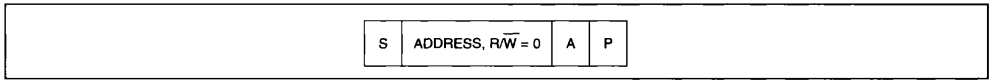


Figure 4 : Data Format for Synchronization (deviation < 30sec)



Power Fail

In case of total power fail an internal register is set to "0". This register disables the data of the watch. So in a read cycle the µP recognizes "0" of the watch content. This is a unique situation appearing only in case of a power fail. The power fail register is automatically reset by the first "write" command.

Pulse Outputs F_{OUT}, SEC

The output frequency of the first divider block (128Hz) is provided on the pin F_{OUT} and facilitates adjustment of the oscillator frequency without loading (and detuning) the oscillator.

The output SEC (1Hz) may be utilized for a blinking second indication.

Both pins F_{OUT} and SEC can also be used as input during the functional test. A Low impedance (50 to 100Ω) external signal source which overrides the internal output buffer can drive the circuit at a frequency higher than the normal rate. This allows to reduce test time.

Figure 5 : Test Circuit

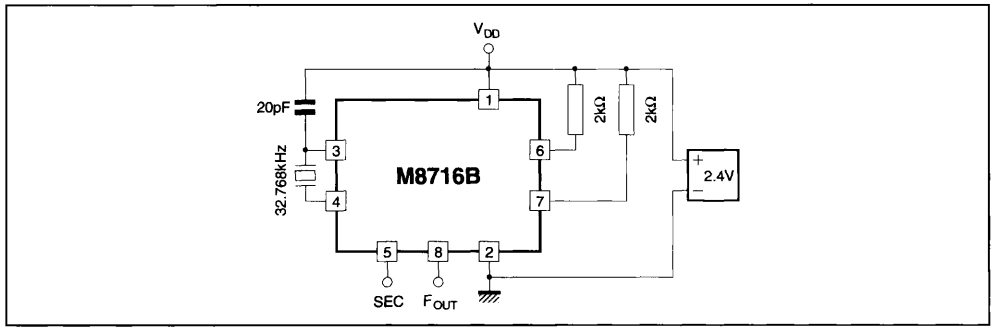


Figure 6 : Typical Application