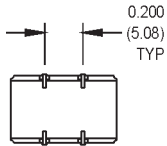
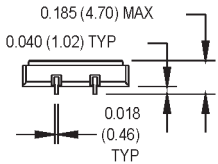
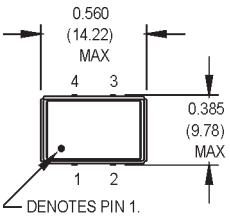


# M3V Series

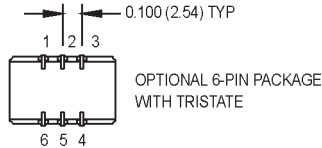
## 9x14 mm, 3.3 Volt, HCMOS/TTL, VCXO



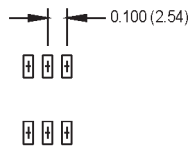
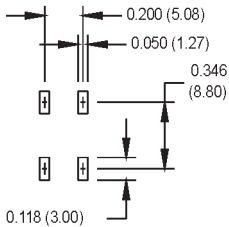
- HCMOS/TTL output to 160 MHz and excellent jitter (2.1 ps typ.) in a SMT package
- Phase-Locked Loops (PLL's), Clock Recovery, Reference Signal Tracking, Synthesizers, Frequency Modulation/Demodulation



All dimensions in inches (mm).



### SUGGESTED SOLDER PAD LAYOUT



### Ordering Information

	M3V	1	3	V	2	C	J	00.0000 MHz
Product Series								
Temperature Range								
1: 0°C to +70°C								
2: -40°C to +85°C								
6: -20°C to +70°C								
Stability								
1: ±1000 ppm								
2: ±500 ppm								
3: ±100 ppm								
4: ±50 ppm								
5: ±35 ppm								
6: ±25 ppm								
*8: ±20 ppm								
Output Type								
V: Voltage Controlled								
T: Tri-state								
Pull Range (Vc = 0.3 to 3.0 V)**								
1: ±50 ppm min.								
2: ±80 ppm min.								
Symmetry/Logic Compatibility								
A: 40/60 CMOS/TTL								
C: 45/55 CMOS								
Package/Lead Configurations								
J: J Lead								
Frequency (customer specified)								

\*Contact factory for availability.

\*\*Other pull ranges available. Contact factory.

### APR Equivalents

APR	Pull Range	Stability
±25 ppm	±50 ppm	±25 ppm
±50 ppm	±80 ppm	±25 ppm

### Pin Connections

FUNCTION	4 Pin Pkg.	6 Pin Pkg.
Control Voltage	1	1
Tri-State		2
Circuit/Case Ground	2	3
Output	3	4
N/C		5
+Vdd	4	6

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# M3V Series

## 9x14 mm, 3.3 Volt, HCMOS/TTL, VCXO



Electrical Specifications	PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition
	Frequency Range <sup>1</sup>	F	1.544		160	MHz	
	Frequency Stability	ΔF/F	(See Ordering Information)				
	Operating Temperature	T <sub>A</sub>	(See Ordering Information)				
	Storage Temperature	T <sub>s</sub>	-55		+125	°C	
	Input Voltage	V <sub>cc</sub>	3.135	3.3	3.465	V	
	Input Current	I <sub>dd</sub>					
	1.544 to 24.000 MHz				20	mA	
	24.000 to 96.000 MHz				55	mA	
	96.000 to 155.520 MHz				65	mA	
	Symmetry (Duty Cycle) <sup>2</sup>		(See Ordering Information)				
	Load <sup>3</sup>		10 TTL or 50 pF				1.544 to 60.000 MHz
			5 TTL or 30 pF				60.001 to 160.000 MHz
	Rise/Fall Time <sup>4</sup>	Tr/Tf		3	10	ns	
	Logic “1” Level	Voh	90% Vdd			V	HCMOS load
			Vdd -0.5			V	TTL load
	Logic “0” Level	Vol			10% Vdd	V	HCMOS load
					0.5	V	TTL load
	Cycle to Cycle Jitter						1 Sigma
	@ 38.88 MHz			5.5	7	ps RMS	
@ 77.76 MHz			10	15	ps RMS		
@ 155.52 MHz			10	15	ps RMS		
Phase Jitter	ϕ J					Integrated 12 kHz - 20 MHz	
@ 38.88 MHz			.3	.5	ps RMS		
@ 77.76 MHz			3	5	ps RMS		
@ 155.52 MHz			3	5	ps RMS		
Peak to Peak Jitter (+/-)	Tj					@ BER 1E-12	
@ 38.88 MHz			2.1	3.5	ps RMS		
@ 77.76 MHz			21	35	ps RMS		
@ 155.52 MHz			21	35	ps RMS		
Phase Noise (Typical)	10Hz	100 Hz	1 kHz	10 kHz	100 kHz	Offset from carrier	
@ 38.88 MHz	-68	-100	-130	-145	-155		
@ 77.76 MHz	-60	-90	-112	-128	-125		
@ 155.52 MHz	-60	-90	-112	-123	-120		
Modulation Bandwidth	f <sub>m</sub>			10	kHz		
Input Impedance (Pin 1)	Z <sub>in</sub>	50			KΩ		
Control Voltage	V <sub>c</sub>	0.3		3.0	V		
Center Frequency	V <sub>c0</sub>	1.65			V		
Pullability		(See Ordering Information)				Over control voltage	
Linearity				10	%		
Tri-State Function		Input Logic “1” or floating; output active					
		Input Logic “0”; output to High-Z					
Environmental	Mechanical Shock	Per MIL-STD-202, Method 213, Condition C					
	Vibration	Per MIL-STD-202, Method 201 & 204					
	Reflow Solder Conditions	See “Figure 2” on page 147					
	Hermeticity	Per MIL-STD-202, Method 112 (1 x 10 <sup>-3</sup> atm.cc/s of helium)					
	Solderability	Per EIAJ-STD-002					

1. Frequencies above 70 MHz utilize a PLL design. Fundamental and PLL designs are available at other frequencies. Contact factory.
2. Symmetry is measured at 1.4 V with TTL load, and at 50% V<sub>dd</sub> with HCMOS load.
3. TTL load - see load circuit diagram #1 on page 148. HCMOS load - see load circuit diagram #2 on page 148.
4. Rise/Fall times are measured between 0.5 V and 2.4 V with TTL load, and between 10% V<sub>dd</sub> and 90% V<sub>dd</sub> with HCMOS load.

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