

**3.3V 32M x 64/72-Bit SDRAM Modules**  
**3.3V 64M x 64/72-Bit SDRAM Modules**

**HYS64/72V32200GU**  
**HYS64/72V64220GU**

## PC100-168 pin unbuffered DIMM Modules

- 168 Pin unbuffered 8 Byte Dual-In-Line SDRAM Modules for PC main memory applications
- One bank 32M x 64 and 32M x 72 organisation
- Two bank 64M x 64 and 64M x 72 organisation
- Optimized for byte-write non-parity or ECC applications
- Fully PC board layout compatible to INTEL's Rev. 1.0 module specification
- JEDEC standard Synchronous DRAMs (SDRAM)
- SDRAM Performance:

		-8	-8B	Units
f <sub>CK</sub>	Clock frequency (max.)	100	100	MHz
t <sub>AC</sub>	Clock access time	6	6	ns

- Programmed Latencies :

Product Speed		CL	tRCD	tRP
-8	PC100	2	2	2
-8B	PC100	3	2	3

- Single +3.3V(± 0.3V ) power supply
- Programmable  $\overline{CAS}$  Latency, Burst Length and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- Decoupling capacitors mounted on substrate
- All inputs, outputs are LVTTTL compatible
- Serial Presence Detect with E<sup>2</sup>PROM
- Uses SIEMENS 256Mbit SDRAM components in 32M x 8 organisation and TSOP11-54 packages
- Gold contact pad
- Card Size: 133,35 mm x 31.75 mm x 4,00 mm

The HYS64/72V32200 and HYS64/72V64220 are industry standard 168-pin 8-byte Dual in-line Memory Modules (DIMMs) which are organised as 32M x 64 and 32M x 72 in 1 bank and 64M x 64 and 64M x 72 in two banks high speed memory arrays designed with 256M Synchronous DRAMs (SDRAMs) for non-parity and ECC applications. The DIMMs use -8 and -8B speed sort for 32M x 8 SDRAM devices in TSOP54 packages to meet the PC100 requirement. Decoupling capacitors are mounted on the PC board. The PC board design is according to INTEL's PC 100 module specification.

The DIMMs have a serial presence detect, implemented with a serial E<sup>2</sup>PROM using the two pin I<sup>2</sup>C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user.

All SIEMENS 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133,35 mm long footprint, with 1,25" ( 31,75 mm) height.

### Ordering Information

Type	Code	Package	Descriptions	Module Height
HYS 64V32200GU-8	PC100-222-620	L-DIM-168-30	PC100 32M x 64 1 bank SDRAM module	1,25"
HYS 72V32200GU-8	PC100-222-620	L-DIM-168-30	PC100 32M x 72 1 bank SDRAM module	1,25"
HYS 64V64220GU-8	PC100-222-620	L-DIM-168-30	PC100 64M x 64 2 bank SDRAM module	1,25"
HYS 72V64220GU-8	PC100-222-620	L-DIM-168-30	PC100 64M x 72 2 bank SDRAM module	1,25"
HYS 64V32200GU-8B	PC100-323-620	L-DIM-168-30	PC100 32M x 64 1 bank SDRAM module	1,25"
HYS 72V32200GU-8B	PC100-323-620	L-DIM-168-30	PC100 32M x 72 1 bank SDRAM module	1,25"
HYS 64V64220GU-8B	PC100-323-620	L-DIM-168-30	PC100 64M x 64 2 bank SDRAM module	1,25"
HYS 72V64220GU-8B	PC100-323-620	L-DIM-168-30	PC100 64M x 72 2 bank SDRAM module	1,25"

### Pin Names

A0-A12	Address Inputs ( RA0 ~ RA12 / CA0 ~ CA9)		CLK0 - CLK3	Clock Input
BA0, BA1	Bank Selects		DQMB0 - DQMB7	Data Mask
DQ0 - DQ63	Data Input/Output		$\overline{CS}0 - \overline{CS}3$	Chip Select
CB0-CB7	Check Bits (x72 organisation only)		Vcc	Power (+3.3 Volt)
$\overline{RAS}$	Row Address Strobe		Vss	Ground
$\overline{CAS}$	Column Address Strobe		SCL	Clock for Presence Detect
$\overline{WE}$	Read / Write Input		SDA	Serial Data Out for Presence Detect
$\overline{CKE}0, \overline{CKE}1$	Clock Enable		N.C. / DU	No Connection

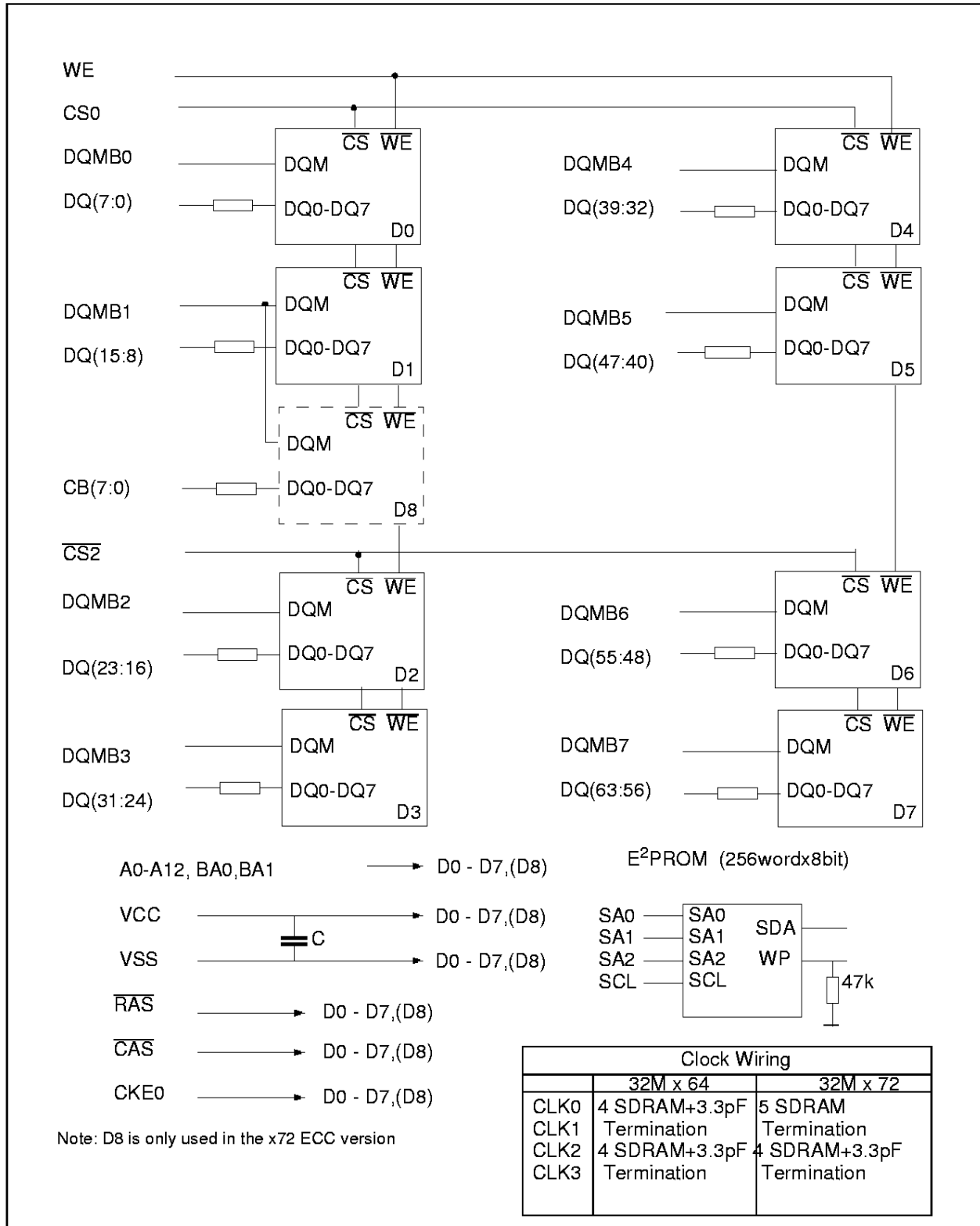
### Address Format:

	Part Number	Rows	Columns	Bank Select	Refresh	Period	Interval
32M x 64/72	HYS64/72V32200GU	13	10	2	8k	64 ms	7,8 $\mu$ s
64M x 64/72	HYS64/72V64220GU	13	10	2	8k	64 ms	7,8 $\mu$ s

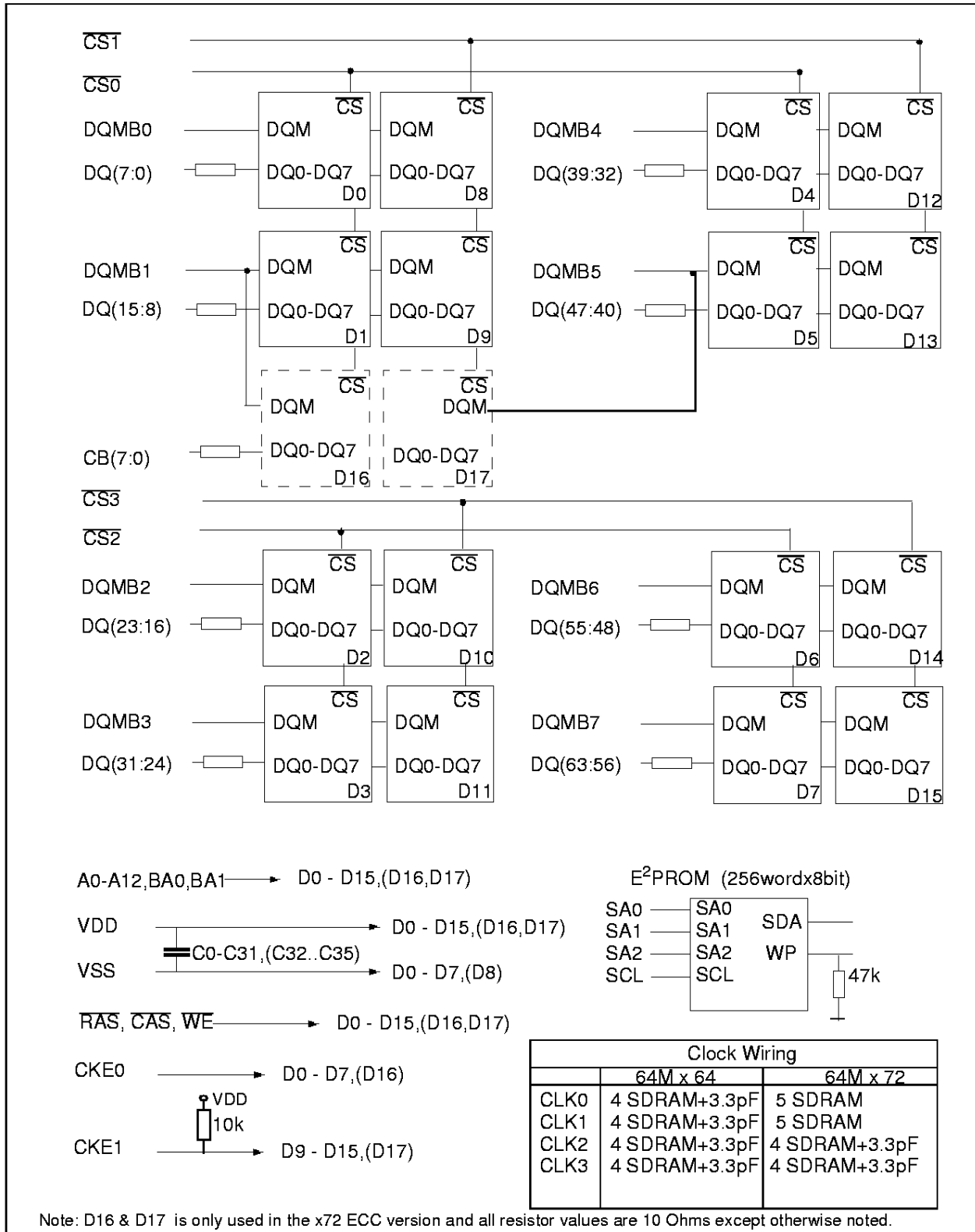
### Pin Configuration

PIN #	Symbol	PIN #	Symbol	PIN #	Symbol	PIN #	Symbol
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	CS2	87	DQ33	129	CS3
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	VCC	48	DU	90	VCC	132	NC
7	DQ4	49	VCC	91	DQ36	133	VCC
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC (CB2)	94	DQ39	136	CB6
11	DQ8	53	NC (CB3)	95	DQ40	137	CB7
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VCC	101	DQ45	143	VCC
18	VCC	60	DQ20	102	VCC	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	DU	104	DQ47	146	DU
21	NC (CB0)	63	CKE1	105	NC (CB4)	147	NC
22	NC (CB1)	64	VSS	106	NC (CB5)	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VCC	68	VSS	110	VCC	152	VSS
27	WE	69	DQ24	111	CAS	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	CS0	72	DQ27	114	CS1	156	DQ59
31	DU	73	VCC	115	RAS	157	VCC
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	VSS	120	A7	162	VSS
37	A8	79	CLK2	121	A9	163	CLK3
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	VCC	82	SDA	124	VCC	166	SA1
41	VCC	83	SCL	125	CLK1	167	SA2
42	CLK0	84	VCC	126	A12	168	VCC

Note : Pinnames in brackets are for the x72 ECC versions



Block Diagram for 32M x 64/72 one bank SDRAM DIMM modules



Block Diagram for 64M x 64/72 two bank SDRAM DIMM modules

**DC Characteristics**

$T_A = 0$  to  $70$  °C;  $V_{SS} = 0$  V;  $V_{DD}, V_{DDQ} = 3.3$  V  $\pm$  0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input high voltage	$V_{IH}$	2.0	$V_{CC}+0.3$	V
Input low voltage	$V_{IL}$	- 0.5	0.8	V
Output high voltage ( $I_{OUT} = - 2.0$ mA)	$V_{OH}$	2.4	-	V
Output low voltage ( $I_{OUT} = 2.0$ mA)	$V_{OL}$	-	0.4	V
Input leakage current, any input ( $0$ V < $V_{IN} < 3.6$ V, all other inputs = $0$ V)	$I_{I(L)}$	- 40	40	$\mu$ A
Output leakage current (DQ is disabled, $0$ V < $V_{OUT} < V_{CC}$ )	$I_{O(L)}$	- 40	40	$\mu$ A

**Capacitance**

$T_A = 0$  to  $70$  °C;  $V_{DD} = 3.3$  V  $\pm$  0.3 V,  $f = 1$  MHz

Parameter	Symbol	Limit Values				Unit
		max. 32Mx64	max. 32Mx72	max. 32Mx64	max. 32Mx72	
Input capacitance (A0 to A11, BA0, BA1, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ )	$C_{I1}$	45	55	80	90	pF
Input capacitance (CS0 -CS3, )	$C_{I2}$	20	25	30	35	pF
Input capacitance (CLK0 - CLK3)	$C_{ICL}$	22	38	22	38	pF
Input capacitance (CKE0, CKE1)	$C_{I3}$	22	38	50	55	pF
Input capacitance (DQMB0 - DQMB7)	$C_{I4}$	13	13	20	20	pF
Input / Output capacitance (DQ0-DQ63, CB0-CB7)	$C_{IO}$	13	12	20	20	pF
Input Capacitance (SCL, SA0-2)	$C_{sc}$	8	8	8	8	pF
Input/Output Capacitance	$C_{sd}$	10	10	10	10	pF

### Operating Currents per SDRAM ( $T_A = 0$ to $70^\circ\text{C}$ , $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$ 1)

(Recommended Operating Conditions unless otherwise noted)

Parameter & Test Condition	Symb.	-8/-8B	-10		Note	
		max.				
<b>OPERATING CURRENT</b>  trc=trcmin., tck=tckmin. Outputs open, Burst Length = 4, CL=3 All banks operated in random access, all banks operated in ping-pong manner to maximize gapless data access	ICC1  x4 x8 x16	210 210 210	165 165 165	mA mA mA	2	
<b>PRECHARGE STANDBY CURRENT in Power Down Mode</b>  $\overline{\text{CS}} = V_{IH}(\text{min.}), \text{CKE} \leq V_{il}(\text{max})$	tck = min.  ICC2P	2	2	mA	2	
<b>PRECHARGE STANDBY CURRENT in Non-Power Down Mode</b>  $\overline{\text{CS}} = V_{IH}(\text{min.}), \text{CKE} \geq V_{ih}(\text{min})$	tck = min.  ICC2N	19	16	mA	2	
<b>NO OPERATING CURRENT</b>  tck = min., $\overline{\text{CS}} = V_{IH}(\text{min})$ , active state ( max. 4 banks)	CKE $\geq V_{IH}(\text{min.})$	ICC3N	45	40	mA	2
	CKE $\leq V_{IL}(\text{max.})$	ICC3P	10	10	mA	2
<b>BURST OPERATING CURRENT</b> tck = min., Read command cycling	ICC4  x4 x8 x16	210 210 210	165 165 165	mA mA mA	2,3	
<b>AUTO REFRESH CURRENT</b> tck = min., Auto Refresh command cycling	ICC5	240	195	mA	2	
<b>SELF REFRESH CURRENT</b> Self Refresh Mode, CKE=0.2V	standard version ICC6	2.5	2.5	mA	2	

#### Notes:

1. All values are shown per one SDRAM component.
2. These parameters depend on the cycle rate. These values are measured at 100 MHz for -8 and at 66 MHz for -10 parts. Input signals are changed once during tck, excepts for ICC6 and for standby currents when tck=infinity.
3. These parameters are measured with continuous data stream during read access and all DQ toggling. CL=3 and BL=4 is assumed and the VDDQ current is excluded.

### AC Characteristics 1)2)

$T_A = 0$  to  $70$  °C;  $V_{SS} = 0$  V;  $V_{CC} = 3.3$  V  $\pm$  0.3 V,  $t_T = 1$  ns

Parameter	Symbol	Limit Values				Unit	Note
		-8 PC100-222		-8B PC100-323			
		min.	max.	min.	max.		

### Clock and Clock Enable

Clock Cycle Time $\overline{\text{CAS}}$ Latency = 3 $\overline{\text{CAS}}$ Latency = 2	$t_{CK}$	10	–	10	–	ns	
		10	–	12	–	ns	
System Frequency $\overline{\text{CAS}}$ Latency = 3 $\overline{\text{CAS}}$ Latency = 2	$f_{CK}$	–	100	–	100	MHz	
		–	100	–	83	MHz	
Clock Access Time $\overline{\text{CAS}}$ Latency = 3 $\overline{\text{CAS}}$ Latency = 2	$t_{AC}$	–	6	–	6	ns	3,4)
		–	6	–	7	ns	
Clock High Pulse Width	$t_{CH}$	3	–	3	–	ns	4)
Clock Low Pulse Width	$t_{CL}$	3	–	3	–	ns	4)
Input Setup time	$t_{CS}$	2	–	2	–	ns	5)
Input Hold Time	$t_{CH}$	1	–	1	–	ns	5)
CKE Setup Time (Power down mode)	$t_{CKSP}$	2	–	2	–	ns	6)
CKE Setup Time (Self Refresh Exit)	$t_{CKSR}$	10	–			ns	7)
Transition time (rise and fall)	$t_T$	1	–			ns	

### Common Parameters

RAS to $\overline{\text{CAS}}$ delay	$t_{RCD}$	20	–	20	–	ns	
Cycle Time	$t_{RC}$	70	–	70	–	ns	
Active Command Period	$t_{RAS}$	48	–	48	–	ns	
Precharge Time	$t_{RP}$	20	–	30	–	ns	
Bank to Bank Delay Time	$t_{RRD}$	16	–	20	–	ns	
$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ delay time (same bank)	$t_{CCD}$	1	–	1	–	CLK	

### Refresh Cycle

Self Refresh Exit Time	$t_{SREX}$	10	–	10	–	ns	9)
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Parameter	Symbol	Limit Values				Unit	Note
		-8 PC100-222		-8B PC100-323			
		min.	max.	min.	max.		
Refresh Period	$t_{REF}$	64	–	64	–	ms	6)
Refresh Intervall							
128Mbit SDRAM based modules		–	15,6	–	15,6	$\mu$ s	
256Mbit SDRAM based modules		–	7,8	–	7,8	$\mu$ s	

### Read Cycle

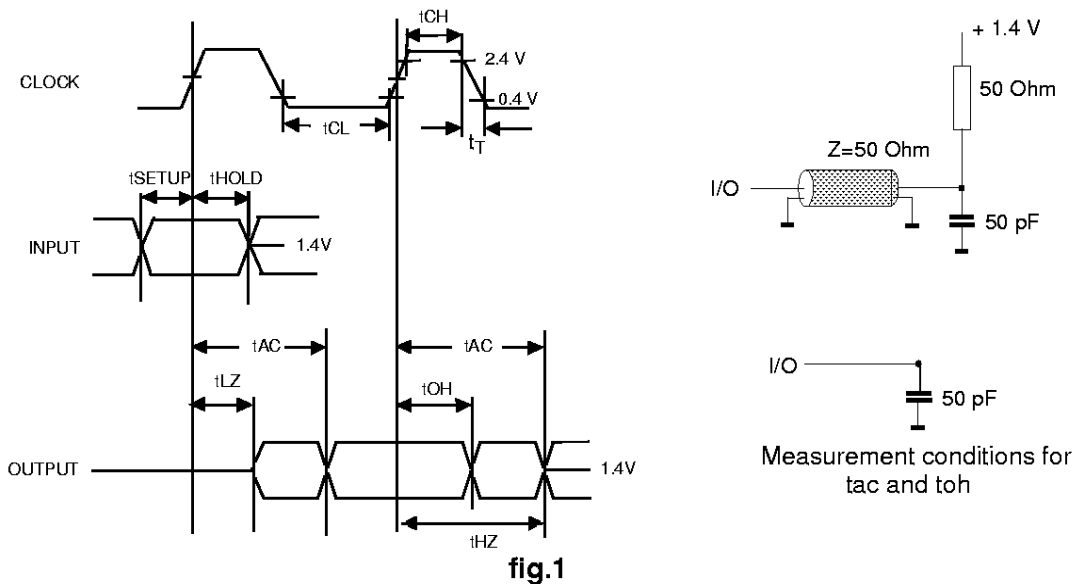
Data Out Hold Time	$t_{OH}$	3	–	3	–	ns	2)
Data Out to Low Impedance Time	$t_{LZ}$	0	–	0	–	ns	
Data Out to High Impedance Time	$t_{HZ}$	3	8	3	10	ns	8)
DQM Data Out Disable Latency	$t_{DQZ}$	–	2	–	2	CLK	

### Write Cycle

Data Input to Precharge (write recovery)	$t_{WR}$	2	–	2	–	CLK	
Data In to Active / Refresh	$t_{DAL}$	5	–	5	–	CLK	
DQM Write Mask Latency	$t_{DQW}$	0	–	0	–	CLK	

**Notes:**

1. An initial pause of 100µs is required after power-up, then a Precharge All Banks command must be given followed by 8 Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin.
2. AC timing tests have  $V_{il} = 0.4\text{ V}$  and  $V_{ih} = 2.4\text{ V}$  with the timing referenced to the 1.4 V crossover point. The transition time is measured between  $V_{ih}$  and  $V_{il}$ . All AC measurements assume  $t_T=1\text{ ns}$  with the AC output load circuit show. Specified  $t_{ac}$  and  $t_{oh}$  parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1V / ns edge rate between 0.8V and 2.0 V.



3. If clock rising time is longer than 1ns, a time  $(t_T/2 - 0.5)$  ns has to be added to this parameter.
4. Rated at 1.5 V
5. If  $t_T$  is longer than 1 ns, a time  $(t_T - 1)$  ns has to be added to this parameter.
6. Any time that the refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to “wake-up“ the device.
7. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to  $t_{RC}$  is satisfied once the Self Refresh Exit command is registered.
8. Referenced to the time which the output achieves the open circuit condition, not to output voltage levels.

A serial presence detect storage device - E<sup>2</sup>PROM - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E<sup>2</sup>PROM device during module production using a serial presence detect protocol ( I<sup>2</sup>C synchronous 2-wire bus).

### SPD-Table for 256MBit SDRAM based PC100 Modules:

Byte#	Description	SPD Entry Value	Hex			
			32Mx64 one bank -8	32Mx64 one bank -8B	32Mx72 one bank -8	32Mx72 one bank -8B
0	Number of SPD bytes	128	80	80	80	80
1	Total bytes in Serial PD	256	08	08	08	08
2	Memory Type	SDRAM	04	04	04	04
3	Number of Row Addresses (without BS bits)	13	0D	0D	0D	0D
4	Number of Column Addresses (for 32Mx8 SDRAMs)	10	0A	0A	0A	0A
5	Number of DIMM Banks	1	01	01	01	01
6	Module Data Width	64 / 72	40	40	48	48
7	Module Data Width (cont'd)	0	00	00	00	00
8	Module Interface Levels	LVTTL	01	01	01	01
9	SDRAM Cycle Time at CL=3	10.0 ns	A0	A0	A0	A0
10	SDRAM Access time from Clock at CL=3	6.0 ns	60	60	60	60
11	Dimm Config	none / ECC	00	00	02	02
12	Refresh Rate/Type	Self-Refresh, 7,8µs	82	82	82	82
13	SDRAM width, Primary	x8	08	08	08	08
14	Error Checking SDRAM data width	n/a / x8	00	00	08	08
15	Minimum clock delay for back- to-back random column address	t <sub>ccd</sub> = 1 CLK	01	01	01	01
16	Burst Length supported	1, 2, 4 & 8	0F	0F	0F	0F
17	Number of SDRAM banks	4	04	04	04	04
18	Supported CAS Latencies	CAS latency = 2 & 3	06	06	06	06
19	CS Latencies	CS latency = 0	01	01	01	01
20	WE Latencies	Write latency = 0	01	01	01	01
21	SDRAM DIMM module attributes	non buffered/non reg.	00	00	00	00
22	SDRAM Device Attributes :General	Vcc tol +/- 10%	06	06	06	06
23	Min. Clock Cycle Time at CAS Latency = 2	10.0 / 12.0 ns	A0	C0	A0	C0
24	Max. data access time from Clock for CL=2	6.0 / 7.0 ns	60	70	60	70
25	Minimum Clock Cycle Time at CL = 1	not supported	FF	FF	FF	FF

Byte#	Description	SPD Entry Value	Hex			
			32Mx64 one bank -8	32Mx64 one bank -8B	32Mx72 one bank -8	32Mx72 one bank -8B
26	Maximum Data Access Time from Clock at CL=1	not supported	FF	FF	FF	FF
27	Minimum Row Precharge Time	20 / 30 ns	14	1E	14	1E
28	Minimum Row Active to Row Active delay tRRD	16 / 20 ns	10	14	10	14
29	Minimum RAS to CAS delay tRCD	20 ns	14	14	14	14
30	Minimum RAS pulse width tRAS	50 / 60 ns	32	3C	32	3C
31	Module Bank Density (per bank)	256 MByte	40	40	40	40
32	SDRAM input setup time	2 ns	20	20	20	20
33	SDRAM input hold time	1 ns	10	10	10	10
34	SDRAM data input setup time	2 ns	20	20	20	20
35	SDRAM data input hold time	1 ns	10	10	10	10
62-61	Superset information (may be used in future)		FF	FF	FF	FF
62	SPD Revision	Revision 1.2	12	12	12	12
63	Checksum for bytes 0 - 62		91	D9	A3	EB
64-125	Manufacturers information (optional) (FFh if not used)		XX	XX	XX	XX
126	Frequency Specification	100 MHz	64	64	64	64
127	100 MHz support details		AF	AD	AF	AD
128+	Unused storage locations		FF	FF	FF	FF

### SPD-Table for 256Mbit SDRAM based PC100 Modules:

Byte#	Description	SPD Entry Value	Hex			
			64Mx64 two bank -8	64Mx64 two bank -8B	64Mx72 two bank -8	64Mx72 two bank -8B
0	Number of SPD bytes	128	80	80	80	80
1	Total bytes in Serial PD	256	08	08	08	08
2	Memory Type	SDRAM	04	04	04	04
3	Number of Row Addresses (without BS bits)	13	0D	0D	0D	0D
4	Number of Column Addresses (for 32Mx8 SDRAMs)	10	0A	0A	0A	0A
5	Number of DIMM Banks	2	02	02	02	02
6	Module Data Width	64 / 72	40	40	48	48
7	Module Data Width (cont'd)	0	00	00	00	00
8	Module Interface Levels	LVTTL	01	01	01	01
9	SDRAM Cycle Time at CL=3	10.0 ns	A0	A0	A0	A0
10	SDRAM Access time from Clock at CL=3	6.0 ns	60	60	60	60
11	Dimm Config	none / ECC	00	00	02	02
12	Refresh Rate/Type	Self-Refresh, 7.8 $\mu$ s	82	82	82	82
13	SDRAM width, Primary	x8	08	08	08	08
14	Error Checking SDRAM data width	n/a / x8	00	00	08	08
15	Minimum clock delay for back- to-back random column address	$t_{ccd} = 1$ CLK	01	01	01	01
16	Burst Length supported	1, 2, 4 & 8	0F	0F	0F	0F
17	Number of SDRAM banks	4	04	04	04	04
18	Supported CAS Latencies	CAS latency = 2 & 3	06	06	06	06
19	CS Latencies	CS latency = 0	01	01	01	01
20	WE Latencies	Write latency = 0	01	01	01	01
21	SDRAM DIMM module attributes	non buffered/non reg.	00	00	00	00
22	SDRAM Device Attributes :General	Vcc tol +/- 10%	06	06	06	06
23	Min. Clock Cycle Time at CAS Latency = 2	10.0 / 12.0 ns	A0	C0	A0	C0
24	Max. data access time from Clock for CL=2	6.0 / 7.0 ns	60	70	60	70
25	Minimum Clock Cycle Time at CL = 1	not supported	FF	FF	FF	FF

Byte#	Description	SPD Entry Value	Hex			
			64Mx64 two bank -8	64Mx64 two bank -8B	64Mx72 two bank -8	64Mx72 two bank -8B
26	Maximum Data Access Time from Clock at CL=1	not supported	FF	FF	FF	FF
27	Minimum Row Precharge Time	20 / 30 ns	14	1E	14	1E
28	Minimum Row Active to Row Active delay tRRD	16 / 20 ns	10	14	10	14
29	Minimum RAS to CAS delay tRCD	20 ns	14	14	14	14
30	Minimum RAS pulse width tRAS	50 / 60 ns	32	3C	32	3C
31	Module Bank Density (per bank)	256 MByte	40	40	40	40
32	SDRAM input setup time	2 ns	20	20	20	20
33	SDRAM input hold time	1 ns	10	10	10	10
34	SDRAM data input setup time	2 ns	20	20	20	20
35	SDRAM data input hold time	1 ns	10	10	10	10
62-61	Superset information (may be used in future)		FF	FF	FF	FF
62	SPD Revision	Revision 1.2	12	12	12	12
63	Checksum for bytes 0 - 62		92	DA	A4	EC
64-125	Manufacturers information (optional) (FFh if not used)		XX	XX	XX	XX
126	Frequency Specification	100 MHz	64	64	64	64
127	100 MHz support details		FF	FD	FF	FD
128+	Unused storage locations		FF	FF	FF	FF

### L-DIM-168-30 SDRAM DIMM Module package

