

PRELIMINARY PRODUCT INFORMATION



MOS INTEGRATED CIRCUIT μ PD780016Y, 780018Y

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μ PD780016Y and 780018Y are members of the μ PD780018Y subseries of the 78K/0 series microcontrollers. Besides a high-speed, high-performance CPU, these microcontrollers have on-chip ROM, RAM, I/O ports, timer, serial interface, real-time output port, interrupt control, and various other peripheral hardware.

The μ PD78P0018Y devices including a one-time PROM version and an EPROM version, both of which can operate in the same power supply voltage range as a mask ROM version, and various development tools are available.

The details of the functions are described in the following user's manuals. Be sure to read it before starting design.

μ PD780018,780018Y Subseries User's Manual: U11754E

78K/0 Series User's Manual – Instructions : IEU-1372

FEATURES

- Internal high capacity ROM and RAM

| Part Number | Item | Program Memory (ROM) | Data Memory | | | Package |
|-----------------|------|----------------------|-------------------------|------------|-----------------------|----------------------------------|
| | | | Internal High-Speed RAM | Buffer RAM | Internal Extended RAM | |
| μ PD780016Y | | 48K bytes | 1024 bytes | 32 bytes | 1024 bytes | 100-pin plastic QFP (14 × 20 mm) |
| μ PD780018Y | | 60K bytes | | | | |

- External memory expansion space: 64K bytes
- Instruction execution time can be changed from high-speed (0.4 μ s) to ultra-low-speed (122 μ s)
- I/O ports: 88
- 8-bit resolution A/D converter: 8 channels
- Timer: 7 channels
- Serial interface: 3 channels
 - 3-wire serial I/O mode (with automatic data transmit/receive function): 1 channel
 - 3-wire serial I/O mode (with time division transfer function): 1 channel
 - I²C bus mode (supporting multi-task): 1 channel
- Supply voltage : V_{DD} = 2.7 to 5.5 V

APPLICATION FIELD

Cellular phones, cordless phones, AV equipment, etc.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

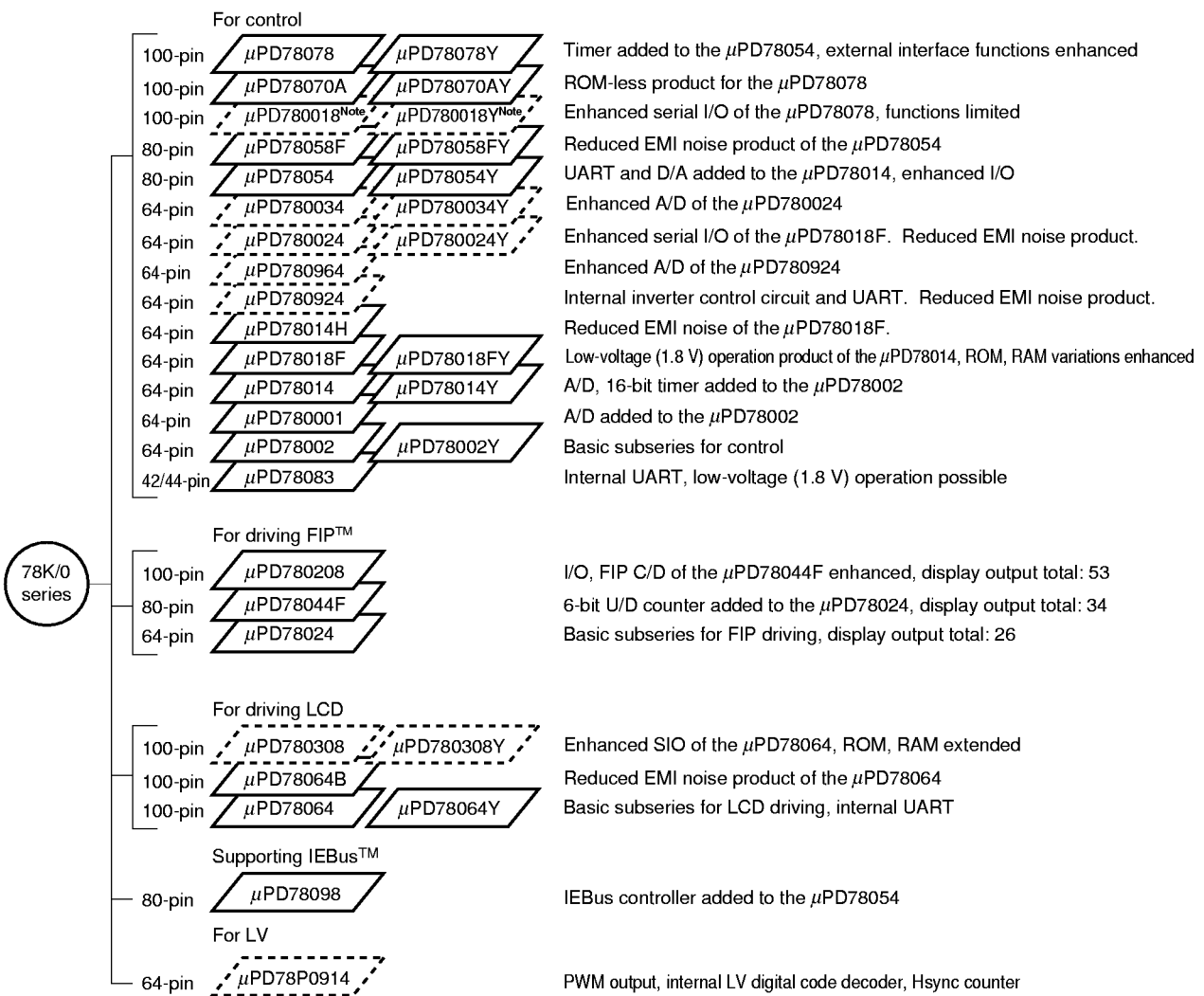
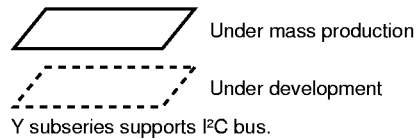
ORDERING INFORMATION

| Part Number | Package |
|----------------------|----------------------------------|
| μPD780016YGF-XXX-3BA | 100-pin plastic QFP (14 × 20 mm) |
| μPD780018YGF-XXX-3BA | 100-pin plastic QFP (14 × 20 mm) |

Remark XXX indicates ROM code suffix.

78K/0 SERIES DEVELOPMENT

These products are a further development in the 78K/0 Series. The designations appearing inside the boxes are subseries names.



Note Under planning

The major functional differences among the subseries are shown below.

| Subseries Name | Function | ROM Capacity | Timer | | | | 8-bit A/D | 10-bit A/D | 8-bit D/A | Serial Interface | I/O | V _{DD} MIN. Value | External Expansion | | |
|-----------------|------------|--------------|-------|--------|-------|-----|-----------|------------|-----------------|------------------|-------|----------------------------|--------------------|-------|-------|
| | | | 8-bit | 16-bit | Watch | WDT | | | | | | | | | |
| For Control | μPD78078 | 32 K-60 K | 4ch | 1ch | 1ch | 1ch | 8ch | — | 2ch | 3ch (UART: 1ch) | 88 | 1.8 V | ○ | | |
| | μPD78070A | — | | | | | | | | 61 | 2.7 V | | | | |
| | μPD780018 | 48 K-60 K | 2ch | — | — | — | — | — | 2ch | 88 | 2.0 V | | | | |
| | μPD78058F | | | | | | | | 3ch (UART: 1ch) | 69 | | | | | |
| | μPD78054 | 16 K-60 K | 3ch | Note | — | — | — | — | — | 51 | 1.8 V | | | | |
| | μPD780034 | 8 K-32 K | | | | | | | | 8ch | — | | | | |
| | μPD780024 | 8 K-32 K | 3ch | Note | — | — | — | — | — | 8ch | — | 47 | | 2.7 V | |
| | μPD780964 | | | | | | | | | 2ch (UART: 2ch) | | | | | |
| | μPD780924 | 8 K-32 K | 2ch | 1ch | 1ch | — | — | — | — | — | 8ch | — | | 53 | 1.8 V |
| | μPD78014H | | | | | | | | | | 2ch | 53 | | 1.8 V | |
| | μPD78018F | 8 K-60 K | 2ch | 1ch | 1ch | — | — | — | — | — | 53 | 2.7 V | | | |
| | μPD78014 | 8 K-32 K | | | | | | | | | 39 | — | | | |
| | μPD780001 | 8 K | 2ch | — | — | — | — | — | — | — | 1ch | 39 | | — | |
| | μPD78002 | 8 K-16 K | | | | | | | | | 53 | ○ | | | |
| μPD78083 | 8 K | 1ch | — | — | — | — | — | — | — | 33 | 1.8 V | — | | | |
| For FIP driving | μPD780208 | 32 K-60 K | 2ch | 1ch | 1ch | 1ch | 8ch | — | — | 2ch | 74 | 2.7 V | — | | |
| | μPD78044F | 16 K-40 K | | | | | | | | | 68 | | | | |
| | μPD78024 | 24 K-32 K | | | | | | | | | 54 | | | | |
| For LCD driving | μPD780308 | 48 K-60 K | 2ch | 1ch | 1ch | 1ch | 8ch | — | — | 3ch (UART: 1ch) | 57 | 1.8 V | — | | |
| | μPD78064B | 32 K | | | | | | | | 2ch (UART: 1ch) | | 2.0 V | | | |
| | μPD78064 | 16 K-32 K | | | | | | | | 1ch | — | | | | |
| For IEBus | μPD78098 | 32 K-60 K | 2ch | 1ch | 1ch | 1ch | 8ch | — | 2ch | 3ch (UART: 1ch) | 69 | 2.7 V | ○ | | |
| For LV | μPD78P0914 | 32 K | 6ch | — | — | 1ch | 8ch | — | — | 2ch | 54 | 4.5 V | ○ | | |

Note 10-bit timer: 1 channel

OVERVIEW OF FUNCTION

| Item | | Part Number | μPD780016Y | μPD780018Y |
|----------------------------|---------------------------------|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|
| | | | | |
| Internal memory | ROM | | 48K bytes | 60K bytes |
| | Internal high-speed RAM | | 1024 bytes | |
| | Buffer RAM | | 32 bytes | |
| | Internal expansion RAM | | 1024 bytes | |
| Memory space | | | 64K bytes | |
| General registers | | | 8 bits × 32 registers (8 bits × 8 registers × 4 banks) | |
| Instruction cycle | | | On-chip instruction execution time selective function | |
| | When main system clock selected | | 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (at 5.0 MHz) | |
| | When subsystem clock selected | | 122 μs (at 32.768 kHz) | |
| Instruction set | | | <ul style="list-style-type: none"> • 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD adjustment, etc. | |
| I/O ports | | | Total : 88 <ul style="list-style-type: none"> • CMOS input : 9 • CMOS I/O : 79 | |
| A/D converter | | | • 8-bit resolution × 8 channels | |
| Serial interface | | | <ul style="list-style-type: none"> • 3-wire serial I/O mode (with automatic data transmit/receive function): 1 channel • 3-wire serial I/O mode (with time division transfer function) : 1 channel • I²C bus mode (supporting multi-task) : 1 channel | |
| Timer | | | <ul style="list-style-type: none"> • 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 4 channels • Watch timer : 1 channel • Watchdog timer : 1 channel | |
| Timer output | | | 5 (14-bit PWM output × 1, 8-bit PWM output × 2) | |
| Clock output | | | 39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz, 2.5 MHz, 5.0 MHz (at main system clock of 5.0 MHz) 32.768 kHz (at subsystem clock of 32.768 kHz) | |
| Buzzer output | | | 2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock: at 5.0 MHz) | |
| Vectored interrupt sources | Maskable | | Internal : 12 External: 7 | |
| | Non-maskable | | Internal : 1 | |
| | Software | | 1 | |
| Test input | | | Internal : 1 External: 1 | |
| Supply voltage | | | V _{DD} = 2.7 to 5.5 V | |
| Package | | | • 100-pin plastic QFP (14 × 20 mm) | |

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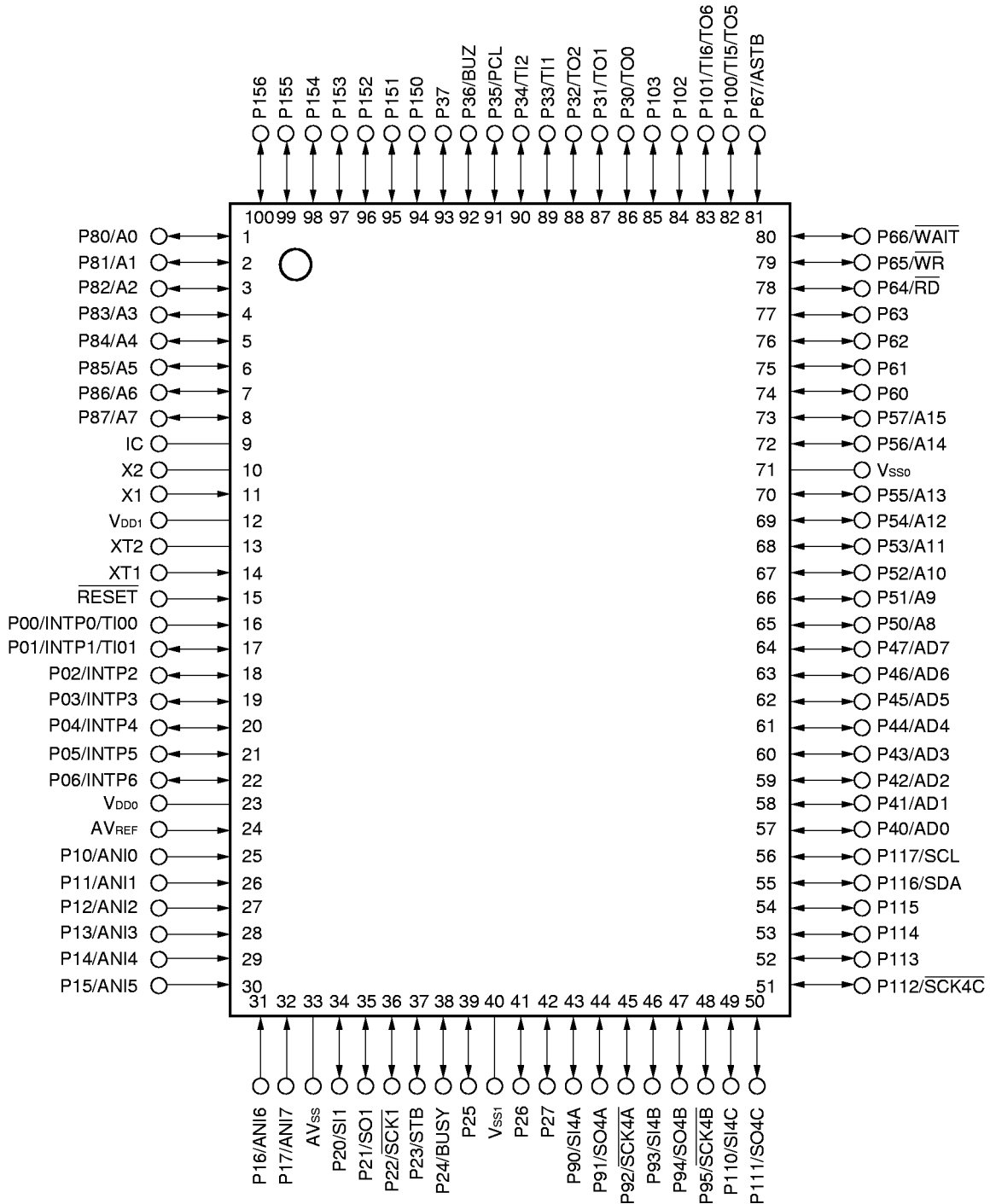
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1. PIN CONFIGURATION (TOP VIEW)

- 100-pin plastic QFP (14 × 20 mm)
μPD780016YGF-XXX-3BA, 780018YGF-XXX-3BA

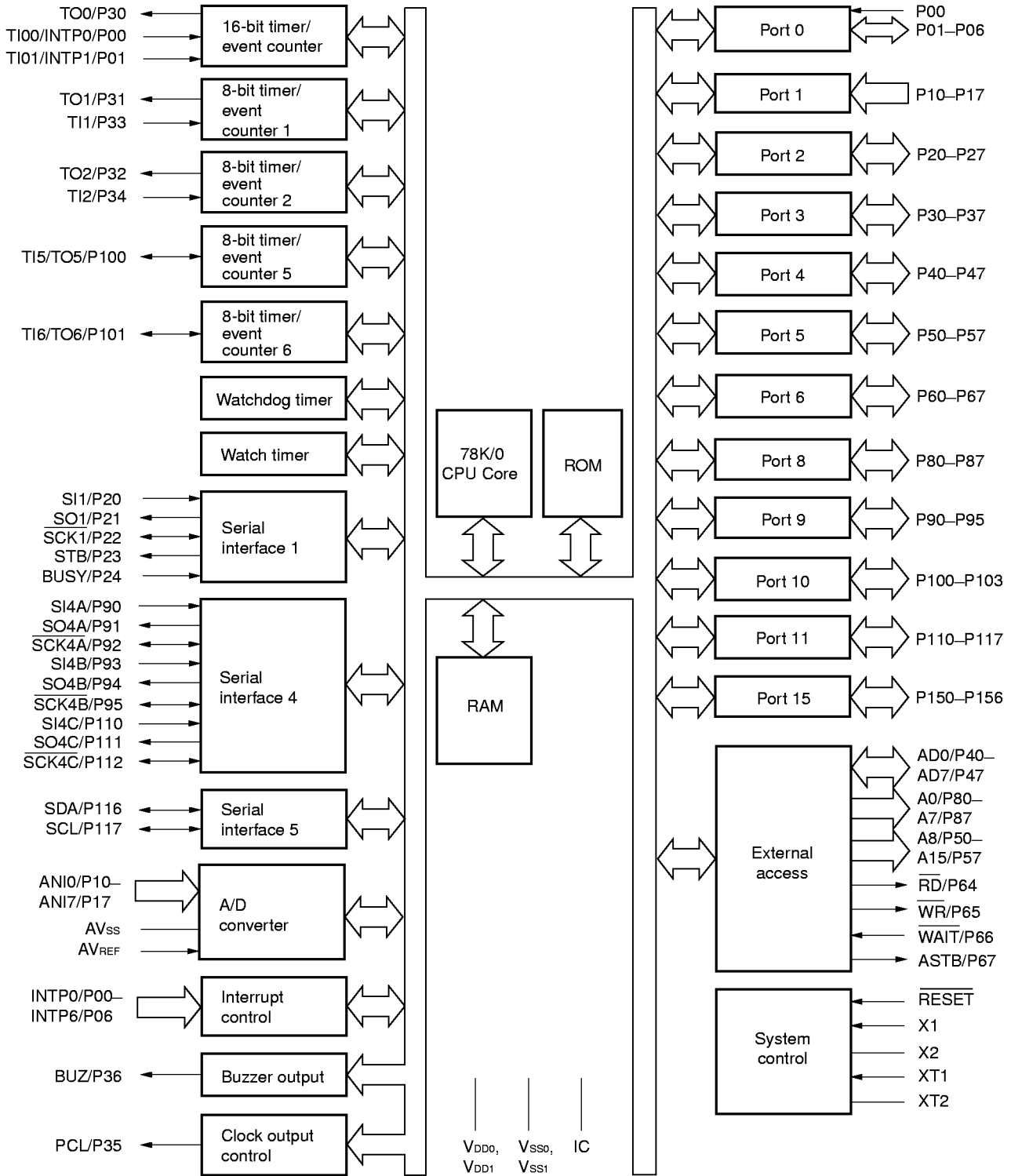


- Cautions**
1. Connect IC (internally connected) pin directly to V_{SS0}.
 2. AV_{SS} pin should be connected to V_{SS0}.

Remark When the circuit is used in an application where the noise generated from the inside of the microcontroller needs to be reduced, take countermeasures against noise such as supplying power to V_{DD0} and V_{DD1} separately and connecting V_{SS0} and V_{SS1} to the ground line separately.

| | | | |
|-------------------|------------------------------|--------------------------------------------------------------|-------------------------------|
| A0-A15 | : Address Bus | PCL | : Programmable Clock |
| AD0-AD7 | : Address/Data Bus | \overline{RD} | : Read Strobe |
| ANI0-ANI7 | : Analog Input | \overline{RESET} | : Reset |
| ASTB | : Address Strobe | $\overline{SCK1}$ | : Serial Clock |
| AV _{REF} | : Analog Reference Voltage | $\overline{SCK4A}$, $\overline{SCK4B}$, $\overline{SCK4C}$ | : Serial Clock |
| AV _{SS} | : Analog Ground | SCL | : Serial Clock |
| BUSY | : Busy | SDA | : Serial Data |
| BUZ | : Buzzer Clock | SI1 | : Serial Input |
| IC | : Internally Connected | SI4A, SI4B, SI4C | : Serial Input |
| INTP0-INTP6 | : Interrupt from Peripherals | SO1 | : Serial Output |
| P00-P06 | : Port0 | SO4A, SO4B, SO4C | : Serial Output |
| P10-P17 | : Port1 | STB | : Strobe |
| P20-P27 | : Port2 | TI00, TI01 | : Timer Input |
| P30-P37 | : Port3 | TI1, TI2, TI5, TI6 | : Timer Input |
| P40-P47 | : Port4 | TO0-TO2, TO5, TO6 | : Timer Output |
| P50-P57 | : Port5 | V _{DD0} , V _{DD1} | : Power Supply |
| P60-P67 | : Port6 | V _{SS0} , V _{SS1} | : Ground |
| P80-P87 | : Port8 | \overline{WAIT} | : Wait |
| P90-P96 | : Port9 | \overline{WR} | : Write Strobe |
| P100-P103 | : Port10 | X1, X2 | : Crystal (Main System Clock) |
| P110-P117 | : Port11 | XT, XT2 | : Crystal (Subsystem Clock) |
| P150-P156 | : Port15 | | |

2. BLOCK DIAGRAM



Remark The internal ROM capacity depends on the product.

3. PIN FUNCTIONS

3.1 Port Pins (1/2)

| Pin Name | I/O | Function | | After Reset | Alternate Function Pin |
|------------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------|--------------|------------------------|
| P00 | Input | Port 0 7-bit I/O port | Input only | Input | INTP0/TI00 |
| P01 | Input/ output | | Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. | Input | INTP1/TI01 |
| P02 | | | | | INTP2 |
| P03 | | | | | INTP3 |
| P04 | | | | | INTP4 |
| P05 | | | | | INTP5 |
| P06 | | | | | INTP6 |
| P10 to P17 | Input | Port 1 8-bit input port On-chip pull-up resistor can be used by software. ^{Note} | Input | ANI0 to ANI7 | |
| P20 | Input/ output | Port 2 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. | Input | SI1 | |
| P21 | | | | SO1 | |
| P22 | | | | SCK1 | |
| P23 | | | | STB | |
| P24 | | | | BUSY | |
| P25-P27 | | | | — | |
| P30 | Input/ output | Port 3 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. | Input | TO0 | |
| P31 | | | | TO1 | |
| P32 | | | | TO2 | |
| P33 | | | | TI1 | |
| P34 | | | | TI2 | |
| P35 | | | | PCL | |
| P36 | | | | BUZ | |
| P37 | | | | — | |
| P40 to P47 | Input/ output | Port 4 8-bit input/output port Input/output can be specified in 8-bit units. When used as an input port, on-chip pull-up resistor can be used by software. Test input flag (KRIF) is set to 1 by falling edge detection. | Input | AD0 to AD7 | |

Note When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input, on-chip pull-up resistor is automatically disconnected.

3.1 Port Pins (2/2)

| Pin Name | I/O | Function | After Reset | Alternate Function Pin |
|------------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|------------------------|
| P50 to P57 | Input/output | Port 5 8-bit input/output port LED can be driven directly. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. | Input | A8 to A15 |
| P60 | Input/output | Port 6 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. | Input | — |
| P61 | | | | |
| P62 | | | | |
| P63 | | | | |
| P64 | | | | \overline{RD} |
| P65 | | | | \overline{WR} |
| P66 | | | | \overline{WAIT} |
| P67 | | | | ASTB |
| P80 to P87 | Input/output | Port 8 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. | Input | A0 to A7 |
| P90 | Input/output | Port 9 6-bit input/output port Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. | Input | SI4A |
| P91 | | | | SO4A |
| P92 | | | | $\overline{SCK4A}$ |
| P93 | | | | SI4B |
| P94 | | | | SO4B |
| P95 | | | | $\overline{SCK4B}$ |
| P100 | Input/output | Port 10 4-bit input/output port Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. | Input | TI5/TO5 |
| P101 | | | | TI6/TO6 |
| P102, P103 | | | | — |
| P110 | Input/output | Port 11 8-bit input/output port Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. | Input | SI4C |
| P111 | | | | SO4C |
| P112 | | | | $\overline{SCK4C}$ |
| P113-P115 | | | | — |
| P116 | | | | SDA |
| P117 | | | | SCL |
| P150-P156 | Input/output | Port 15 7-bit input/output port Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. | Input | — |

3.2 Non-port Pins (1/2)

| Pin Name | I/O | Function | After Reset | Alternate Function Pin |
|------------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------|-------------|------------------------|
| INTP0 | Input | External interrupt request input by which the active edge (rising edge, falling edge, or both rising and falling edges) can be specified. | Input | P00/TI00 |
| INTP1 | | | | P01/TI01 |
| INTP2 | | | | P02 |
| INTP3 | | | | P03 |
| INTP4 | | | | P04 |
| INTP5 | | | | P05 |
| INTP6 | | | | P06 |
| SI1 | Input | Serial interface serial data input. | Input | P20 |
| SI4A | | | | P90 |
| SI4B | | | | P93 |
| SI4C | | | | P110 |
| SO1 | Output | Serial interface serial data output. | Input | P21 |
| SO4A | | | | P91 |
| SO4B | | | | P94 |
| SO4C | | | | P111 |
| SDA | Input/output | Input/output of serial data of serial interface. | Input | P116 |
| SCK1 | Input /output | Serial interface serial clock input/output. | Input | P22 |
| SCK4A | | | | P92 |
| SCK4B | | | | P95 |
| SCK4C | | | | P112 |
| SCL | | | | P117 |
| STB | Output | Serial interface automatic transmit/receive strobe output. | Input | P23 |
| BUSY | Input | Serial interface automatic transmit/receive busy input. | Input | P24 |
| TI00 | Input | External count clock input to 16-bit timer (TM0). | Input | P00/INTP0 |
| TI01 | | Capture trigger signal input to capture register (CR00). | | P01/INTP1 |
| TI1 | | External count clock input to 8-bit timer (TM1). | | P33 |
| TI2 | | External count clock input to 8-bit timer (TM2). | | P34 |
| TI5 | | External count clock input to 8-bit timer (TM5). | | P100/TO5 |
| TI6 | | External count clock input to 8-bit timer (TM6). | | P100/TO6 |
| TO0 | Output | 16-bit timer (TM0) output (also used for 14-bit PWM output). | Input | P30 |
| TO1 | | 8-bit timer (TM1) output. | | P31 |
| TO2 | | 8-bit timer (TM2) output. | | P32 |
| TO5 | | 8-bit timer (TM5) output (also used for 8-bit PWM output). | | P100/TO5 |
| TO6 | | 8-bit timer (TM6) output (also used for 8-bit PWM output). | | P101/TO6 |
| PCL | Output | Clock output (for main system clock, subsystem clock trimming). | Input | P35 |
| BUZ | Output | Buzzer output. | Input | P36 |
| AD0 to AD7 | Input /output | Low-order address/data bus at external memory expansion. | Input | P40 to P47 |

3.2 Non-port Pins (2/2)

| Pin Name | I/O | Function | After Reset | Alternate Function Pin |
|--------------------|--------|----------------------------------------------------------------------------------------------------------------------|-------------|------------------------|
| A0 to A7 | Output | Low-order address bus at external memory expansion. | Input | P80 to P87 |
| A8 to A15 | Output | High-order address bus at external memory expansion. | Input | P50 to P57 |
| \overline{RD} | Output | External memory read operation strobe signal output. | Input | P64 |
| \overline{WR} | | External memory write operation strobe signal output. | | P65 |
| \overline{WAIT} | Input | Wait insertion at external memory access. | Input | P66 |
| ASTB | Output | Strobe output which externally latches the address information output to ports 4, 5 and 8 to access external memory. | Input | P67 |
| ANI0 to ANI7 | Input | A/D converter analog input. | Input | P10 to P17 |
| AVREF | Input | A/D converter reference voltage input (shared with analog power supply). | — | — |
| AVSS | — | A/D converter ground potential. Same potential as V _{SS0} . | — | — |
| \overline{RESET} | Input | System reset input. | — | — |
| X1 | Input | Main system clock oscillation crystal connection. | — | — |
| X2 | — | | — | — |
| XT1 | Input | Subsystem clock oscillation crystal connection. | Input | — |
| XT2 | — | | — | — |
| VDD0 | — | Port block positive power supply. | — | — |
| VSS0 | — | Port block ground potential. | — | — |
| VDD1 | — | Positive power supply (except for port and analog blocks) | — | — |
| VSS1 | — | Ground potential (except for port and analog blocks) | — | — |
| IC | — | Internal connection. Connect directly to V _{SS0} . | — | — |

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1. For the input/output circuit configuration of each type, see Figure 3-1.

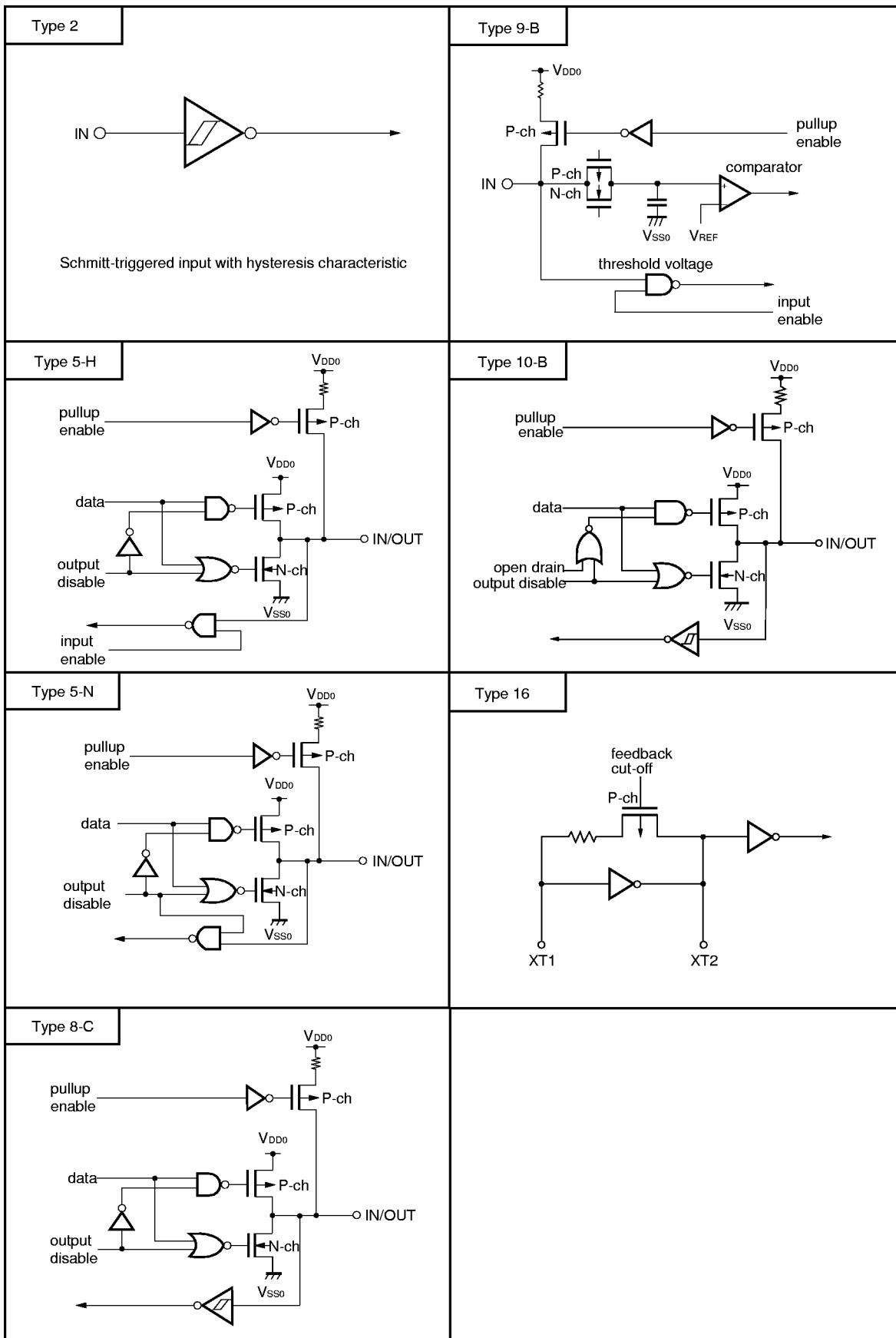
Table 3-1. Types of Pin Input/Output Circuits (1/2)

| Pin Name | Input/Output Circuit Type | I/O | Recommended Connection for Unused Pins | | |
|-------------------|---------------------------|--------------|------------------------------------------------------------------------------|--------------|------------------------------------------------------------------------------|
| P00/INTP0/TI00 | 2 | Input | Connect to V _{SS0} . | | |
| P01/INTP1/TI01 | 8-C | Input/output | Connect to V _{SS0} via a resistor individually. | | |
| P02/INTP2 | | | | | |
| P03/INTP3 | | | | | |
| P04/INTP4 | | | | | |
| P05/INTP5 | | | | | |
| P06/INTP6 | | | | | |
| P10/ANI0-P17/ANI7 | 9-B | Input | Connect to V _{DD0} or V _{SS0} via a resistor individually. | | |
| P20/SI1 | 8-C | Input/output | | | |
| P21/SO1 | 5-H | | | | |
| P22/SCK1 | 8-C | | | | |
| P23/STB | 5-H | | | | |
| P24/BUSY | 8-C | | | | |
| P25-P27 | 5-H | | | | |
| P30/TO0-P32/TO2 | | | | | |
| P33/TI1 | 8-C | | | | |
| P34/TI2 | | | | | |
| P35/PCL | 5-H | | | | |
| P36/BUZ | | | | | |
| P37 | | | | | |
| P40/AD0-P47/AD7 | 5-N | | | Input/output | Connect to V _{DD0} via a resistor individually. |
| P50/A8-P57/A15 | 5-H | | | Input/output | Connect to V _{DD0} or V _{SS0} via a resistor individually. |
| P60-P63 | | | | | |
| P64/RD | | | | | |
| P65/WR | | | | | |
| P66/WAIT | | | | | |
| P67/ASTB | | | | | |
| P80/A0-P87/A7 | | | | | |
| P90/SI4A | | 8-C | | | |
| P91/SO4A | | 5-H | | | |
| P92/SCK4A | | 8-C | | | |
| P93/SI4B | | | | | |
| P94/SO4B | | 5-H | | | |
| P95/SCK4B | | 8-C | | | |

Table 3-1. Types of Pin Input/Output Circuits (2/2)

| Pin Name | Input/Output Circuit Type | I/O | Recommended Connection for Unused Pins |
|---------------------------------|---------------------------|--------------|----------------------------------------------------------------|
| P100/TI5/TO5 | 8-C | Input/output | Connect to V_{DD0} or V_{SS0} via a resistor individually. |
| P101/TI6/TO6 | | | |
| P102, P103 | 5-H | | |
| P110/SI4C | 8-C | | |
| P111/SO4C | 5-H | | |
| P112/ $\overline{\text{SCK4C}}$ | 8-C | | |
| P113-P115 | 5-H | | |
| P116/SDA | 10-B | | |
| P117/SCL | | | |
| P150-P156 | 5-H | | |
| $\overline{\text{RESET}}$ | 2 | Input | — |
| XT1 | 16 | — | Connect to V_{DD0} . |
| XT2 | | | Leave open. |
| AV_{REF} | — | | Connect to V_{SS0} . |
| AV_{SS} | | | |
| IC | | | Connect to V_{SS0} . |

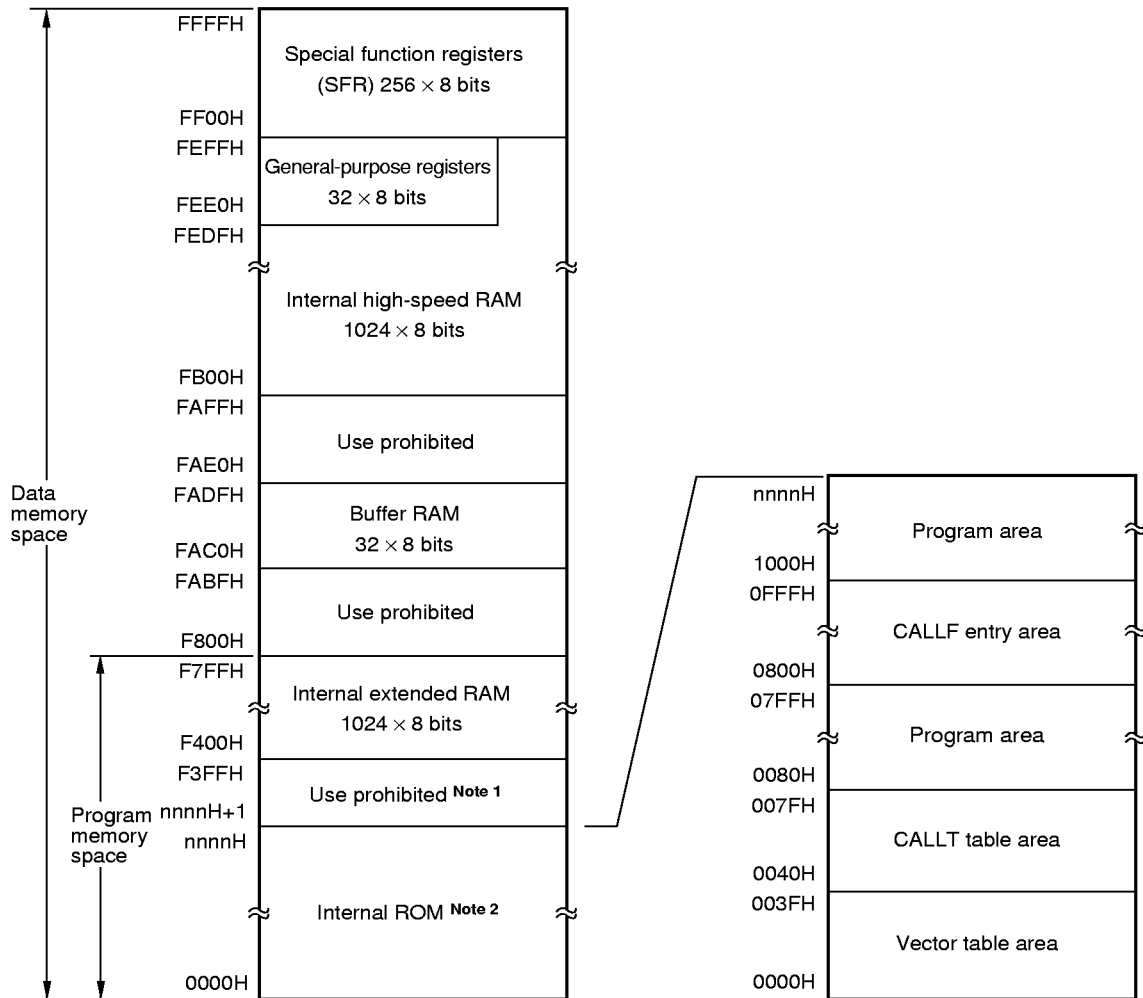
Figure 3-1. Pin Input/Output Circuits



4. MEMORY SPACE

The memory map of the μPD780016Y and 780018Y is shown in Figure 4-1.

Figure 4-1. Memory Map



- Notes**
1. If external device expansion functions are to be employed for the μPD780018Y, set the size of the internal ROM to below 56K bytes using the memory size switching register (IMS).
 2. The internal ROM capacity depends on the product. (See the following table.)

| Part Number | Internal ROM Last Address nnnnH |
|-------------|------------------------------------|
| μPD780016Y | BFFFH |
| μPD780018Y | EFFFH |

5. PERIPHERAL HARDWARE FUNCTIONS

5.1 Ports

Input/output ports are classified into two types.

- CMOS input (P00, Port 1) : 9
 - CMOS input/output (P01 to P06, Port 2 to 6, Port 8 to 11, Port 15) : 79
-
- Total : 88

Table 5-1. Functions of Ports

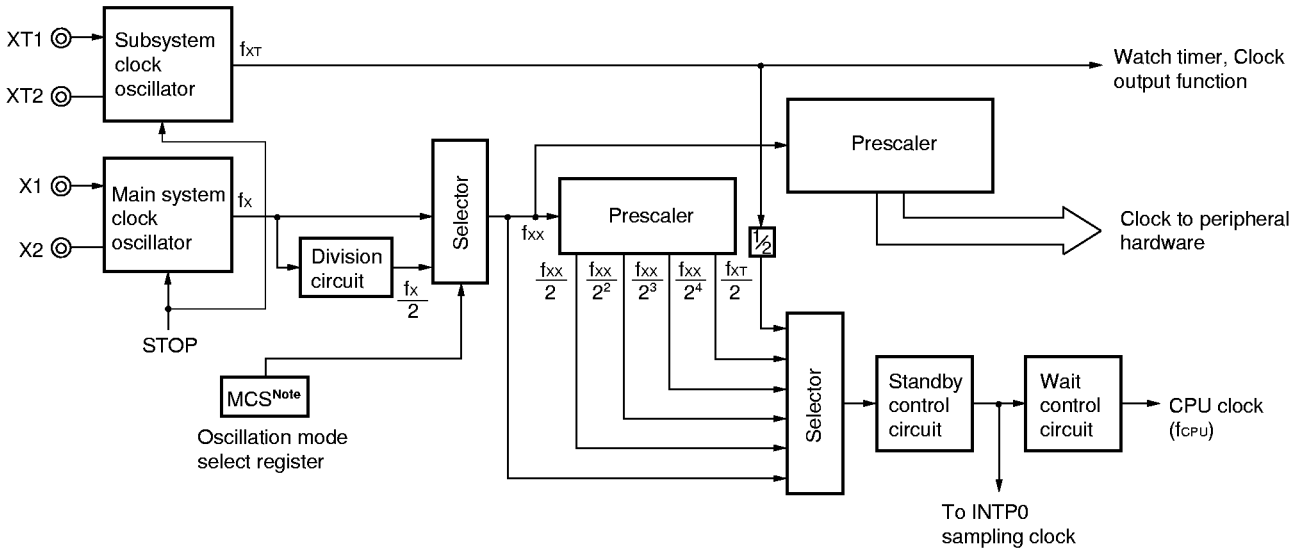
| Port Name | Pin Name | Function |
|-----------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Port 0 | P00 | Input only. |
| | P01 to P06 | Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. |
| Port 1 | P10 to P17 | Input only. On-chip pull-up resistor can be used by software. |
| Port 2 | P20 to P27 | Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. |
| Port 3 | P30 to P37 | Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. |
| Port 4 | P40 to P47 | Input/output port. Input/output can be specified in 8-bit units. When used as an input port, on-chip pull-up resistor can be used by software. The test input flag (KRIF) is set to 1 by falling edge detection. |
| Port 5 | P50 to P57 | Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. LED can be driven directly. |
| Port 6 | P60 to P67 | Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. |
| Port 8 | P80 to P87 | Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. |
| Port 9 | P90 to P95 | Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. |
| Port 10 | P100 to P103 | Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. |
| Port 11 | P110 to P117 | Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. |
| Port 15 | P150 to P156 | Input/output port. Input/output can be specified bit-wise. When used as an input port, on-chip pull-up resistor can be used by software. |

5.2 Clock Generator

There are two kinds of clock generators: main system and subsystem clock generators.
It is possible to change the instruction execution time.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (at main system clock frequency of 5.0 MHz)
- 122 μs (at subsystem clock frequency of 32.768 kHz)

Figure 5-1. Clock Generator Block Diagram



Note Be sure to set 1 to MCS.

5.3 Timer/Event Counter

There are the following seven timer/event counter channels:

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 4 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2. Types and Functions of Timer/Event Counters

| | | 16-bit Timer/Event Counter | 8-bit Timer/Event Counters 1, 2 | 8-bit Timer/Event Counters 5, 6 | Watch Timer | Watchdog Timer |
|----------|-------------------------|----------------------------|---------------------------------|---------------------------------|-------------|----------------|
| Type | Interval timer | 1 channel | 2 channels | 2 channels | 1 channel | 1 channel |
| | External event counter | 1 channel | 2 channels | 2 channels | — | — |
| Function | Timer output | 1 output | 2 outputs | 2 outputs | — | — |
| | PWM output | 1 output | — | 2 outputs | — | — |
| | Pulse width measurement | 2 inputs | — | — | — | — |
| | Square wave output | 1 output | 2 outputs | 2 outputs | — | — |
| | One-shot pulse output | 1 output | — | — | — | — |
| | Interrupt request | 2 | 2 | 2 | 1 | 1 |
| | Test input | — | — | — | 1 input | — |

Figure 5-2. 16-Bit Timer/Event Counter Block Diagram

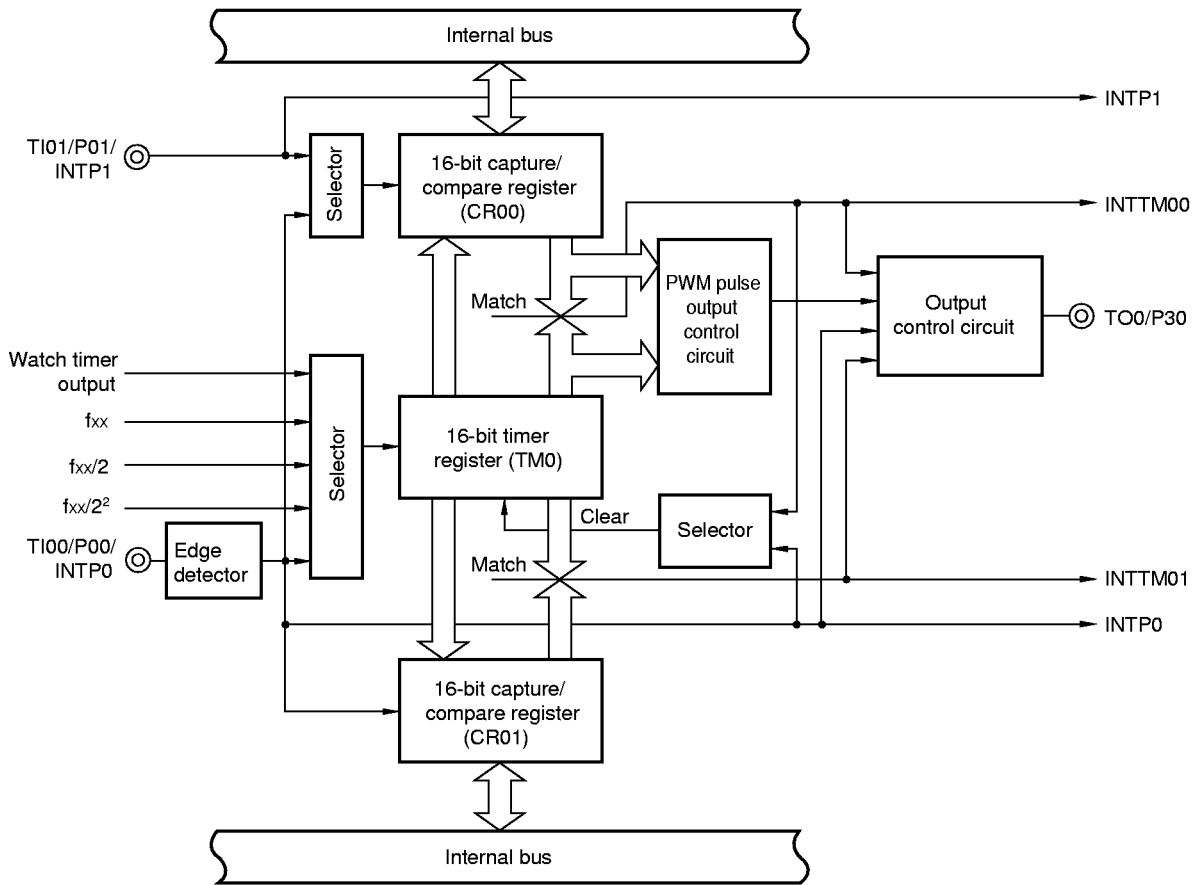


Figure 5-3. 8-Bit Timer/Event Counter 1, 2 Block Diagram

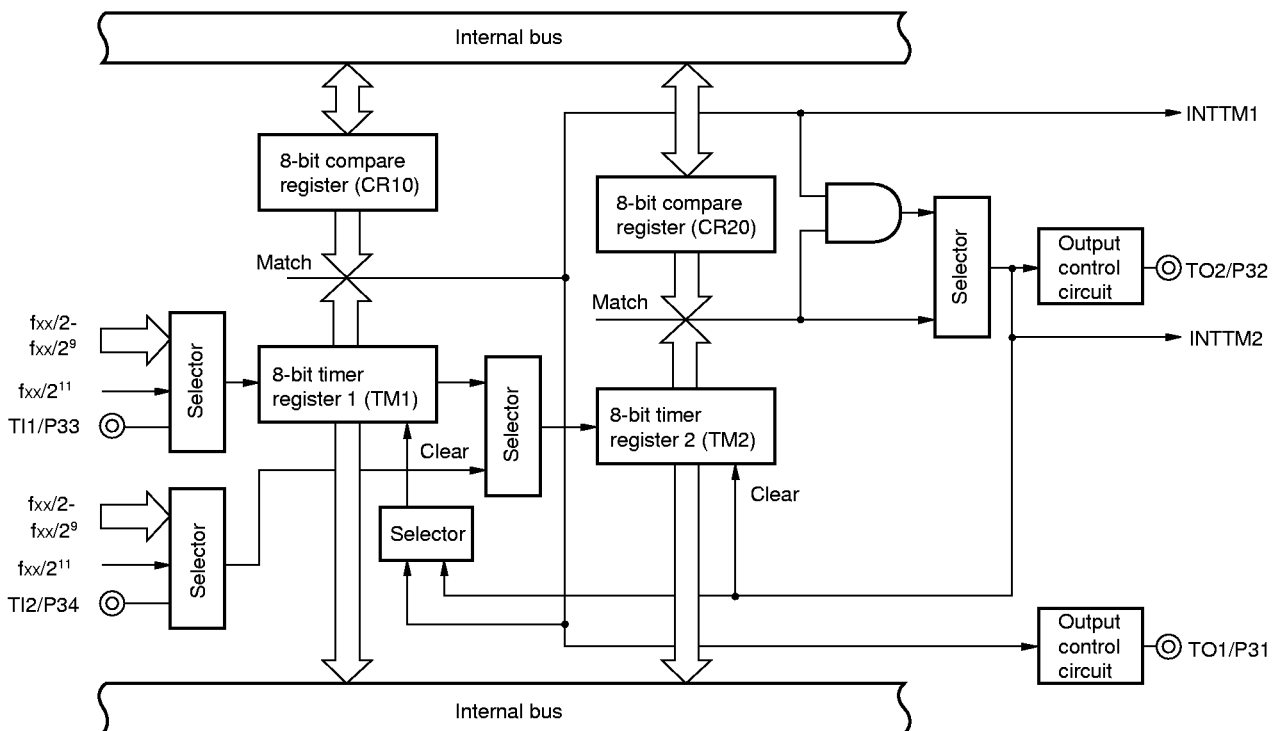
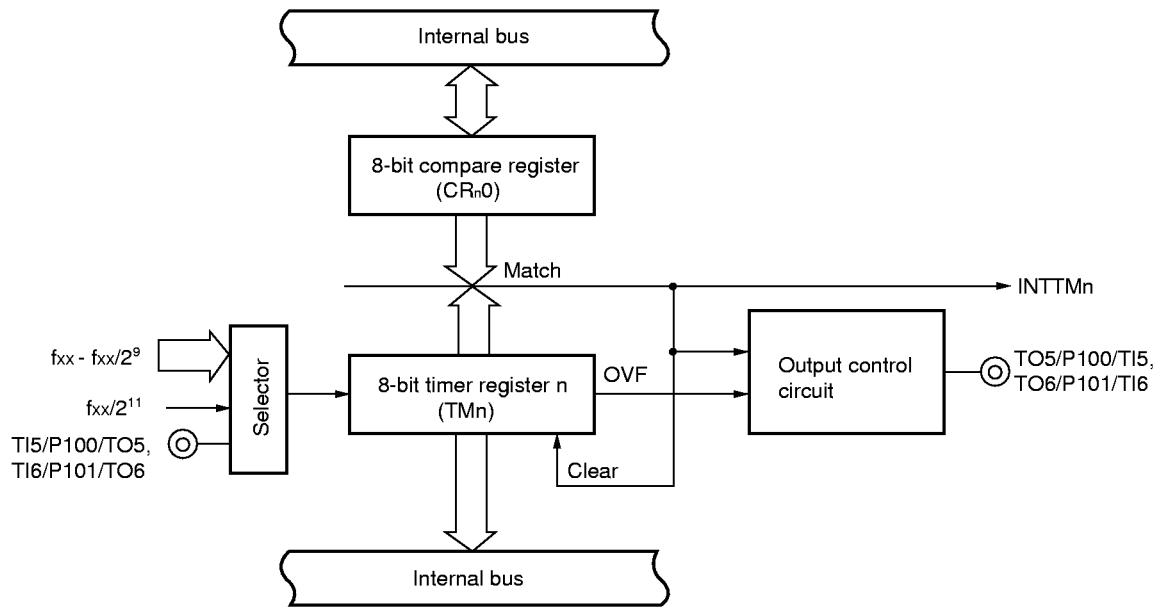


Figure 5-4. 8-Bit Timer/Event Counter 5, 6 Block Diagram



n = 5, 6

Figure 5-5. Watch Timer Block Diagram

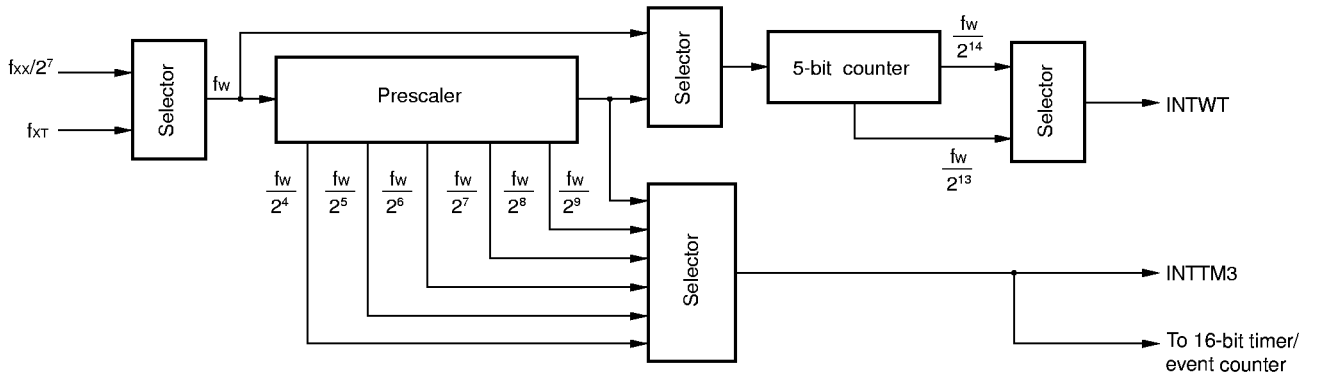
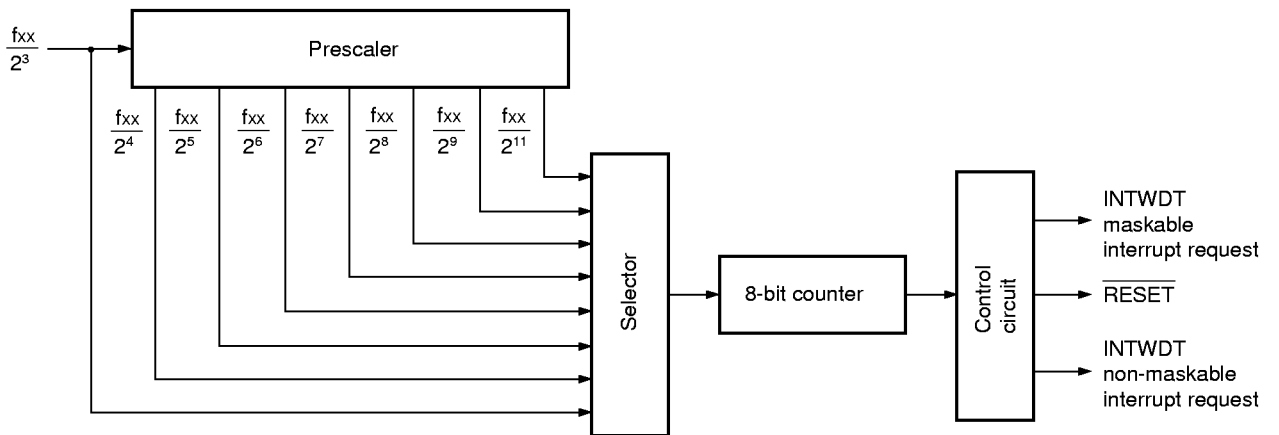


Figure 5-6. Watchdog Timer Block Diagram

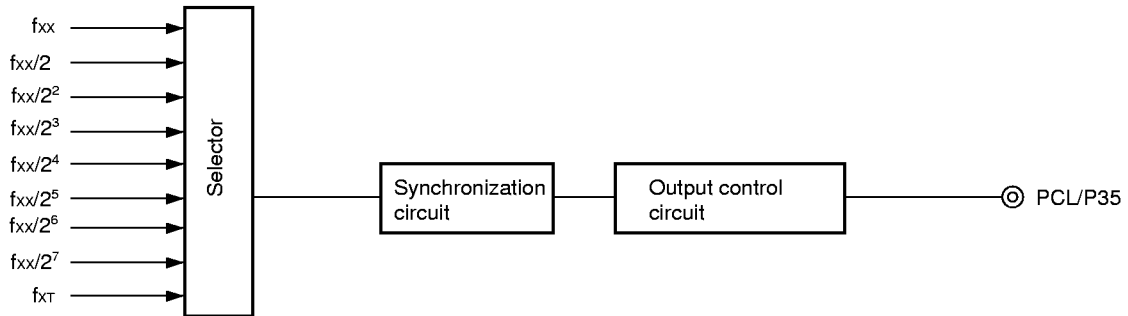


5.4 Clock Output Control Circuit

This circuit can output clocks of the following frequencies:

- 39.1 kHz/78.1 kHz/156 kHz/313 kHz/625 kHz/1.25 MHz/2.5 MHz/5.0 MHz (at main system clock frequency of 5.0 MHz)
- 32.768 kHz (at subsystem clock frequency of 32.768 kHz)

Figure 5-7. Clock Output Control Circuit Block Diagram

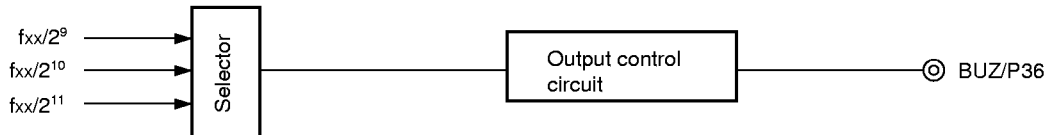


5.5 Buzzer Output Control Circuit

This circuit can output clocks of the following frequencies that can be used for driving buzzers:

- 2.4 kHz/4.9 kHz/9.8 kHz (at main system clock frequency of 5.0 MHz)

Figure 5-8. Buzzer Output Control Circuit Block Diagram



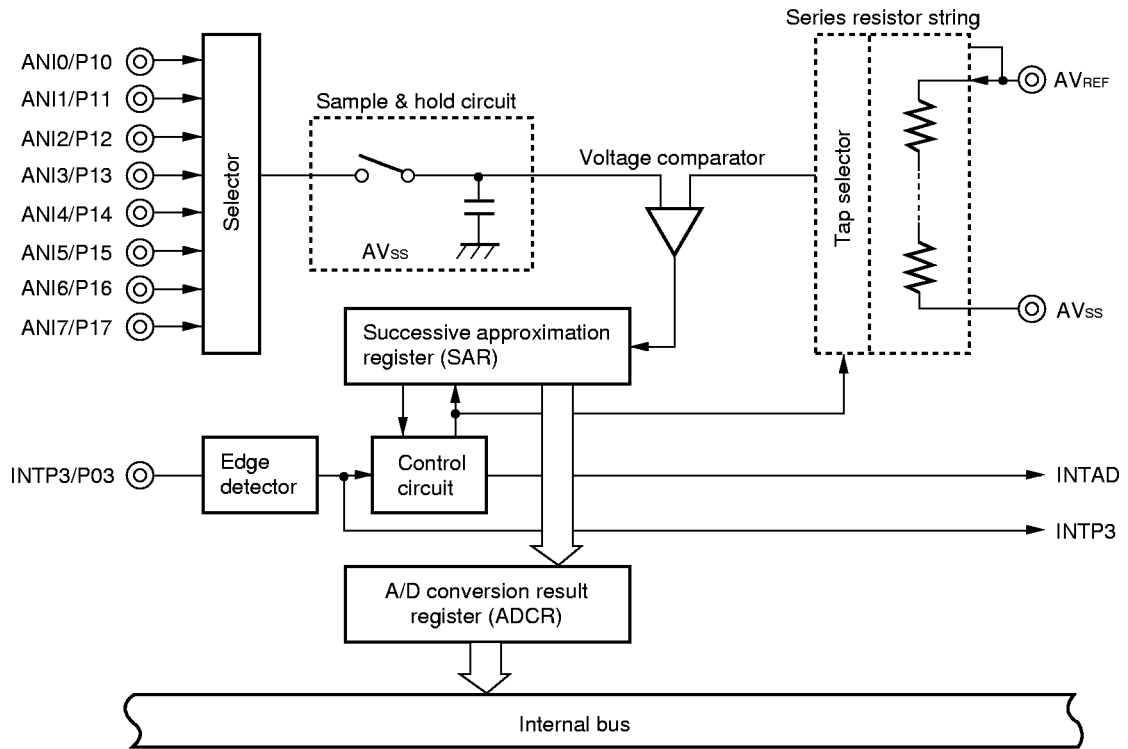
5.6 A/D Converter

The A/D converter consists of eight 8-bit resolution channels.

A/D conversion can be started by the following two methods:

- Hardware starting
- Software starting

Figure 5-9. A/D Converter Block Diagram



5.7 Serial Interfaces

There are the following three on-chip serial interface channels synchronous with the clock:

- Serial interface channel 1
- Serial interface channel 4
- Serial interface channel 5

Table 5-3. Types and Functions of Serial Interfaces

| Function | Serial Interface Channel 1 | Serial Interface Channel 4 | Serial Interface Channel 5 |
|----------------------------------------------------------------------|------------------------------------------------|------------------------------------------------|----------------------------|
| 3-wire serial I/O mode | ○ (Starting bit MSB/LSB switching possible) | ○ (Starting bit MSB/LSB switching possible) | — |
| 3-wire serial I/O mode with automatic data transmit/receive function | ○ (Starting bit MSB/LSB switching possible) | — | — |
| 3-wire serial I/O mode with automatic data transmit/receive function | — | ○ (Starting bit MSB/LSB switching possible) | — |
| I ² C bus mode | — | — | ○ (MSB first) |

Figure 5-10. Serial Interface Channel 1 Block Diagram

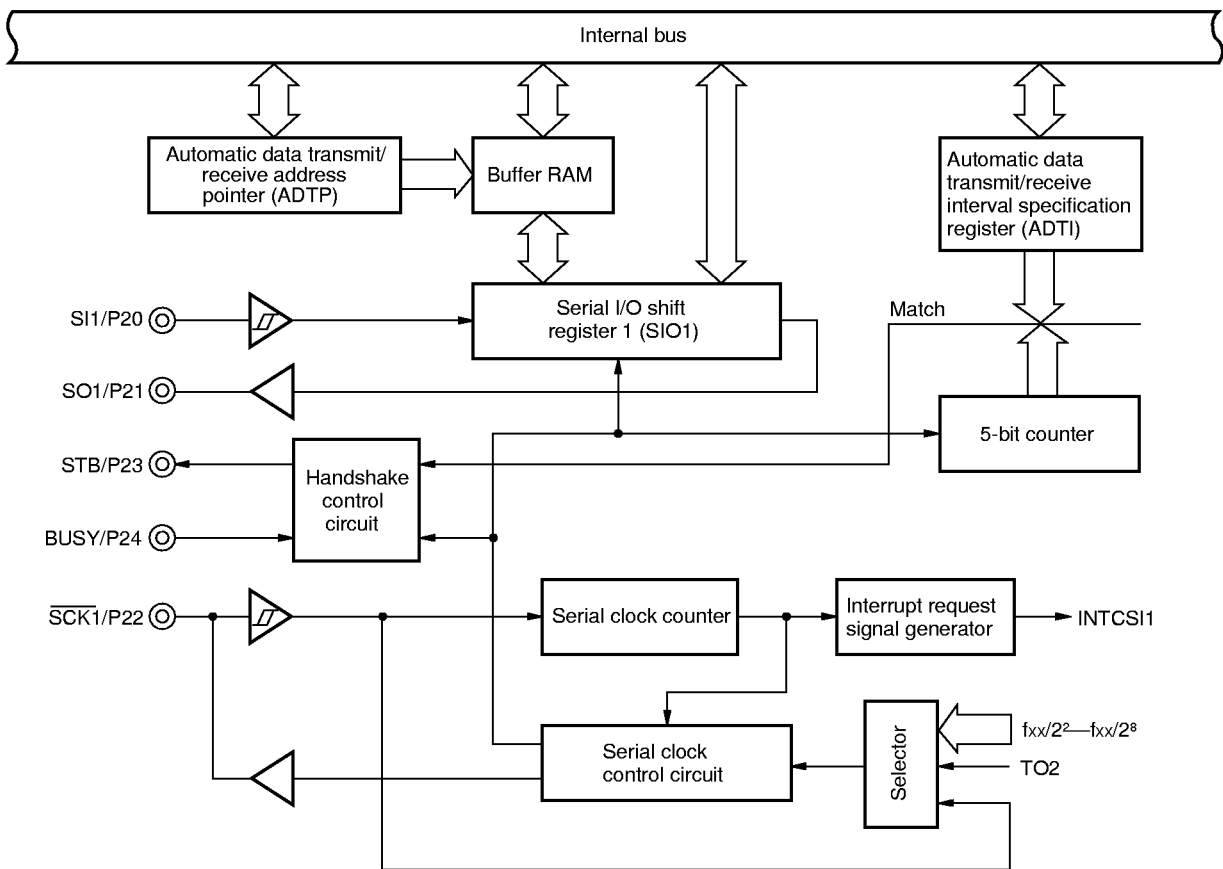


Figure 5-11. Serial Interface Channel 4 Block Diagram

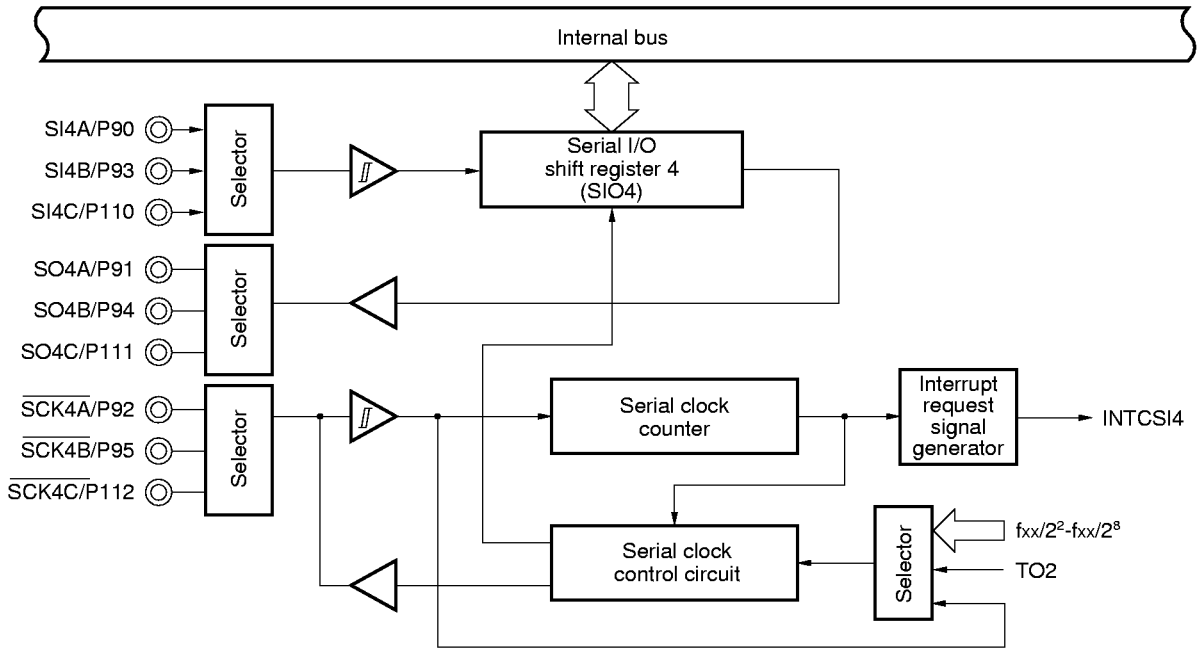
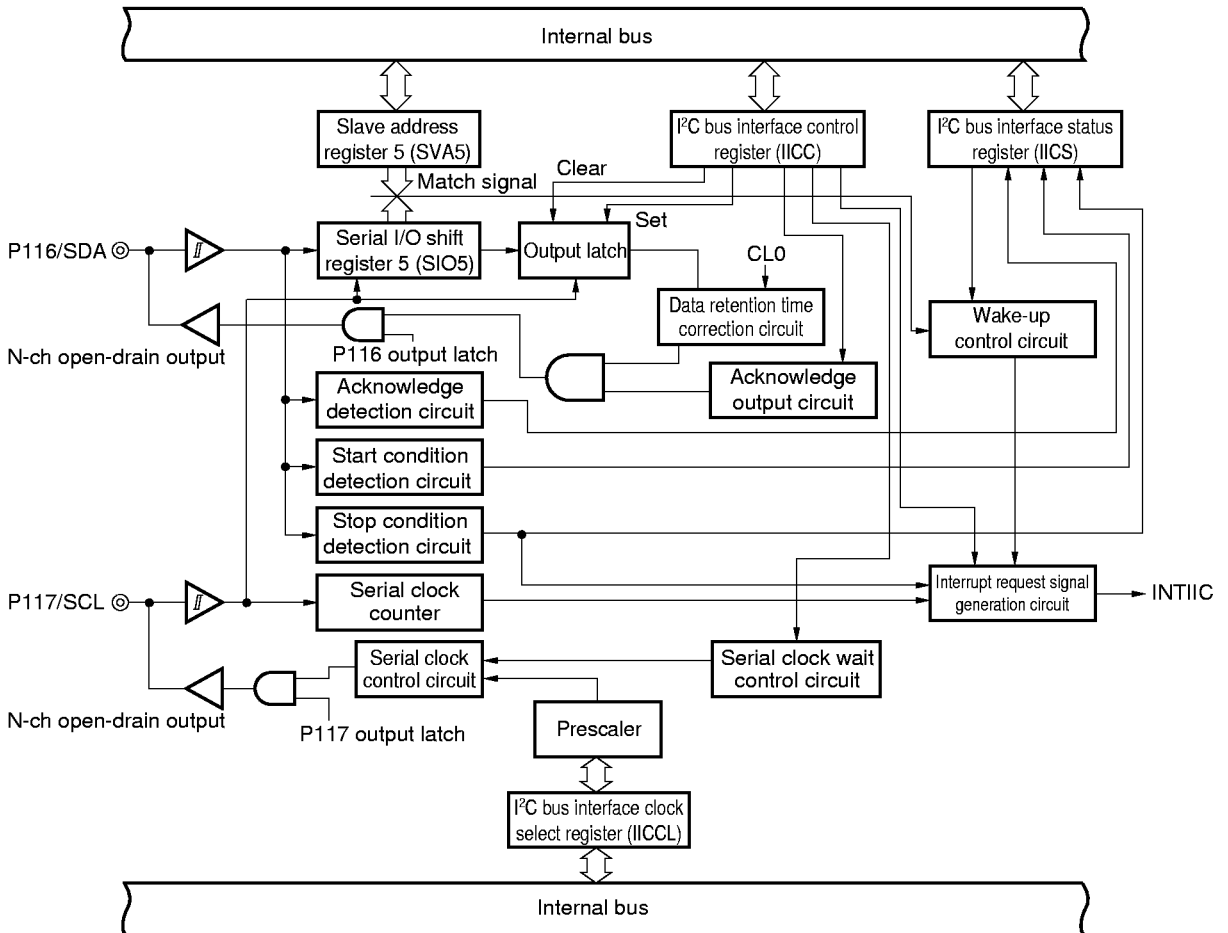


Figure 5-12. Serial Interface Channel 5 Block Diagram



6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

6.1 Interrupt Functions

A total of 21 interrupt functions are provided, divided into the following three types.

- Non-maskable : 1
- Maskable : 19
- Software : 1

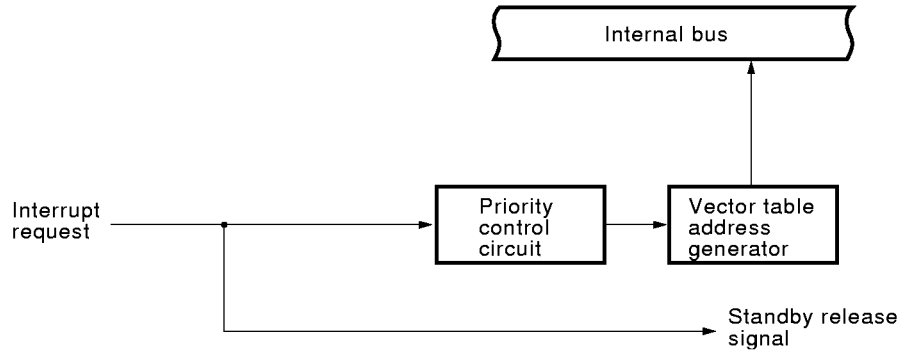
Table 6-1. List of Interrupt Factors

| Interrupt Type | Default ^{Note 1} Priority | Interrupt Factor | | Internal/ External | Vector Table Address | Basic ^{Note 2} Structure Type | | |
|----------------|------------------------------------|------------------|--------------------------------------------------------------------------------------------|--------------------|-------------------------------------------------------------|----------------------------------------|-------------------------------------------------------------------------------------------------|---------------------------------------------------|
| | | Name | Trigger | | | | | |
| Non-maskable | — | INTWDT | Overflow of watchdog timer (When the watchdog timer mode 1 is selected) | Internal | 0004H | (A) | | |
| Maskable | 0 | INTWDT | Overflow of watchdog timer (When the interval timer mode is selected) | External | 0006H 0008H 000AH 000CH 000EH 0010H 0012H | (B) | | |
| | 1 | INTP0 | Pin input edge detection | | | Internal | 0016H 001EH 0020H 0022H 0024H 0026H 0028H 002AH 002CH 002EH 0030H | (C) |
| | 2 | INTP1 | | | | | | (D) |
| | 3 | INTP2 | | | | | | |
| | 4 | INTP3 | | | | | | |
| | 5 | INTP4 | | | | | | |
| | 6 | INTP5 | | | | | | |
| | 7 | INTP6 | | | | | | |
| | 8 | INTCSI1 | | | | | | Completion of serial interface channel 1 transfer |
| | 9 | INTTM3 | Reference interval signal from watch timer | | | | | |
| | 10 | INTTM00 | Generation of matching signal of 16-bit timer register and capture/compare register (CR00) | | | | | |
| | 11 | INTTM01 | Generation of matching signal of 16-bit timer register and capture/compare register (CR01) | | | | | |
| | 12 | INTTM1 | Generation of matching signal of 8-bit timer/event counter 1 | | | | | |
| | 13 | INTTM2 | Generation of matching signal of 8-bit timer/event counter 2 | | | | | |
| | 14 | INTAD | Completion of A/D conversion | | | | | |
| | 15 | INTTM5 | Generation of matching signal of 8-bit timer/event counter 5 | | | | | |
| | 16 | INTTM6 | Generation of matching signal of 8-bit timer/event counter 6 | | | | | |
| | 17 | INTCSI4 | Completion of serial interface channel 4 transfer | | | | | |
| | 18 | INTIIC | Completion of serial interface channel 5 transfer | | | | | |
| Software | — | BRK | Execution of BRK instruction | — | 003EH | (E) | | |

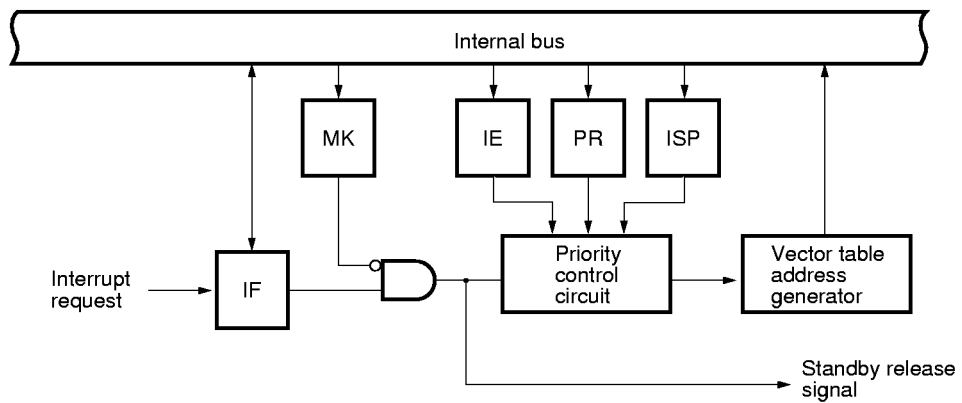
- Notes**
1. Default priority is the priority order when several maskable interruptions are generated at the same time. 0 is the highest order and 18 is the lowest order.
 2. Basic structure types (A) to (E) correspond to (A) to (E) in Figure 6-1.

Figure 6-1. Interrupt Function Basic Configuration (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0)

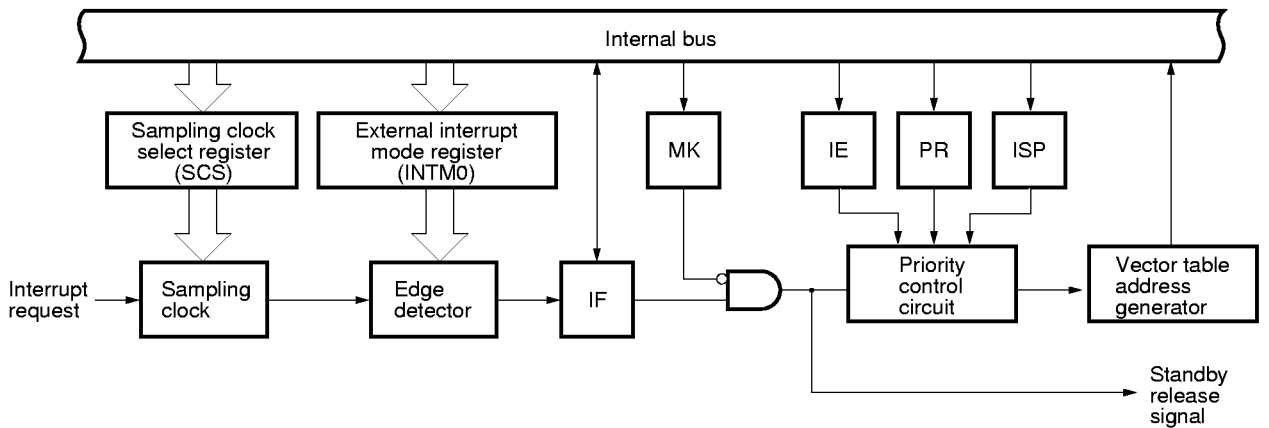
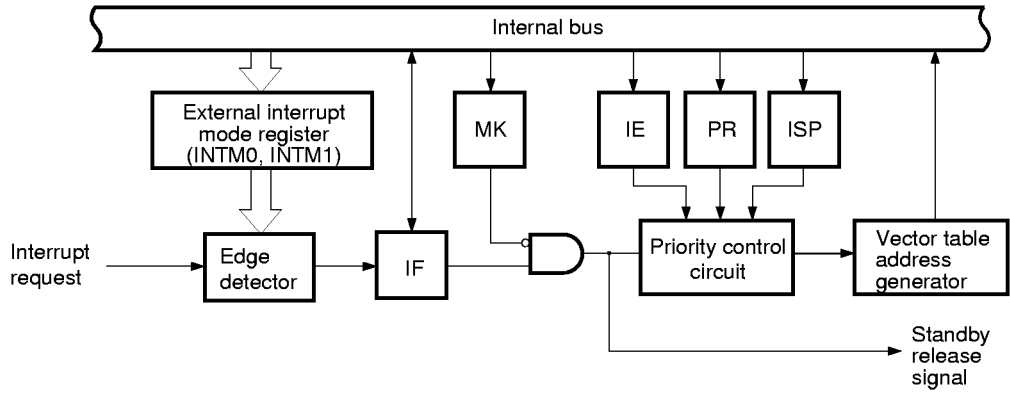
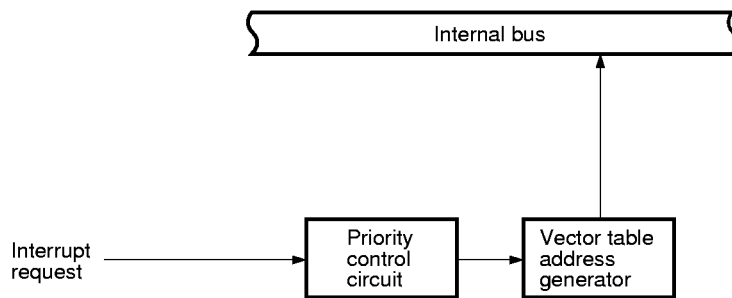


Figure 6-1. Interrupt Function Basic Configuration (2/2)

(D) External maskable interrupt (except INTP0)



(E) Software interrupt



- IF : Interrupt request flag
- E : Interrupt enable flag
- ISP : In-service priority flag
- MK : Interrupt mask flag
- PR : Priority specification flag

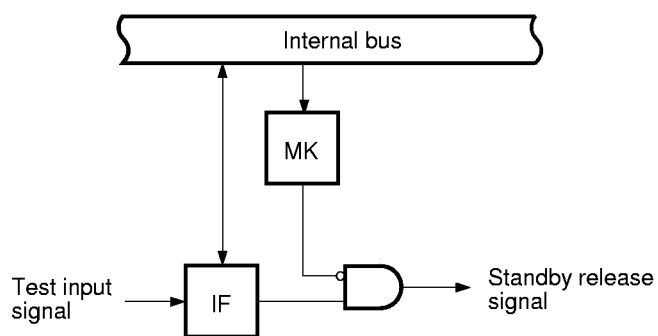
6.2 Test Functions

Table 6-2 shows the two test functions available.

Table 6-2. Test Input Factors

| Test Input Factor | | Internal/ External |
|-------------------|-------------------------------------|-----------------------|
| Name | Trigger | |
| INTWT | Overflow of watch timer | Internal |
| INTPT4 | Detection of falling edge of port 4 | External |

Figure 6-2. Basic Configuration of Test Function



IF : Test input flag
 MK : Test mask flag

7. EXTERNAL DEVICE EXPANSION FUNCTIONS

The external device expansion functions connect external devices to areas other than the internal ROM, RAM and SFR.

External devices connection uses ports 4 to 6 and port 8.

The external device expansion function has the following two modes:

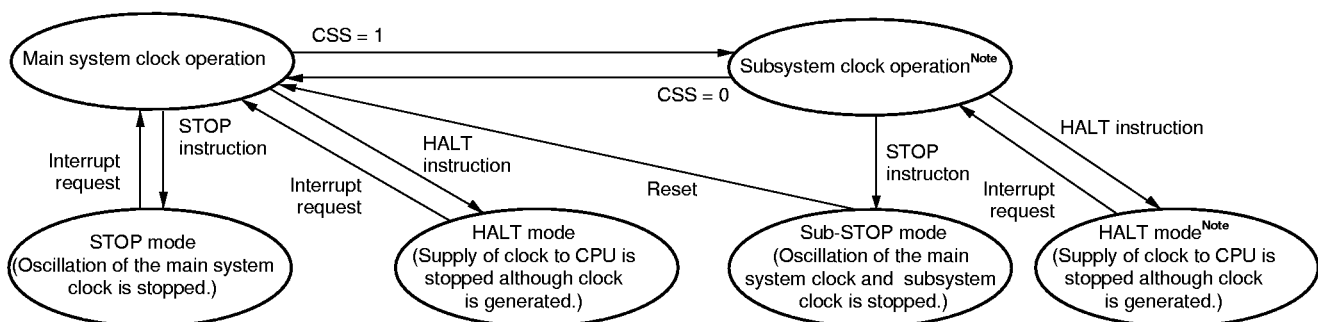
- Separate bus mode : External devices are connected by using an independent address bus and data bus. Because an external latch circuit is not necessary, this mode is effective for reducing the number of components and the mounting area on a printed wiring board.
- Multiplexed bus mode : External devices are connected by using a time-division multiplexed address/data bus. This mode is useful for reducing the number of ports used when external devices are connected.

8. STANDBY FUNCTION

The standby function intends to reduce current consumption. It has the following three modes:

- HALT mode : In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- Main STOP mode : In this mode, oscillation of the main system clock is stopped. The power consumption can be reduced because the whole internal circuit is stopped.
- Sub-STOP mode : In this mode, oscillation of the subsystem clock is stopped. The whole operation is stopped and the power is consumed very little.

Figure 8-1. Standby Function



Note Current consumption is reduced by shutting off the main system clock.
 If the CPU is operating on subsystem clock, shut off the main system clock by setting MCC. You cannot use a STOP instruction in HALT mode.

- Cautions**
1. The main stop mode can be used only when the main system clock is being operated. (The oscillation of the subsystem clock cannot be stopped.)
 2. When switching on the main system clock again after the subsystem clock has been used with the main system clock stopped, be sure to provide enough time for the generation to be stable with the program first.

9. RESET FUNCTION

There are the following two reset methods.

- External reset input by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog timer inadvertent program loop time detection

10. INSTRUCTION SET

(1) 8-bit Instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

| 2nd Operand | #byte | A | r ^{Note} | sfr | saddr | laddr16 | PSW | [DE] | [HL] | [HL + byte] [HL + B] [HL + C] | \$addr16 | 1 | None |
|-------------------------------------|--------------------------------------------------------------|---------------------------------------------------------------------|-------------------|------------|---------------------------------------------------------------------|---------------------------------------------------------------------|-----|------------|---------------------------------------------------------------------|---------------------------------------------------------------------|----------|----------------------------|--------------|
| 1st Operand | | | | | | | | | | | | | |
| A | ADD ADDC SUB SUBC AND OR XOR CMP | MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP | MOV XCH | MOV XCH | MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP | MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP | MOV | MOV XCH | MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP | MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP | | ROR ROL RORC ROLC | |
| r | MOV | MOV ADD ADDC SUB SUBC AND OR XOR CMP | | | | | | | | | | | INC DEC |
| B, C | | | | | | | | | | | DBNZ | | |
| sfr | MOV | MOV | | | | | | | | | | | |
| saddr | MOV ADD ADDC SUB SUBC AND OR XOR CMP | MOV | | | | | | | | | DBNZ | | INC DEC |
| laddr16 | | MOV | | | | | | | | | | | |
| PSW | MOV | MOV | | | | | | | | | | | PUSH POP |
| [DE] | | MOV | | | | | | | | | | | |
| [HL] | | MOV | | | | | | | | | | | ROR4 ROL4 |
| [HL + byte] [HL + B] [HL + C] | | MOV | | | | | | | | | | | |
| X | | | | | | | | | | | | | MULU |
| C | | | | | | | | | | | | | DIVUW |

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

| 1st Operand \ 2nd Operand | #word | AX | rp ^{Note} | sfrp | saddrp | !addr16 | SP | None |
|---------------------------|----------------------|----------------------|--------------------|------|--------|---------|------|-------------------------|
| AX | ADDW SUBW CMPW | | MOVW XCHW | MOVW | MOVW | MOVW | MOVW | |
| rp | MOVW | MOVW ^{Note} | | | | | | INCW, DECW PUSH, POP |
| sfrp | MOVW | MOVW | | | | | | |
| saddrp | MOVW | MOVW | | | | | | |
| !addr16 | | MOVW | | | | | | |
| SP | MOVW | MOVW | | | | | | |

Note Only when rp = BC, DE, HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

| 1st Operand \ 2nd Operand | A.bit | sfr.bit | saddr.bit | PSW.bit | [HL].bit | CY | \$addr16 | None |
|---------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|------|-------------------|----------------------|
| A.bit | | | | | | MOV1 | BT BF BTCLR | SET1 CLR1 |
| sfr.bit | | | | | | MOV1 | BT BF BTCLR | SET1 CLR1 |
| saddr.bit | | | | | | MOV1 | BT BF BTCLR | SET1 CLR1 |
| PSW.bit | | | | | | MOV1 | BT BF BTCLR | SET1 CLR1 |
| [HL].bit | | | | | | MOV1 | BT BF BTCLR | SET1 CLR1 |
| CY | MOV1 AND1 OR1 XOR1 | MOV1 AND1 OR1 XOR1 | MOV1 AND1 OR1 XOR1 | MOV1 AND1 OR1 XOR1 | MOV1 AND1 OR1 XOR1 | | | SET1 CLR1 NOT1 |

(4) Call instructions/Branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

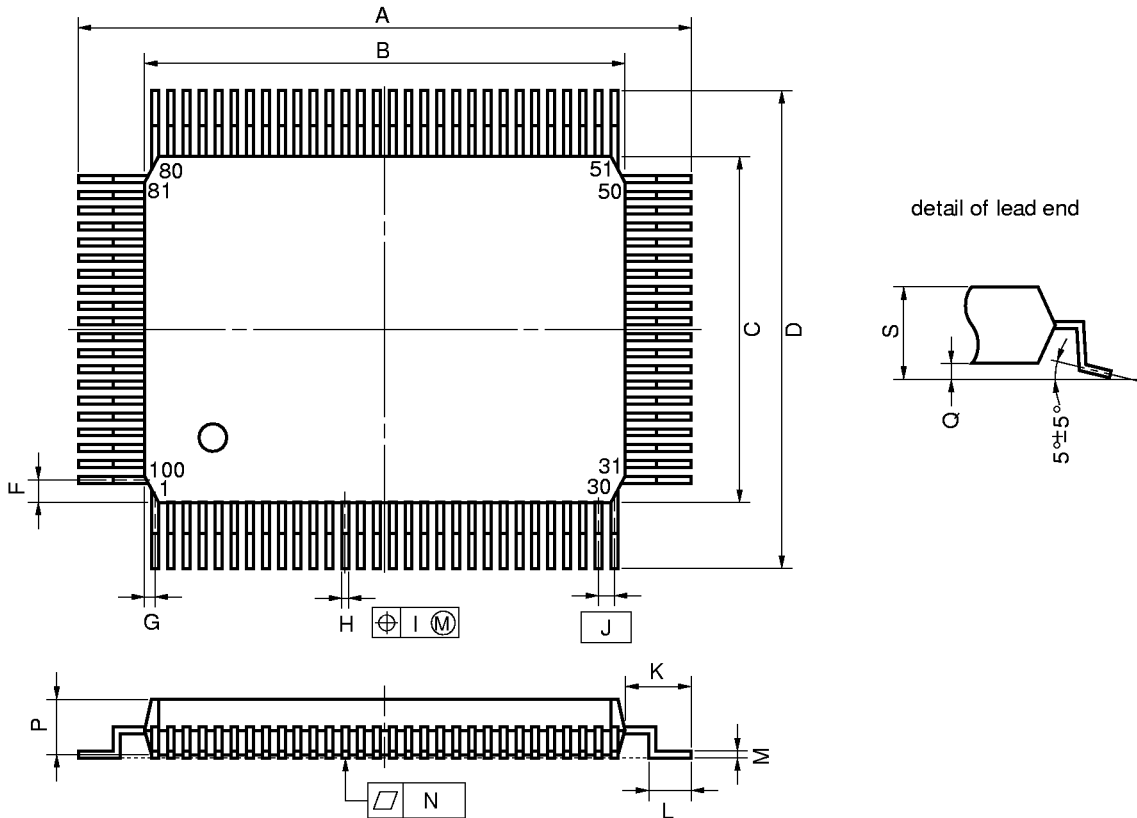
| 1st Operand \ 2nd Operand | AX | !addr16 | !addr11 | [addr5] | \$addr16 |
|---------------------------|----|------------|---------|---------|--------------------------|
| Basic instruction | BR | CALL BR | CALLF | CALLT | BR, BC BNC BZ, BNZ |
| Compound instruction | | | | | BT, BF BTCLR DBNZ |

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

11. PACKAGE DRAWINGS

100 PIN PLASTIC QFP (14 × 20)



NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

P100GF-65-3BA1-2

| ITEM | MILLIMETERS | INCHES |
|------|----------------------------------------|-------------------------------------------|
| A | 23.6±0.4 | 0.929±0.016 |
| B | 20.0±0.2 | 0.795 ^{+0.009} _{-0.008} |
| C | 14.0±0.2 | 0.551 ^{+0.009} _{-0.008} |
| D | 17.6±0.4 | 0.693±0.016 |
| F | 0.8 | 0.031 |
| G | 0.6 | 0.024 |
| H | 0.30±0.10 | 0.012 ^{+0.004} _{-0.005} |
| I | 0.15 | 0.006 |
| J | 0.65 (T.P.) | 0.026 (T.P.) |
| K | 1.8±0.2 | 0.071 ^{+0.008} _{-0.009} |
| L | 0.8±0.2 | 0.031 ^{+0.009} _{-0.008} |
| M | 0.15 ^{+0.10} _{-0.05} | 0.006 ^{+0.004} _{-0.003} |
| N | 0.10 | 0.004 |
| P | 2.7 | 0.106 |
| Q | 0.1±0.1 | 0.004±0.004 |
| S | 3.0 MAX. | 0.119 MAX. |

APPENDIX A. DEVELOPMENT TOOLS

The following tools are available for system development using the μPD780016Y and 780018Y.

Language Processing Software

| | |
|-----------------------------------------|--------------------------------------------------------------------|
| RA78K/0 ^{Notes 1, 2, 3, 4} | Assembler package used in common for the 78K/0 series |
| CC78K/0 ^{Notes 1, 2, 3, 4} | C compiler package used in common for the 78K/0 series |
| DF780018 ^{Notes 1, 2, 3, 4, 8} | Device file used in common for the μPD780018 subseries |
| CC78K/0-L ^{Notes 1, 2, 3, 4} | C compiler library source file used in common for the 78K/0 series |

PROM Writing Tools

| | |
|--------------------------------------------------------------------|---------------------------------------------|
| PG-1500 | PROM programmer |
| PA-78P0018GF ^{Note 8} PA-78P0018KL-T ^{Note 8} | Programmer adapter connected to the PG-1500 |
| PG-1500 controller ^{Notes 1, 2} | Control program for the PG-1500 |

Debugging Tools

| | |
|-----------------------------------------------|------------------------------------------------------------------------------------------|
| IE-78000-R | In-circuit emulator used in common for the 78K/0 series |
| IE-78000-R-A ^{Note 8} | In-circuit emulator used in common for the 78K/0 series (for integrated debugger) |
| IE-78000-R-BK | Break board used in common for the 78K/0 series |
| IE-780018-R-EM ^{Note 8} | Emulation board used in common for the μPD780018 subseries |
| EP-78064GF-R | Emulation probe used in common for the μPD78064 subseries |
| EV-9200GF-100 | Socket mounted on the target system board prepared for 100-pin plastic QFP (GF-3BA type) |
| EV-9900 | Tool used for removing the μPD78P0018YKL-T from the EV-9200GF-100. |
| SM78K0 ^{Notes 5, 6, 7} | System simulator used in common for the 78K/0 series |
| ID78K0 ^{Notes 4, 5, 6, 7, 8} | Integrated debugger for IE-78000-R-A |
| SD78K/0 ^{Notes 1, 2} | Screen debugger for the IE-78000-R |
| DF780018 ^{Notes 1, 2, 4, 5, 6, 7, 8} | Device file used in common for the μPD780018 subseries |

Real-Time OS

| | |
|-------------------------------------|----------------------------------------|
| RX78K/0 ^{Notes 1, 2, 3, 4} | Real-time OS used for the 78K/0 series |
| MX78K0 ^{Notes 1, 2, 3, 4} | OS used for the 78K/0 series |

Fuzzy Inference Development Support System

| | |
|----------------------------------------------------|------------------------------------|
| FE9000 ^{Note 1} /FE9200 ^{Note 6} | Fuzzy knowledge data creating tool |
| FT9080 ^{Note 1} /FT9085 ^{Note 2} | Translator |
| FI78K0 ^{Notes 1, 2} | Fuzzy inference module |
| FD78K0 ^{Notes 1, 2} | Fuzzy inference debugger |

- Notes**
1. Based on PC-9800 series (MS-DOS™)
 2. Based on IBM PC/AT™ and compatible machines (PC DOS™/IBM DOS™/MS-DOS)
 3. Based on HP9000 series 300™ (HP-UX™)
 4. Based on HP9000 series 700™ (HP-UX), SPARCstation™ (SunOS™), and EWS-4800 series (EWS-UX/V)
 5. Based on PC-9800 series (MS-DOS + Windows™)
 6. Based on IBM PC/AT and compatible machines (PC DOS/IBM DOS/MS DOS + Windows)
 7. Based on NEW™ (NEWS-OS™)
 8. Under development

- Remarks**
1. For development tools supplied by third-party manufacturers, refer to **78K/0 Series Selection Guide** (U11126E).
 2. Use the RA78K/0, CC78K/0, SM78K0, ID78K0, SD78K/0, and RX78K/0 in combination with the DF780018.

APPENDIX B. RELATED DOCUMENTS

Documents Related to Devices

| Document | Document No. | |
|------------------------------------------------------|----------------|----------------|
| | Japanese | English |
| μPD780018Y, 780018Y Subseries User's Manual | U11754J | To be prepared |
| μPD780016Y, 780018Y Preliminary Product Information | U11810J | This document |
| μPD78P0018Y Preliminary Product Information | U11603J | To be prepared |
| 78K/0 Series User's Manual-Instruction | IEU-849 | IEU-1372 |
| 78K/0 Series Instruction Table | U10903J | — |
| 78K/0 Series Instruction Set | U10904J | — |
| μPD780018Y Subseries Special-Function Register Table | To be prepared | — |

Documents on Development Tools (User's Manuals)

| Document | | Document No. | |
|-------------------------------------------------|------------------------------------------------------|--------------|----------------|
| | | Japanese | English |
| RA78K Series Assembler Package | Operation | EEU-809 | EEU-1399 |
| | Language | EEU-815 | EEU-1404 |
| RA78K Series Structured Assembler Preprocessor | | EEU-817 | EEU-1402 |
| CC78K Series C Compiler | Operation | EEU-656 | EEU-1280 |
| | Language | EEU-655 | EEU-1284 |
| CC78K0 C Compiler | Operation | U11517J | — |
| | Language | U11518J | — |
| CC78K/0 C Compiler Application Note | Programing Know-how | EEA-618 | EEA-1208 |
| CC78K Series Library Source File | | EEU-777 | — |
| PG-1500 PROM Programmer | | EEU-651 | EEU-1335 |
| PG-1500 Controller PC-9800 Series (MS-DOS) Base | | EEU-704 | EEU-1291 |
| PG-1500 Controller IBM PC Series (PC-DOS) Base | | EEU-5008 | U10540E |
| IE-78000-R | | EEU-810 | U11376E |
| IE-78000-R-A | | U10057J | U10057E |
| IE-78000-R-BK | | EEU-867 | EEU-1427 |
| IE-780018-R-EM | | U11838J | To be prepared |
| EP-78064 | | EEU-934 | EEU-1469 |
| SM78K0 System Simulator Windows Base | Reference | U10181J | U10181E |
| SM78K Series System Simulator | External component user open interface specification | U10092J | U10092E |
| ID78K0 Integrated Debugger EWS Base | Reference | U11151J | — |
| ID78K0 Integrated Debugger PC Base | Reference | U11539J | — |
| ID78K0 Integrated Debugger Windows Base | Guide | U11649J | — |
| SD78K/0 Screen Debugger | Introduction | EEU-852 | — |
| PC-9800 Series (MS-DOS) Base | Reference | U10952J | — |
| SD78K/0 Screen Debugger | Introduction | EEU-5024 | EEU-1414 |
| IBM PC/AT (PC DOS) Base | Reference | U11279J | EEU-1413 |

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Documents on Embedded Software (User's Manuals)

| Document | | Document No. | |
|-------------------------------------------------------------------------------------|--------------|--------------|----------|
| | | Japanese | English |
| 78K/0 Series Real-time OS | Basic | U11537J | — |
| | Installation | U11536J | — |
| | Technical | U11538J | — |
| 78K/0 Series OS MX78K0 | Fundamental | EEU-5010 | — |
| Fuzzy Knowledge Data Creation Tool | | EEU-829 | EEU-1438 |
| 78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator | | EEU-862 | EEU-1444 |
| 78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module | | EEU-858 | EEU-1441 |
| 78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger | | EEU-921 | EEU-1458 |

Other Documents

| Document | Document No. | |
|----------------------------------------------------------------|--------------|----------|
| | Japanese | English |
| IC Package Manual | C10943X | |
| Semiconductor Device Mounting Technology Manual | C10535J | C10535E |
| Quality Grade on NEC Semiconductor Devices | C11531J | C11531E |
| NEC Semiconductor Device Reliability/Quality Control System | U10983J | U10983E |
| Electrostatic Discharge (ESD) Test | MEM-539 | — |
| Semiconductor Device Quality Assurance Guide | MEI-603 | MEI-1202 |
| Microcontroller-Related Product Guide – Third Party Products – | U11416J | — |

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