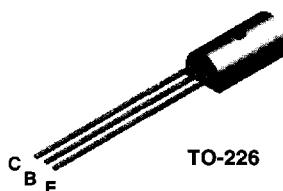




TN3467A



TO-226

PNP Switching Transistor

This device is designed for high speed saturated switching applications at currents to 800 mA. Sourced from Process 70.

Absolute Maximum Ratings*

TA = 25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	40	V
V_{EBO}	Emitter-Base Voltage	5.0	V
I_C	Collector Current - Continuous	1.2	A
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

* These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

NOTES:

- 1) These ratings are based on a maximum junction temperature of 150 degrees C.
- 2) These are steady state limits. The factory should be consulted on applications involving pulsed or low duty cycle operations.
- 3) All voltages (V) and currents (A) are negative polarity for PNP transistors.

Thermal Characteristics

TA = 25°C unless otherwise noted

Symbol	Characteristic	Max	Units
		TN3467A	
P_D	Total Device Dissipation Derate above 25°C	1.0 8.0	W mW/°C
R_{eJC}	Thermal Resistance, Junction to Case	125	°C/W
R_{eJA}	Thermal Resistance, Junction to Ambient	50	°C/W

PNP Switching Transistor

(continued)

Electrical Characteristics

TA = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Max	Units
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OFF CHARACTERISTICS

$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage*	$I_C = 10 \text{ mA}, I_B = 0$	40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 10 \mu\text{A}, I_E = 0$	40		V
$V_{(BRI)EBO}$	Emitter-Base Breakdown Voltage	$I_E = 10 \mu\text{A}, I_C = 0$	5.0		V
I_{BEV}	Base-Cutoff Current	$V_{CE} = 30 \text{ V}, V_{BE} = 3.0 \text{ V}$		120	nA
I_{CEX}	Collector-Cutoff Current	$V_{CE} = 30 \text{ V}, V_{BE} = 3.0 \text{ V}$		100	nA
I_{CBO}	Collector-Cutoff Current	$V_{CB} = 30 \text{ V}, I_E = 0$ $V_{CE} = 30 \text{ V}, I_E = 0, T_A = 150^\circ\text{C}$		0.01 15	μA μA

ON CHARACTERISTICS*

h_{FE}	DC Current Gain	$I_C = 150 \text{ mA}, V_{CE} = 1.0 \text{ V}$ $I_C = 500 \text{ mA}, V_{CE} = 1.0 \text{ V}$ $I_C = 1.0 \text{ A}, V_{CE} = 5.0 \text{ V}$	40	120	
$V_{CE(\text{sat})}$	Collector-Emitter Saturation Voltage	$I_C = 150 \text{ mA}, I_B = 15 \text{ mA}$ $I_C = 500 \text{ mA}, I_B = 50 \text{ mA}$ $I_C = 1.0 \text{ A}, I_B = 100 \text{ mA}$		0.3 0.5 1.0	V
$V_{BE(\text{sat})}$	Base-Emitter Saturation Voltage	$I_C = 150 \text{ mA}, I_B = 15 \text{ mA}$ $I_C = 500 \text{ mA}, I_B = 50 \text{ mA}$ $I_C = 1.0 \text{ A}, I_B = 100 \text{ mA}$		1.0 1.2 1.6	V

SMALL SIGNAL CHARACTERISTICS

f_T	Current Gain-Bandwidth Product	$I_C = 50 \text{ mA}, V_{CE} = 10 \text{ V}, f = 100 \text{ MHz}$	175		MHz
C_{obo}	Output Capacitance	$V_{CB} = 10 \text{ V}, I_E = 0, f = 1.0 \text{ kHz}$		25	pF
C_{ibo}	Input Capacitance	$V_{BE} = 0.5 \text{ V}, I_C = 0, f = 1.0 \text{ kHz}$		100	pF

SWITCHING CHARACTERISTICS

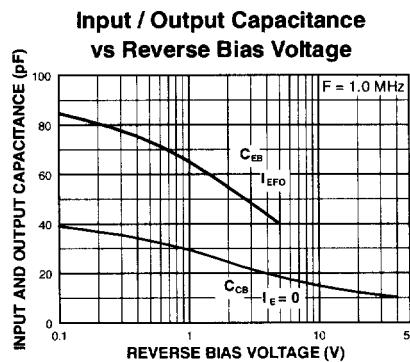
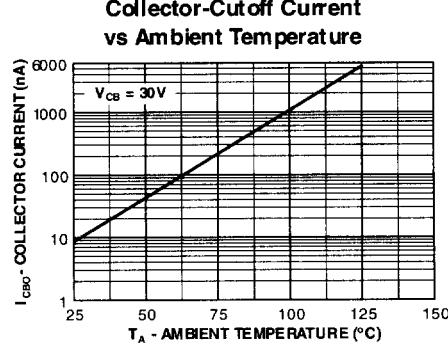
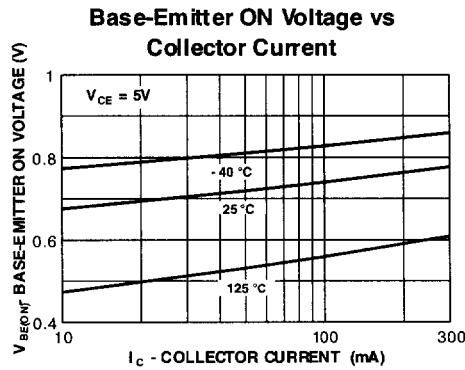
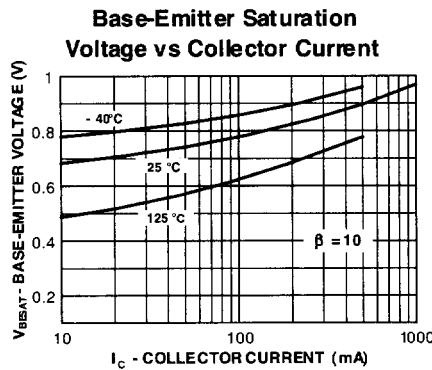
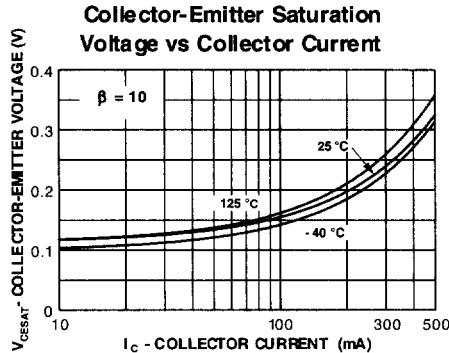
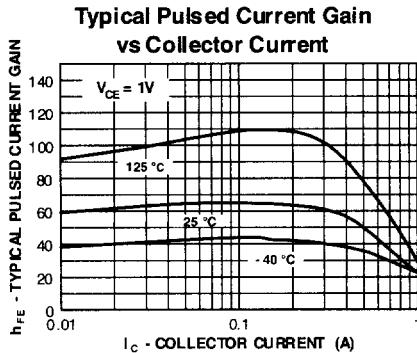
t_d	Delay Time	$V_{CC} = 30 \text{ V}, V_{BE} = 2.0 \text{ V},$		10	ns
t_r	Rise Time	$I_C = 500 \text{ mA}, I_{B1} = 50 \text{ mA}$		30	ns
t_s	Storage Time	$V_{CC} = 30 \text{ V}, I_C = 500 \text{ mA},$		60	ns
t_f	Fall Time	$I_{B1} = I_{B2} = 50 \text{ mA}$		30	ns

* Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 1.0\%$

NOTE: All voltages (V) and currents (A) are negative polarity for PNP transistors.

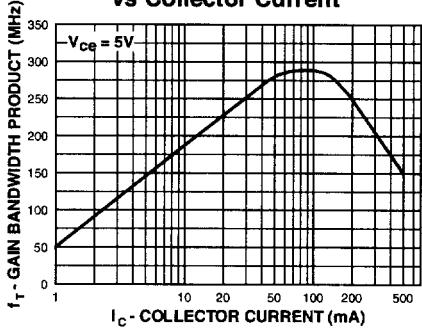
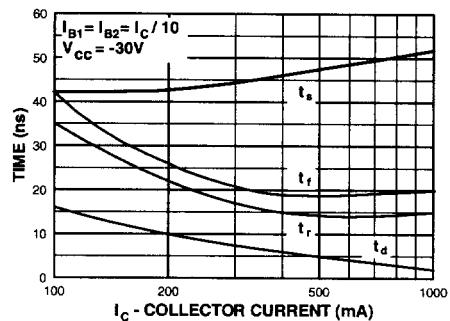
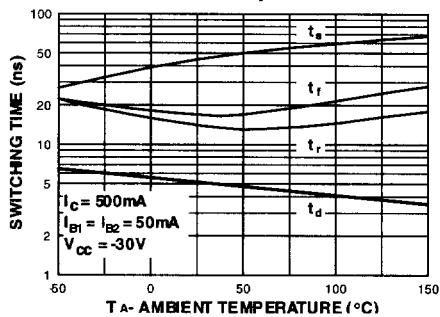
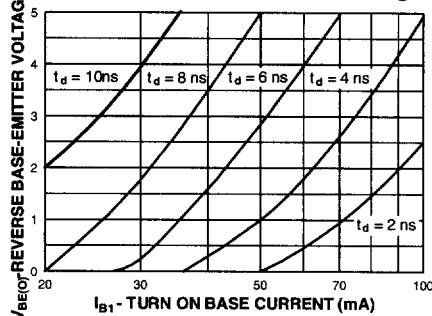
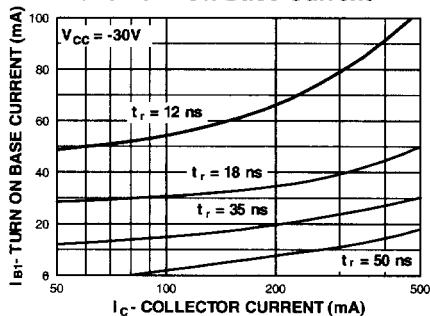
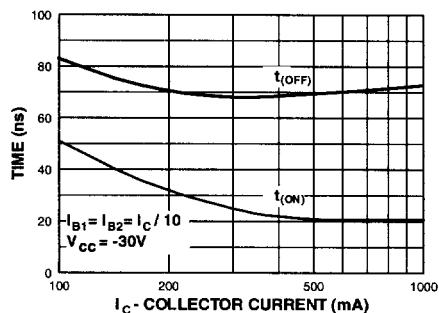
PNP Switching Transistor

(continued)

Typical Characteristics

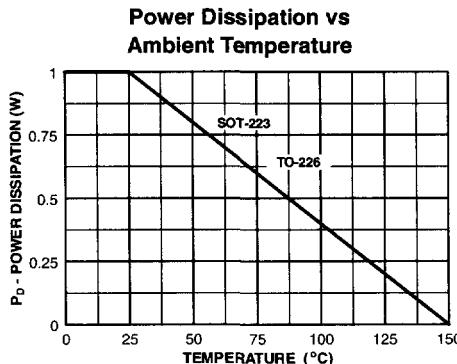
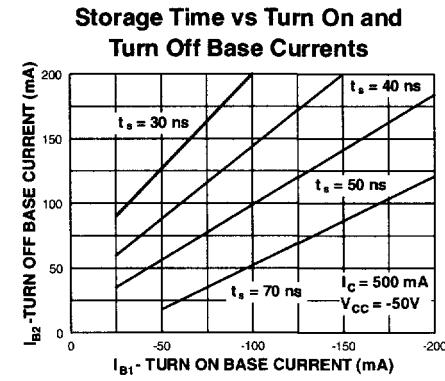
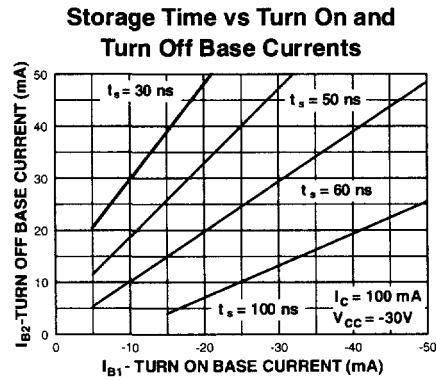
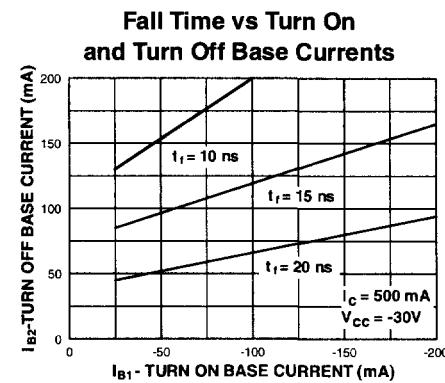
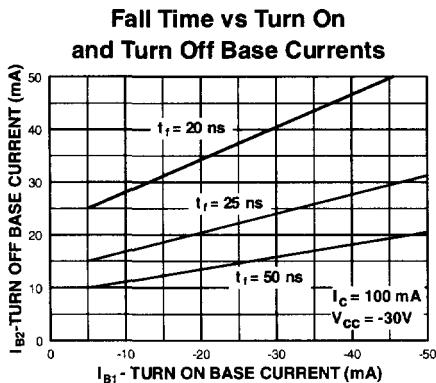
PNP Switching Transistor

(continued)

Typical Characteristics (continued)**Gain Bandwidth Product vs Collector Current****Switching Times vs Collector Current****Switching Times vs Ambient Temperature****Delay Time vs Turn On Base Current and Reverse Bias Emitter Voltage****Rise Time vs Collector Current and Turn On Base Current****Turn On / Turn Off Times vs Collector Current**

PNP Switching Transistor

(continued)

Typical Characteristics (continued)

PNP Switching Transistor

(continued)

Test Circuits

$PW = 200 \text{ ns}$
 $\text{Rise Time} \leq 2.0 \text{ ns}$
 $\text{Duty Cycle} = 2\%$

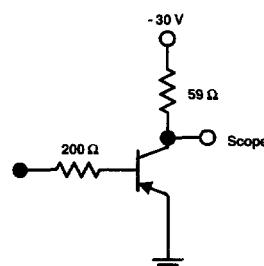
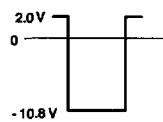


FIGURE 1: t_{ON} Equivalent Test Circuit

$2.0 < t_1 < 500 \mu\text{s}$
 $t_2 < 5 \text{ ns}$
 $t_3 > 1.0 \mu\text{s}$
 $\text{Duty Cycle} = 2\%$

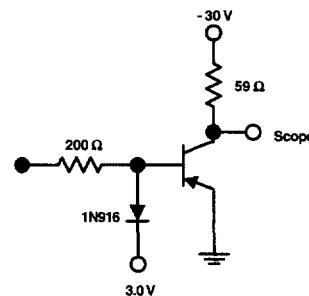
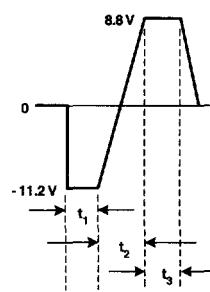


FIGURE 2: t_{OFF} Equivalent Test Circuit