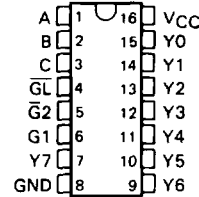


SN54HCT237, SN74HCT237 3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

D2804, MARCH 1984—REVISED JUNE 1989

- Inputs are TTL-Voltage Compatible
- Combines Decoder and 3-Bit Address Latch
- Incorporates 2 Output Enables to Simplify Cascading
- Package Options Include Ceramic Chip Carriers and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

SN54HCT237 . . . J PACKAGE
SN74HCT237 . . . N PACKAGE
(TOP VIEW)

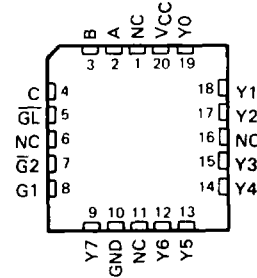


description

The 'HCT237 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input ($\overline{GL}$) is low, the 'HCT237 acts as a decoder/demultiplexer. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as $\overline{GL}$ remains high. The output enable controls, G1 and $\overline{G2}$, control the outputs independently of the select or latch-enable inputs. All of the outputs are forced low if G1 is low or $\overline{G2}$ is high. The 'HCT237 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

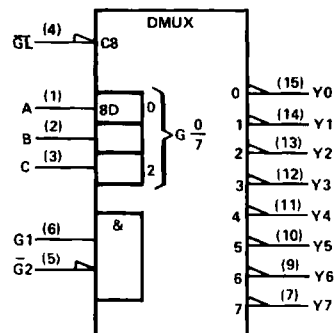
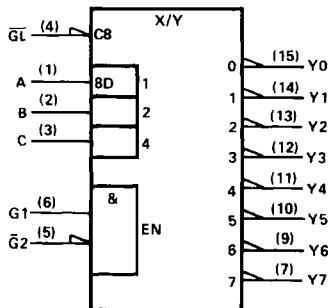
The SN54HCT237 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HCT237 is characterized for operation from -40°C to 85°C .

SN54HCT237 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

logic symbols (alternatives)[†]



[†]These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for J and N packages.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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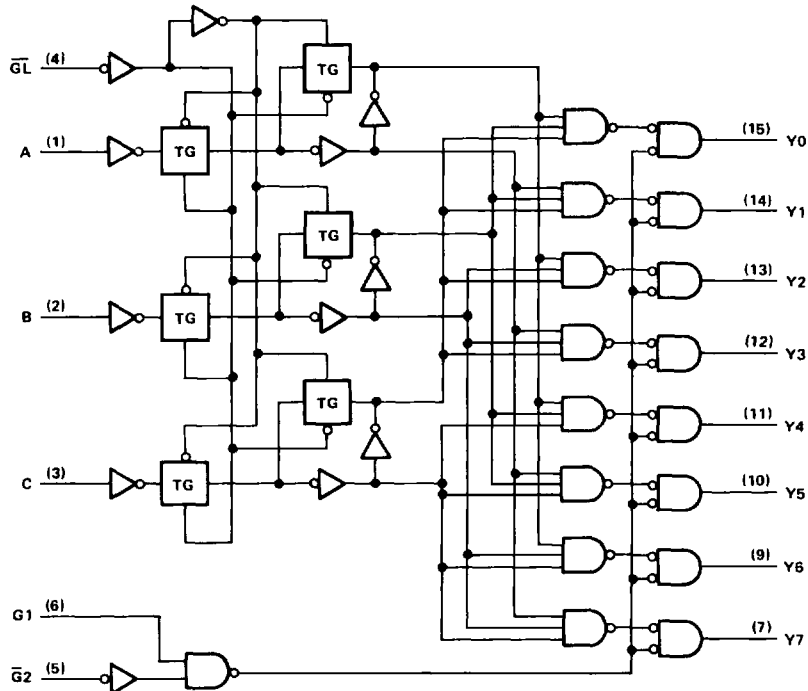
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SN54HCT237, SN74HCT237
3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

logic diagram (positive logic)



Pin numbers shown are for J and N packages.

FUNCTION TABLE

ENABLE			SELECT			OUTPUTS							
$\overline{G1}$	$G1$	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	H	L	L	L	L	L	L	H	L	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

SN54HCT237, SN74HCT237

3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS

WITH ADDRESS LATCHES

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	-0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 25 mA
Continuous current through V_{CC} or GND pins	± 50 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or J package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: N package	260°C
Storage temperature range	-65°C to 150°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54HCT237			SN74HCT237			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 4.5$ V to 5.5 V			2			V
V_{IL}	Low-level input voltage	$V_{CC} = 4.5$ V to 5.5 V			0			V
V_I	Input voltage	0			V_{CC}			V
V_O	Output voltage	0			V_{CC}			V
t_t	Input transition (rise and fall) times	0			500			ns
T_A	Operating free-air temperature	-55			125			°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			SN54HCT237		SN74HCT237		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -20$ μA	4.5 V	4.4	4.499		4.4		4.4		V
	$V_I = V_{IH}$ or V_{IL} , $I_{OH} = -4$ mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 20$ μA	4.5 V		0.001	0.1		0.1		0.1	V
	$V_I = V_{IH}$ or V_{IL} , $I_{OL} = 4$ mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	$V_I = V_{CC}$ or 0	5.5 V	± 0.1 ± 100			± 1000		± 1000		nA
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$	5.5 V	8			160		80		μA
$\Delta I_{CC}^\dagger$	One input at 0.5 V or 2.4 V, Other inputs at 0 V or V_{CC}	5.5 V	1.4			2.4	3.0	2.9		mA
C_i		4.5 to 5.5 V	3			10	10	10		pF

†This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC} .

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HCMOS Devices

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SN54HCT237, SN74HCT237 **3-LINE TO 8-LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES**

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

	V _{CC}	T _A = 25°C		SN54HCT237		SN74HCT237		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w Pulse duration, $\overline{\text{GL}}$ low	4.5 V 5.5 V	26 23		39 35		33 30		ns
t _{su} Setup time, A, B, and C before $\overline{\text{GL}}$ †	4.5 V 5.5 V	15 14		23 21		19 17		ns
t _h Hold time, A, B, and C after $\overline{\text{GL}}$ †	4.5 V 5.5 V	5 5		5 5		5 5		ns

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HCT237		SN74HCT237		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A, B, C	Any	4.5 V 5.5 V		24 20	38 34		57 51		48 43	ns
t _{pd}	$\overline{\text{G}}_2$	Any	4.5 V 5.5 V		19 16	29 26		44 40		36 32	ns
t _{pd}	G1	Any	4.5 V 5.5 V		19 16	29 26		44 40		36 32	ns
t _{pd}	$\overline{\text{GL}}$	Any	4.5 V 5.5 V		29 25	42 36		63 57		52 47	ns
t _t		Any	4.5 V 5.5 V		12 11	15 14		22 20		19 17	ns

C _{pd}	Power dissipation capacitance	No load, T _A = 25°C	85 pF typ
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NOTE 1: Load circuit and voltage waveforms are shown in Section 1.