HARRIS

IRFR120/IRFR121
IRFU120/IRFU121

N-Channel Power MOSFETs
Avalanche-Energy-Rated

August 1991

Features

- 8.4A, 80V and 100V
- $r_{DS(on)} = 0.27\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Description

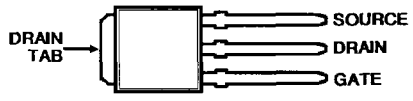
The IRFR120, IRFR121, IRFU120, IRFU121 are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. These are n-channel enhancement-mode silicon gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFU series is supplied in the TO-251AA plastic package and the IRFR series is supplied in the TO-252AA surface-mount plastic package.

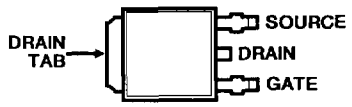
Because of space limitations branding (marking) on type IRFR120 is IRF120, IRFR121 is IFR121, IRFU120 is IFU120 and IRFU121 is IFU121.

Packages

TO-251AA
TOP VIEW

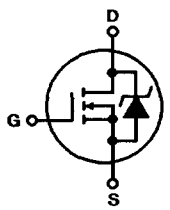


TO-252AA
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = 25^oC$) Unless Otherwise Specified

Gate-Source Voltage, V_{GS}	±20V
Continuous Drain Current, I_D	
$T_C = 25^oC$	8.4A
$T_C = 100^oC$	5.9A
Pulsed Drain Current (1), I_{DM}	34A
Single-Pulse Avalanche Energy Rating (2), E_{AS} (See Figure 14)	36mJ
Maximum Power Dissipation, P_D	50W
Linear Derating Factor	0.4W/°C
Operating and Storage Junction Temperature Range, T_J, T_{STG}	-55 to +175°C
Maximum Lead Temperature for Soldering, T_L (0.063" (1.6mm) from case for 10s)	300°C

NOTES:

1. Repetitive Rating: Pulse width limited by max. junction temperature. See Transient Thermal Impedance Curve (Figure 5)
2. V_{DD} = 25V, Start T_J = +25°C, L = 770µH, $R_G = 25\Omega$, Peak I_L = 8.4A (See Figures 14 and 15)
3. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
4. Mounting pad must cover heatsink surface area. See Packages.

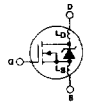
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **2414**

ELECTRICAL CHARACTERISTICS, At T_J = 25°C (Unless Otherwise Specified)

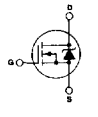
CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Breakdown Voltage	IRFR120, IRFU120	100	—	—	V	V_{GS} = 0 V, I_D = 250 μA
		IRFR121, IRFU121	80				
$R_{DS}(on)$	Static Drain-to-Source On-State Resistance ③	ALL	—	0.25	0.27	Ω	V_{GS} = 10 V, I_D = 5.9 A
$I_D(on)$	On-State Drain Current ③	ALL	8.4	—	—	A	$V_{DS} > I_D(on) \times R_{DS}(on)$ Max. V_{GS} = 10 V
$V_{GS}(th)$	Gate Threshold Voltage	ALL	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250 μA
g_{fs}	Forward Transconductance ③	ALL	2.8	4.2	—	S(℧)	$V_{DS} \geq 50$ V, I_{DS} = 5.9 A
I_{DSS}	Zero-Gate Voltage Drain Current	ALL	—	—	250	μA	V_{DS} = Max. Rating, V_{GS} = 0 V
			—	—	1000		V_{DS} = 0.8 x Max. Rating V_{GS} = 0 V, T_J = 150°C
I_{GSS}	Gate-to-Source Leakage Forward	ALL	—	—	500	nA	V_{GS} = 20 V
I_{GSS}	Gate-to-Source Leakage Reverse	ALL	—	—	-500		V_{GS} = -20 V
Q_g	Total Gate Charge	ALL	—	9.7	15	nC	V_{GS} = 10 V, I_D = 8.4 A
Q_{gs}	Gate-to-Source Charge	ALL	—	2.2	3.3		V_{DS} = 0.8 x Max. Rating
Q_{gd}	Gate-to-Drain ("Miller") Charge		—	2.3	3.4		See Fig. 16. (Independent of operating temperature)
$t_d(on)$	Turn-On Delay Time	ALL	—	8.8	13	ns	V_{DD} = 50 V, $I_D \approx$ 8.4 A, R_G = 18 Ω
t_r	Rise Time	ALL	—	30	45		R_D = 5.1 Ω
$t_d(off)$	Turn-Off Delay Time	ALL	—	19	29		See Fig. 15
t_f	Fall Time	ALL	—	20	30		(Independent of operating temperature)
L_D	Internal Drain Inductance	ALL	—	4.5	—	nH	Measured from the drain lead, 6mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	—	7.5	—	nH	Measured from the source lead, 6mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	ALL	—	350	—	pF	V_{GS} = 0 V, V_{DS} = 25 V
C_{oss}	Output Capacitance	ALL	—	130	—		f = 1.0 MHz
C_{rss}	Reverse Transfer Capacitance	ALL	—	24	—		See Fig. 10

Modified MOSFET symbol showing the internal inductances.



SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

CHARACTERISTIC		TYPE	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
I_S	Continuous Source Current (Body Diode)	ALL	—	—	8.4	A	Modified MOSFET symbol showing the integral reverse p-n junction rectifier.
I_{SM}	Pulsed Source Current (Body Diode) ①	ALL	—	—	34		
V_{SD}	Diode Forward Voltage ③	ALL	—	—	2.5	V	T_J = 25°C, I_S = 8.4 A, V_{GS} = 0 V
t_{rr}	Reverse Recovery Time	ALL	55	110	240	ns	T_J = 25°C, I_F = 8.4 A, di/dt = 100 A/μs
Q_{RR}	Reverse Recovery Charge	ALL	0.25	0.53	1.1	μC	
t_{on}	Forward Turn-On Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				



THERMAL RESISTANCE

$R_{\theta JC}$	Junction-to-Case	ALL	—	—	3.0	°C/W	
$R_{\theta CS}$	Case-to-Sink	ALL	—	1.7	—		Typical solder mount ④
$R_{\theta JA}$	Junction-to-Ambient	ALL	—	—	110		Typical socket mount

① Repetitive Rating; Pulse width limited by maximum junction temperature (see Fig. 5).

② At V_{DD} = 25 V, Starting T_J = 25°C, L = 770 μH, R_G = 25 Ω, Peak I_L = 8.4 A.

③ Pulse Width ≤ 300 μs; Duty Cycle ≤ 2%.

④ Mounting pad must cover heatsink surface area. See Case Style drawing on front page.

The information shown on the following graphs applies also to the IRFU devices.

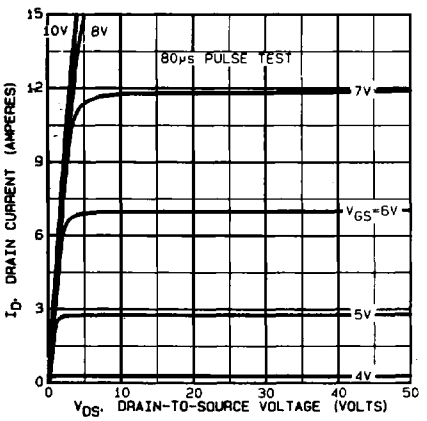


Fig. 1 - Typical output characteristics.

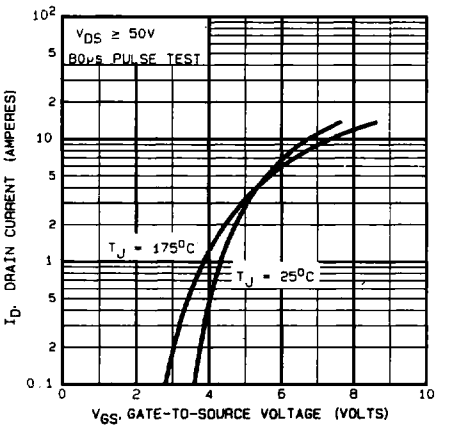


Fig. 2 - Typical transfer characteristics.

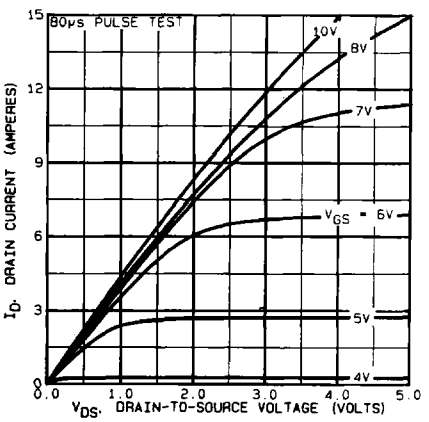


Fig. 3 - Typical saturation characteristics.

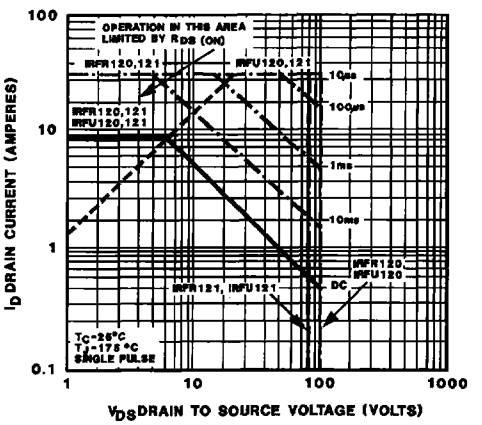


Fig. 4 - Maximum safe operating area.

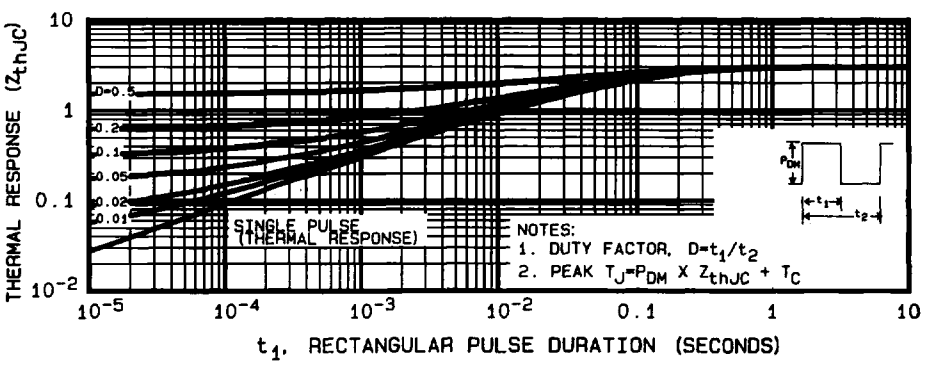


Fig. 5 - Maximum effective transient thermal impedance, junction-to-case vs. pulse duration.

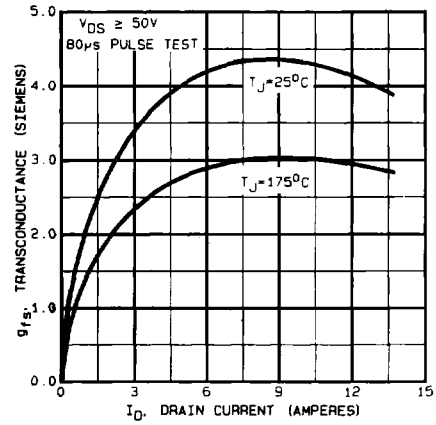


Fig. 6 - Typical transconductance vs. drain current.

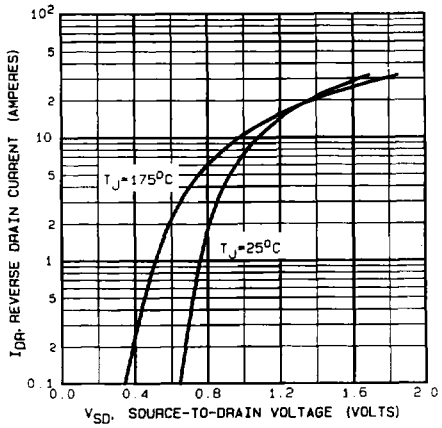


Fig. 7 - Typical source-drain diode forward voltage.

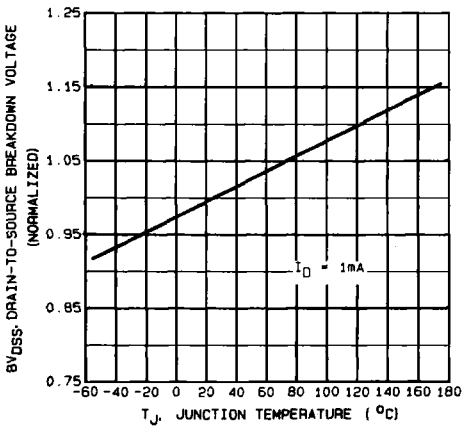


Fig. 8 - Breakdown voltage vs. temperature.

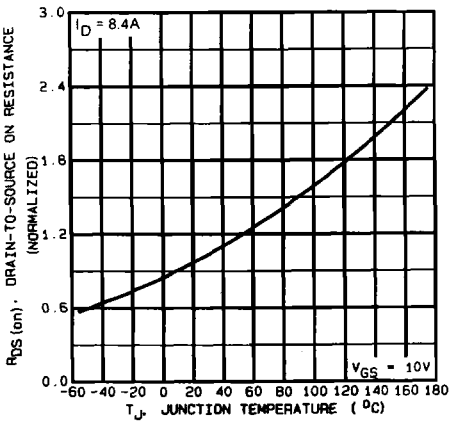


Fig. 9 - Normalized on-resistance vs. temperature.

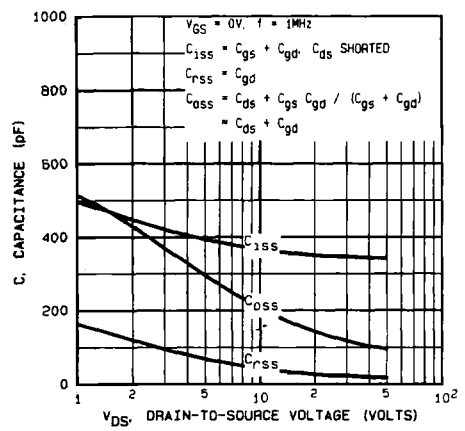


Fig. 10 - Typical capacitance vs. drain-to-source voltage.

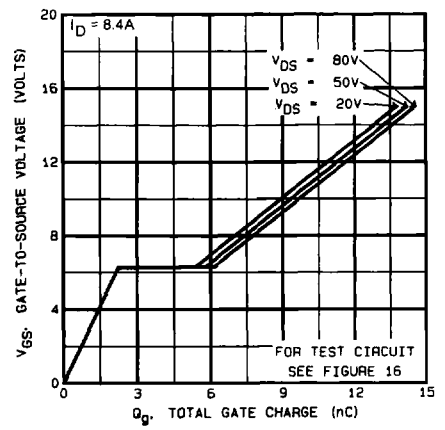


Fig. 11 - Typical gate charge vs. gate-to-source voltage.

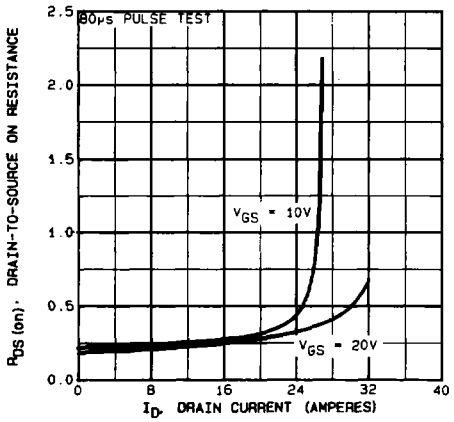


Fig. 12 — Typical on-resistance vs. drain current

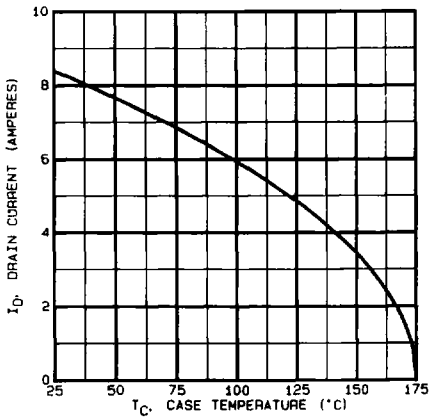


Fig. 13 — Maximum drain current vs. case temperature

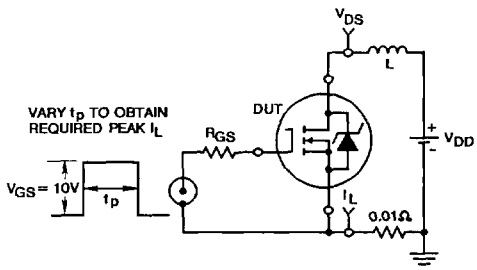


Fig. 14a — unclamped inductive test circuit

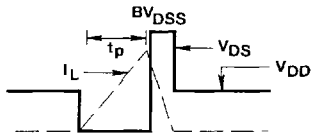


Fig. 14b — unclamped inductive waveforms

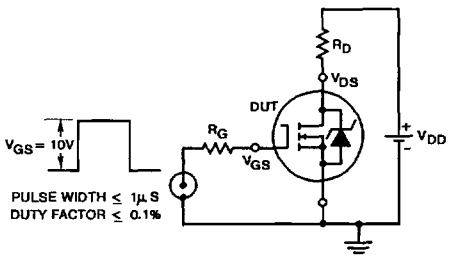


Fig. 15a — switching time test circuit

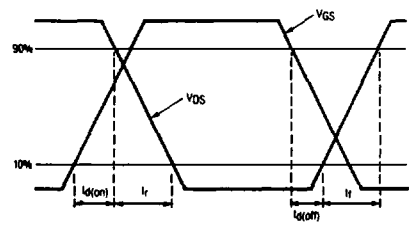


Fig. 15b — switching time waveforms

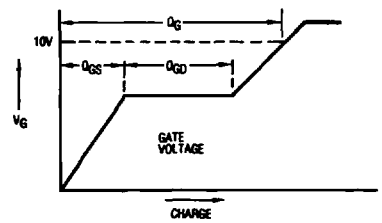


Fig. 16a — Basic gate charge waveform

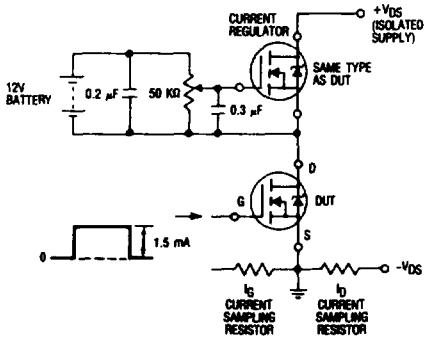


Fig. 16b — Gate charge test circuit