



Features

- Automatic power-down when deselected
- Output Enable (\overline{OE}) feature (7C196)
- CMOS for optimum speed/power
- High speed
 - 25 ns t_{AA}
- Low active power
 - 660 mW
- Low standby power
 - 193 mW
- TTL-compatible inputs and outputs

- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C194 and CY7C196 are high-performance CMOS static RAMs organized as 65,536 by 4 bits. Easy memory expansion is provided by active LOW chip enable(s) (\overline{CE} on the CY7C194, \overline{CE}_1 , \overline{CE}_2 on the CY7C196) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 71% when deselected.

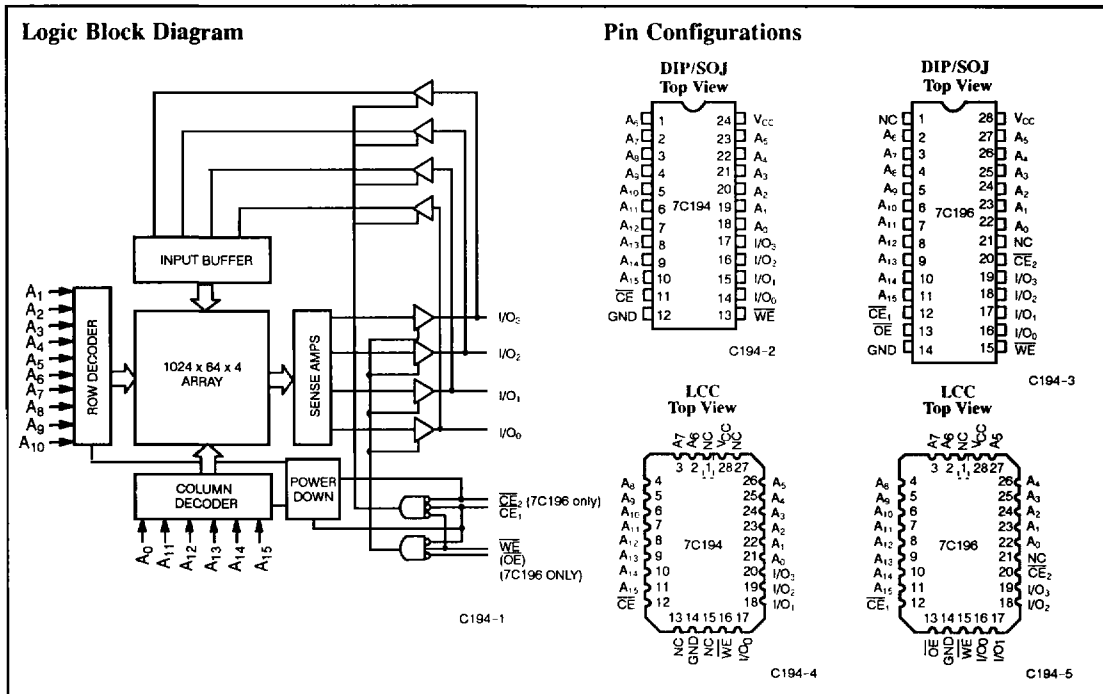
Writing to the device is accomplished when the chip enable(s) (\overline{CE} on the CY7C194,

\overline{CE}_1 , \overline{CE}_2 on the CY7C196) and write enable (\overline{WE}) inputs are both LOW. Data on the four input pins (I/O_0 through I/O_3) is written into the memory location, specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable(s) (\overline{CE} on the CY7C194, \overline{CE}_1 , \overline{CE}_2 on the CY7C196) LOW, while write enable (\overline{WE}) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

A die coat is used to ensure alpha immunity.

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Selection Guide

		7C194-25 7C196-25	7C194-35 7C196-35	7C194-45 7C196-45
Maximum Access Time (ns)		25	35	45
Maximum Operating Current (mA)	Commercial	120	120	120
	Military	130	130	130
Maximum Standby Current (mA)		35	35	35

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	- 65°C to + 150°C
Ambient Temperature with Power Applied	- 55°C to + 125°C
Supply Voltage to Ground Potential	- 0.5V to + 7.0V
DC Voltage Applied to Outputs in High Z State	- 0.5V to + 7.0V
DC Input Voltage	- 3.0V to + 7.0V
Output Current into Outputs (Low)	20 mA

Static Discharge Voltage	> 2001V (per MIL-STD-883, Method 3015)
Latch-Up Current	> 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to + 70°C	5V ± 10%
Military ^[1]	- 55°C to + 125°C	5V ± 10%

Electrical Characteristics Over the Operating Range^[2]

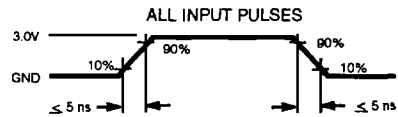
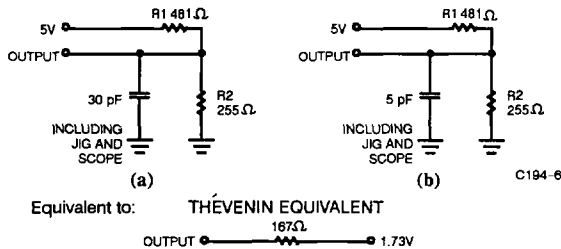
Parameters	Description	Test Conditions	7C194-25, 35, 45 7C196-25, 35, 45		Units
			Min.	Max.	
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = - 4.0 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4	V
V _{IH}	Input HIGH Voltage		2.2	V _{CC}	V
V _{IL}	Input LOW Voltage		-3.0	0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}	-10	+ 10	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled	-10	+ 10	μA
I _{OS}	Output Short Circuit Current ^[3]	V _{CC} = Max., V _{OUT} = GND		-350	mA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max. I _{OUT} = 0 mA	Com'l	120	mA
			Mil	130	
I _{ISB} [†]	Automatic \overline{CE} Power-Down Current ^[4]	Max. V _{CC} , $\overline{CE} \geq V_{IH}$, Min. Duty Cycle = 100%		35	mA
I _{ISB@}	Automatic \overline{CE} Power-Down Current ^[4]	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V		20	mA

Capacitance^[5]

Parameters	Description	Test Conditions	Max.	Units
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz V _{CC} = 5.0V	5	pF
C _{OUT}	Output Capacitance		7	pF

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. A pull-up resistor to V_{CC} on the \overline{CE} input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
5. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms


C194-7

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Switching Characteristics Over the Operating Range^[2,6]

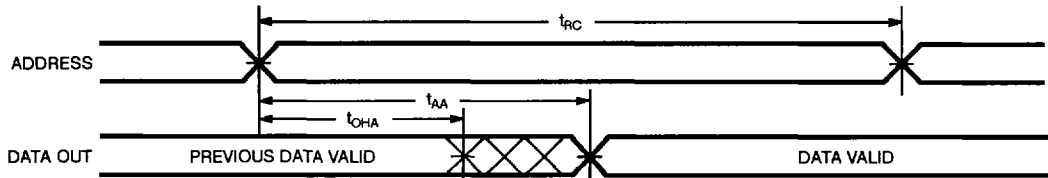
Parameters	Description	7C194-25 7C196-25		7C194-35 7C196-35		7C194-45 7C196-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	25		35		45		ns
t_{AA}	Address to Data Valid		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		ns
$t_{ACE1, ACE2}$	\overline{CE} LOW to Data Valid		25		35		45	ns
t_{DOE}	\overline{OE} LOW to Data Valid		15		20		20	ns
t_{LZOE}	\overline{OE} LOW to Low Z	3		3		3		ns
t_{HZOE}	\overline{OE} HIGH to High Z		13		15		20	ns
$t_{LZCE1, CE2}$	\overline{CE} LOW to Low Z ^[7]	3		3		3		ns
$t_{HZCE1, CE2}$	\overline{CE} HIGH to High Z ^[7, 8]		13		15		20	ns
t_{PU}	\overline{CE} LOW to Power-Up	0		0		0		ns
t_{PD}	\overline{CE} HIGH to Power-Down		25		35		45	ns
WRITE CYCLE^[9]								
t_{WC}	Write Cycle Time	20		30		40		ns
t_{SCE}	\overline{CE} LOW to Write End	20		30		40		ns
t_{AW}	Address Set-Up to Write End	20		25		35		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	\overline{WE} Pulse Width	20		25		30		ns
t_{SD}	Data Set-Up to Write End	15		17		20		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[7]	3		3		3		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[7, 8]	0	13	0	15	0	20	ns

Notes:

- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device.
- t_{HZCE} and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of \overline{CE}_1 LOW, \overline{CE}_2 LOW, and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

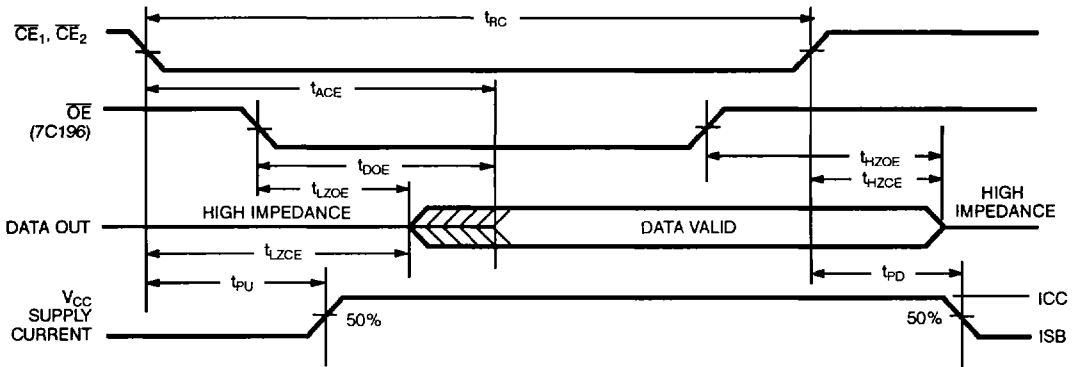
Switching Waveforms

Read Cycle No. 1^[10, 11]



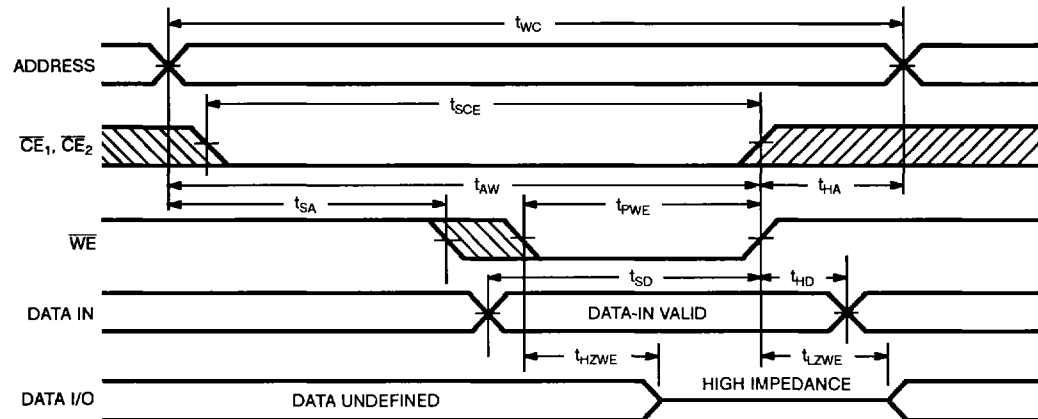
C194-8

Read Cycle No. 2^[10, 12]



C194-9

Write Cycle No. 1 (\overline{WE} Controlled)^[9, 13]



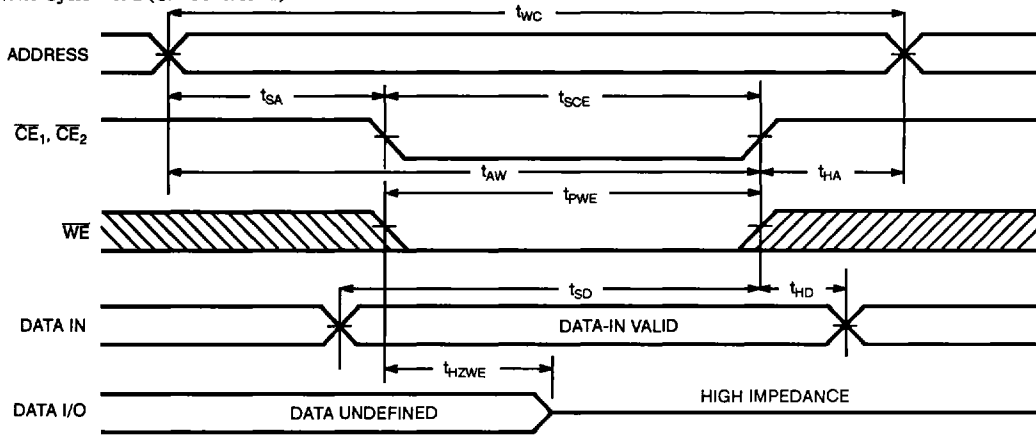
C194-10

Notes:

10. \overline{WE} is HIGH for read cycle.
11. Device is continuously selected, $\overline{CE}_1 = V_{IL}/\overline{CE}_2 = V_{IL}$ (7C196: $\overline{OE} = V_{IL}$, $\overline{CE}_2 = V_{IL}$ also).
12. Address valid prior to or coincident with \overline{CE}_1 and \overline{CE}_2 transition low.
12. 7C196 only: Data I/O will be high impedance if $\overline{OE} = V_{IH}$.
13. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

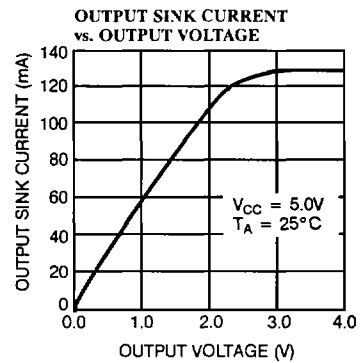
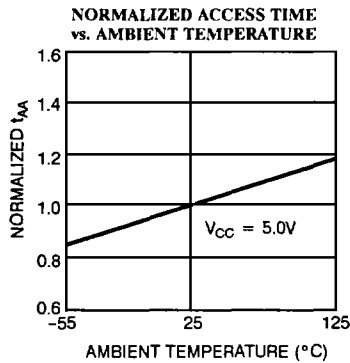
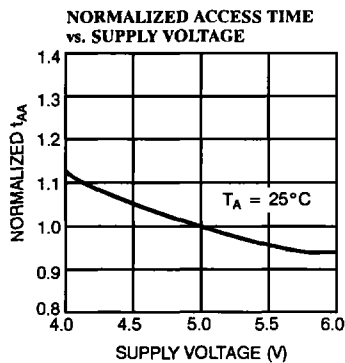
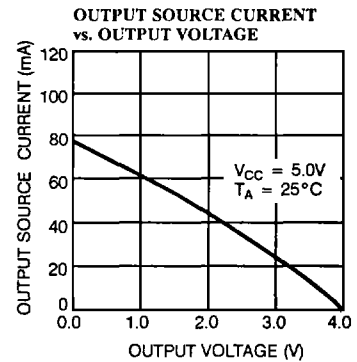
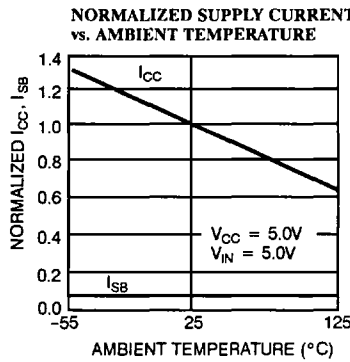
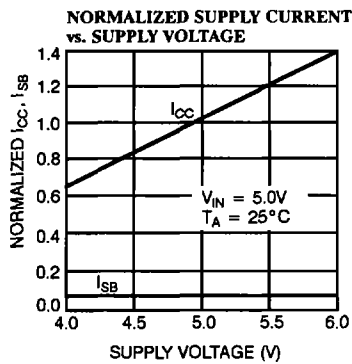
Write Cycle No. 2 (\overline{CE} Controlled)^{9, 13, 14}



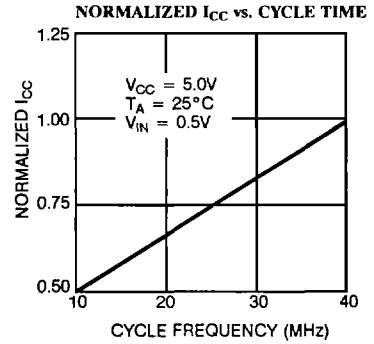
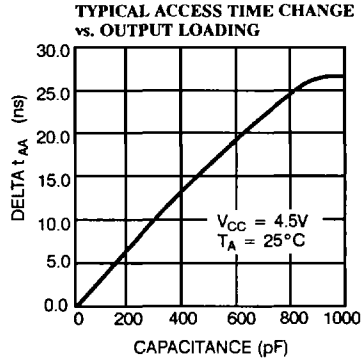
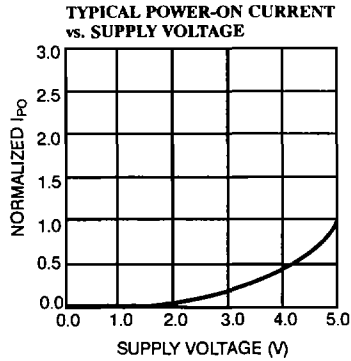
C194-11

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Typical DC and AC Characteristics



Typical DC and AC Characteristics (continued)



7C194 Truth Table

\overline{CE}	\overline{WE}	Inputs/Outputs	Mode
H	X	High Z	Deselect/Power-Down
L	H	Data Out	Read
L	L	Data In	Write

7C196 Truth Table

\overline{CE}_1	\overline{CE}_2	\overline{WE}	\overline{OE}	Inputs/Outputs	Mode
H	X	X	X	High Z	Deselect/Power-Down
X	H	X	X		
L	L	H	L	Data Out	Read
L	L	L	X	Data In	Write
L	L	H	H	High Z	Deselect

Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C194-25PC	P13	Commercial
	CY7C194-25VC	V13	
	CY7C194-25DC	D14	
	CY7C194-25LC	L54	
	CY7C194-25DMB	D14	Military
	CY7C194-25LMB	L54	
	CY7C194-25KMB	K73	
35	CY7C194-35PC	P13	Commercial
	CY7C194-35VC	V13	
	CY7C194-35DC	D14	
	CY7C194-35LC	L54	
	CY7C194-35DMB	D14	Military
	CY7C194-35LMB	L54	
	CY7C194-35KMB	K73	
45	CY7C194-45PC	P13	Commercial
	CY7C194-45VC	V13	
	CY7C194-45DC	D14	
	CY7C194-45LC	L54	
	CY7C194-45DMB	D14	Military
	CY7C194-45LMB	L54	
	CY7C194-45KMB	K73	

Shaded area contains preliminary information.

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C196-25PC	P21	Commercial
	CY7C196-25VC	V21	
	CY7C196-25DC	D22	
	CY7C196-25LC	L54	
	CY7C196-25DMB	D22	Military
	CY7C196-25LMB	L54	
	CY7C196-25KMB	K74	
35	CY7C196-35PC	P21	Commercial
	CY7C196-35VC	V21	
	CY7C196-35DC	D22	
	CY7C196-35LC	L54	
	CY7C196-35DMB	D22	Military
	CY7C196-35LMB	L54	
	CY7C196-35KMB	K74	
45	CY7C196-45PC	P21	Commercial
	CY7C196-45VC	V21	
	CY7C196-45DC	D22	
	CY7C196-45LC	L54	
	CY7C196-45DMB	D22	Military
	CY7C196-45LMB	L54	
	CY7C196-45KMB	K74	

Shaded area contains preliminary information.

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MILITARY SPECIFICATIONS
Group A Subgroup Testing
DC Characteristics

Parameters	Subgroups
V _{OH}	1, 2, 3
V _{OL}	1, 2, 3
V _{IH}	1, 2, 3
V _{IL Max.}	1, 2, 3
I _{Ix}	1, 2, 3
I _{OZ}	1, 2, 3
I _{OS}	1, 2, 3
I _{CC}	1, 2, 3
I _{SB1}	1, 2, 3
I _{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t _{RC}	7, 8, 9, 10, 11
t _{AA}	7, 8, 9, 10, 11
t _{OHA}	7, 8, 9, 10, 11
t _{ACE, ACE2}	7, 8, 9, 10, 11
t _{DOE} ^[15]	7, 8, 9, 10, 11
WRITE CYCLE	
t _{WC}	7, 8, 9, 10, 11
t _{SCE}	7, 8, 9, 10, 11
t _{AW}	7, 8, 9, 10, 11
t _{HA}	7, 8, 9, 10, 11
t _{SA}	7, 8, 9, 10, 11
t _{PWE}	7, 8, 9, 10, 11
t _{SD}	7, 8, 9, 10, 11
t _{HD}	7, 8, 9, 10, 11
t _{AWE}	7, 8, 9, 10, 11
t _{ADV}	7, 8, 9, 10, 11

Note:

15. 7C196 only.

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