VIPER53EDIP
VIPER53ESP

OFF LINE PRIMARY SWITCH

PRELIMINARY DATA

Table 1. TYPICAL OUTPUT POWER CAPABILITY

TYPE	European (195 - 265 Vac)	US / Wide range (85 - 265 Vac)
VIPer53EDIP	50W	30W
VIPer53ESP	65W	40W

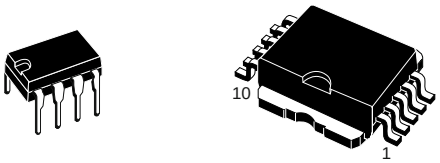
Note : Above power capabilities are given under adequate thermal conditions

- SWITCHING FREQUENCY UP TO 300 KHZ
- CURRENT MODE CONTROL WITH ADJUSTABLE CURRENT LIMITATION
- SOFT START AND SHUT DOWN CONTROL
- AUTOMATIC BURST MODE IN STAND-BY CONDITION (“BLUE ANGEL” COMPLIANT)
- UNDERVOLTAGE LOCKOUT WITH HYSTERESIS
- INTEGRATED STARTUP CURRENT SOURCE
- OVERTEMPERATURE PROTECTION
- OVERLOAD AND SHORT-CIRCUIT CONTROL
- OVERVOLTAGE PROTECTION

DESCRIPTION

The VIPer53E combines in the same package an enhanced current mode PWM controller with a high voltage MDMesh Power Mosfet.

Figure 1. Package



DIP-8 PowerSO-10™

Typical applications cover off line power supplies with a secondary power capability ranging up to 30W in wide range input voltage or 50W in single European voltage range and DIP-8 package, with the following benefits:

– Overload and short circuit controlled by feedback monitoring and delayed device reset.

– Efficient standby mode by enhanced pulse skipping.

Integrated startup current source disabled during the normal operation to reduce the input power.

Table 2. Order Codes

Package	Tube	Tape And Reel
DIP-8	VIPer53EDIP	-
PowerSO-10™	VIPer53ESP	VIPer53ESP13TR

Figure 2. Block Diagram

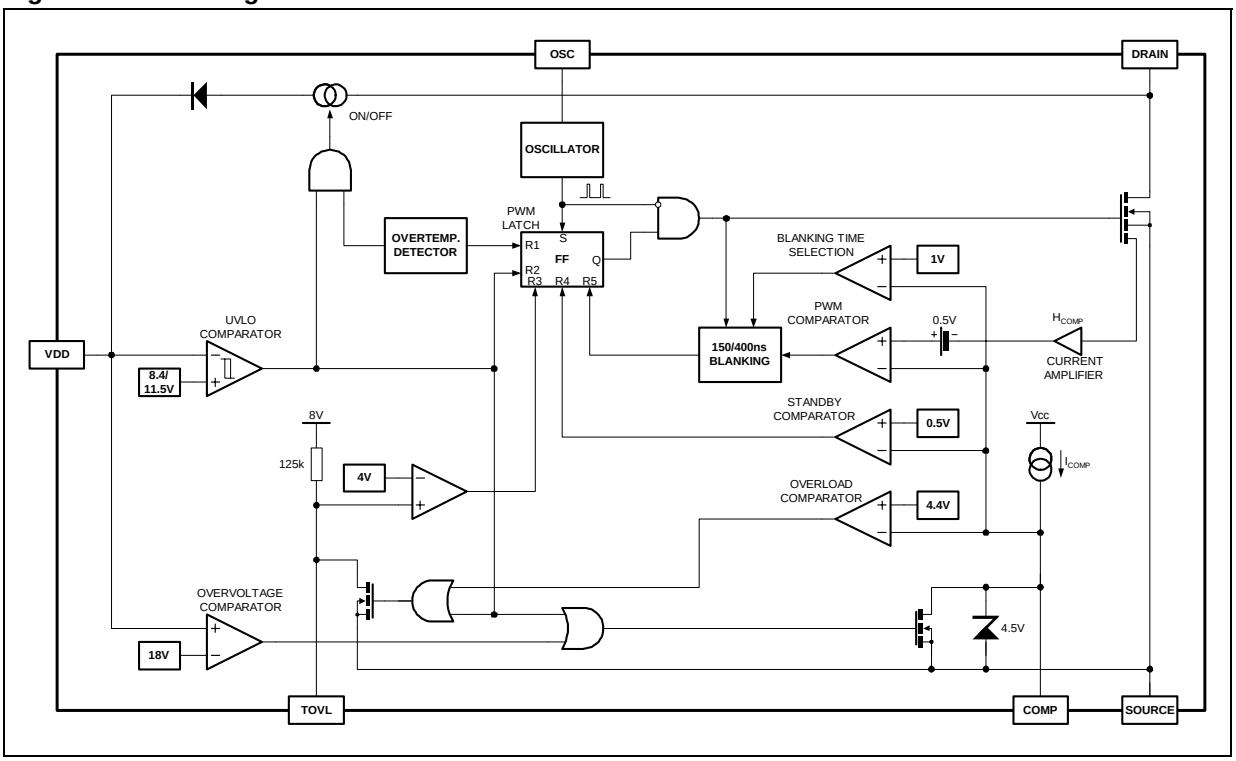
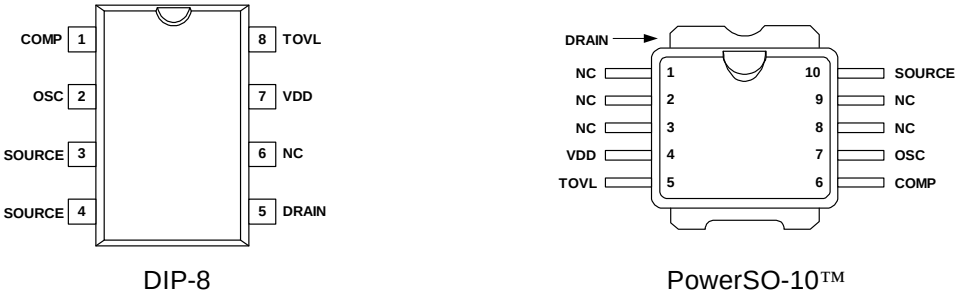


Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DS}	Continuous Drain Source Voltage (T_j=25 ... 125°C) (See note 1)	-0.3 ... 620	V
I_D	Continuous Drain Current	Internally limited	A
V_{DD}	Supply Voltage	0 ... 19	V
V_{OSC}	OSC Input Voltage Range	0 ... V_{DD}	V
I_{COMP} I_{TOVL}	COMP and TOVL Input Current Range (See note 1)	-2 ... 2	mA
V_{ESD}	Electrostatic Discharge: Machine Model (R=0Ω; C=200pF) Charged Device Model	 200 1.5	 V kV
T_j	Junction Operating Temperature	Internally limited	°C
T_c	Case Operating Temperature	-40 to 150	°C
T_{stg}	Storage Temperature	-55 to 150	°C

Note: 1. In order to improve the ruggedness of the device versus eventual drain overvoltages, a resistance of 1 kΩ should be inserted in series with the TOVL pin.

Figure 3. Configuration Diagram (Top View)



DIP-8 PowerSO-10™

Table 4. Pin Function

Name	Function
V_{DD}	Power supply of the control circuits. Also provides the charging current of the external capacitor during startup. The functions of this pin are managed by three threshold voltages: - V_{DDon}: Voltage value at which the device starts switching (Typically 11.5 V). - V_{DDoff}: Voltage value at which the device stops switching (Typically 8.4 V). - V_{DDovp}: Triggering voltage of the overvoltage protection (Trimmed to 18 V).
SOURCE	Power Mosfet source and circuit ground reference.
DRAIN	Power Mosfet drain. Also used by the internal high voltage current source during the start-up phase, for charging the external V_{DD} capacitor.
COMP	Input of the current mode structure. Allows the setting of the dynamic characteristic of the converter through an external passive network. Useful voltage range extends from 0.5 V to 4.5 V. The Power Mosfet is always off below 0.5 V, and the overload protection is triggered if the voltage exceeds 4.4V. This action is delayed by the timing capacitor connected to the TOVL pin.
TOVL	Allows the connection of an external capacitor for delaying the overload protection, which is triggered by a voltage on the COMP pin higher than 4.4 V.
OSC	Allows the setting of the switching frequency through an external Rt-Ct network.

Figure 4. Current and Voltage Conventions

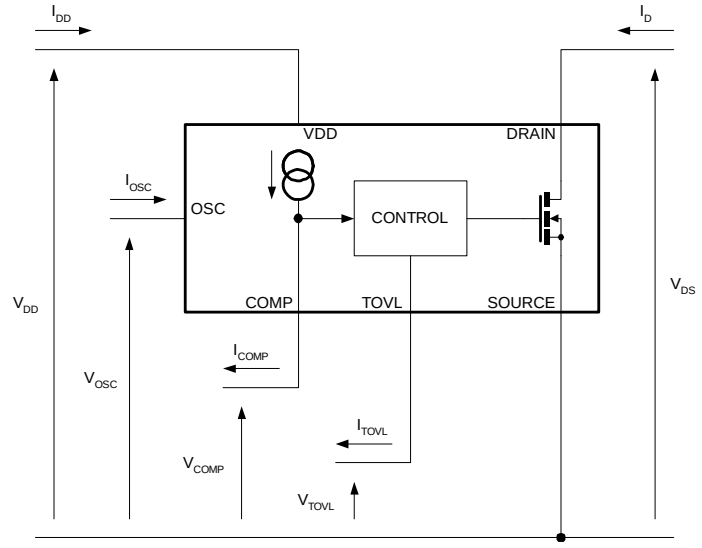


Table 5. Thermal Data

Symbol	Parameter	Max Value	Unit
$R_{thj\text{-}case}$	DIP-8	20	°C/W
$R_{thj\text{-}amb}$	DIP-8 (See note 4)	80	°C/W
$R_{thj\text{-}case}$	PowerSO-10™	2	°C/W
$R_{thj\text{-}amb}$	PowerSO-10™ (See note 4)	60	°C/W

Note: 2. When mounted on a standard single-sided FR4 board with 50mm² of Cu (at least 35 µm thick) connected to the DRAIN pin.

Note: 3. When mounted on a standard single-sided FR4 board with 50mm² of Cu (at least 35 µm thick) connected to the device tab.

ELECTRICAL CHARACTERISTICS (T_j=25°C, V_{DD}=13V, unless otherwise specified)

Table 6. Power Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Voltage	I_D=1mA; V_{COMP}=0V	620			V
I_{DSS}	Off State Drain Current	V_{DS}=500V; V_{COMP}=0V; T_j=125°C			150	µA
$R_{DS(on)}$	Static Drain-Source On State Resistance	I_D=1A; V_{COMP}=4.5V; V_{TOVL}=0V T_j=25°C T_j=100°C		0.9	1 1.7	Ω Ω
t_{fv}	Fall Time	I_D=0.2A; V_{IN}=300V (See figure 5 and note 4)		100		ns
t_{rv}	Rise Time	I_D=1A; V_{IN}=300V (See figure 5 and note 4)		50		ns
C_{oss}	Drain Capacitance	V_{DS}=25V		170		pF
C_{Eon}	Effective Output Capacitance	200V < V_{DSon} < 400V (See note 4)		60		pF

Note: 4. On clamped inductive load

Note: 5. This parameter can be used to compute the energy dissipated at turn on E_{ton} according to the initial drain to source voltage V_{DSon} and the following formula:

$$E_{ton} = \frac{1}{2} \cdot C_{Eon} \cdot 300^2 \cdot \left(\frac{V_{DSon}}{300}\right)^{1.5}$$

Table 7. Oscillator Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
F_{OSC1}	Oscillator Frequency Initial Accuracy	R_T=8kΩ; C_T=2.2nF (See figure 9)	95	100	105	kHz
F_{OSC2}	Oscillator Frequency Total Variation	R_T=8kΩ; C_T=2.2nF (See figure 10) V_{DD}=V_{DDon} ... V_{DDovp}; T_j=0 ... 100°C	93	100	107	kHz
V_{OSChi}	Oscillator Peak Voltage			9		V
V_{OSClo}	Oscillator Valley Voltage			4		V

ELECTRICAL CHARACTERISTICS (T_j=25°C, V_{DD}=13V, unless otherwise specified)

Table 8. Supply Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{DSstart}$	Drain Voltage Starting Threshold	V_{DD}=5V; I_{DD}=0mA		34	50	V
I_{DDch1}	Startup Charging Current	V_{DD}=0 ... 5V; V_{DS}=100V (See figure 6)		-12		mA
I_{DDch2}	Startup Charging Current	V_{DD}=10V; V_{DS}=100V (See figure 6)		-2		mA
$I_{DDchoff}$	Startup Charging Current in Thermal Shutdown	V_{DD}=5V; V_{DS}=100V (See figure 8) $T_j > T_{SD} - T_{HYST}$	0			mA
I_{DD0}	Operating Supply Current Not Switching	F_{sw}=0kHz; V_{COMP}=0V		8	11	mA
I_{DD1}	Operating Supply Current Switching	F_{sw}=100kHz		9		mA
V_{DDoff}	V_{DD} Undervoltage Shutdown Threshold	(See figure 6)	7.5	8.4	9.3	V
V_{DDon}	V_{DD} Startup Threshold	(See figure 6)	10.2	11.5	12.8	V
V_{DDhyst}	V_{DD} Threshold Hysteresis	(See figure 6)	2.6	3.1		V
V_{DDovp}	V_{DD} Overvoltage Shutdown Threshold	(See figure 8)	17	18	19	V

Table 9. Pwm Comparator Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
H_{COMP}	ΔV_{COMP} / ΔI_{DPEAK}	V_{COMP}=1 ... 4 V (See figure 8) dI_D/dt=0	1.7	2	2.3	V/A
V_{COMPos}	V_{COMP} Offset	dI_D/dt=0 (See figure 8)		0.5		V
I_{Dlim}	Peak Drain Current Limitation	I_{COMP}=0mA; V_{TOVL}=0V (See figure 8) dI_D/dt=0	1.7	2	2.3	A
I_{Dmax}	Drain Current Capability	V_{COMP}=$V_{COMPovl}$; V_{TOVL}=0V dI_D/dt=0 (See figure 8)	1.6	1.9	2.3	A
t_d	Current Sense Delay to Turn-Off	I_D=1A		250		ns
V_{COMPbl}	V_{COMP} Blanking Time Change Threshold	(See figure 7)		1		V
t_{b1}	Blanking Time	V_{COMP} < V_{COMPBL} (See figure 7)	300	400	500	ns
t_{b2}	Blanking Time	V_{COMP} > V_{COMPBL} (See figure 7)	100	150	200	ns
t_{ONmin1}	Minimum On Time	V_{COMP} < V_{COMPBL}	450	600	750	ns
t_{ONmin2}	Minimum On Time	V_{COMP} > V_{COMPBL}	250	350	450	ns
$V_{COMPoff}$	V_{COMP} Shutdown Threshold	(See figure 8)		0.5		V
V_{COMPhi}	V_{COMP} High Level	I_{COMP}=0mA (See note 5)		4.5		V
I_{COMP}	COMP Pull Up Current	V_{COMP}=2.5V		0.6		mA

Note: 6. In order to insure a correct stability of the error amplifier, a capacitor of 10nF (minimum value: 8nF) should always be present on the COMP pin.

ELECTRICAL CHARACTERISTICS (T_J=25°C, V_{DD}=13V, unless otherwise specified)

Table 10. Overload Protection Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{COMPovl}$	V_{COMP} Overload Threshold	I_{TOVL}=0mA (See figure 4 and note 6)		4.35		V
$V_{DIFFovl}$	V_{COMPhi} to $V_{COMPovl}$ Voltage Difference	V_{DD}=V_{DDoff} ... V_{DDovp}; I_{TOVL}=0mA (See figure 4 and note 6)	50	150	250	mV
V_{OVLth}	V_{TOVL} Overload Threshold	(See figure 4)		4		V
t_{OVL}	Overload Delay	C_{OVL}=100nF (See figure 4)		8		ms

Note: 7. $V_{COMPovl}$ is always lower than V_{COMPhi}.

Table 11. Overtemperature Protection Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{SD}	Thermal Shutdown Temperature	(See fig. 8)	140	160		°C
T_{HYST}	Thermal Shutdown Hysteresis	(See fig. 8)		40		°C

Figure 5. Rise and Fall Time

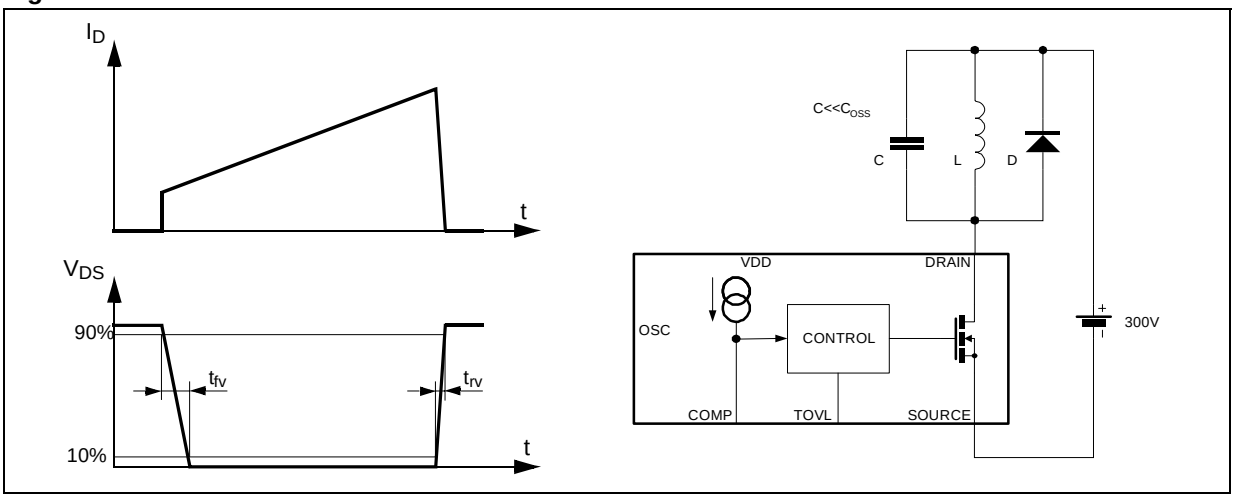


Figure 6. Startup VDD Current

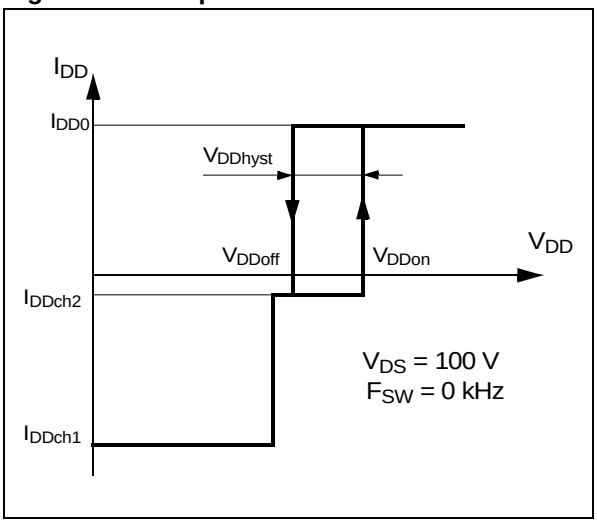


Figure 7. Blanking Time

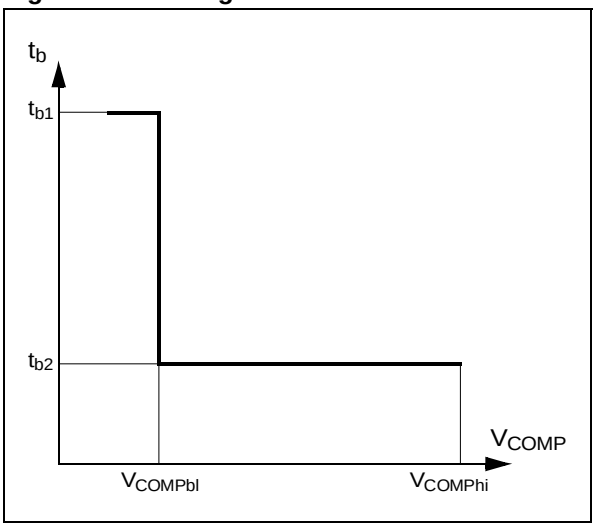


Figure 8. Overload Event

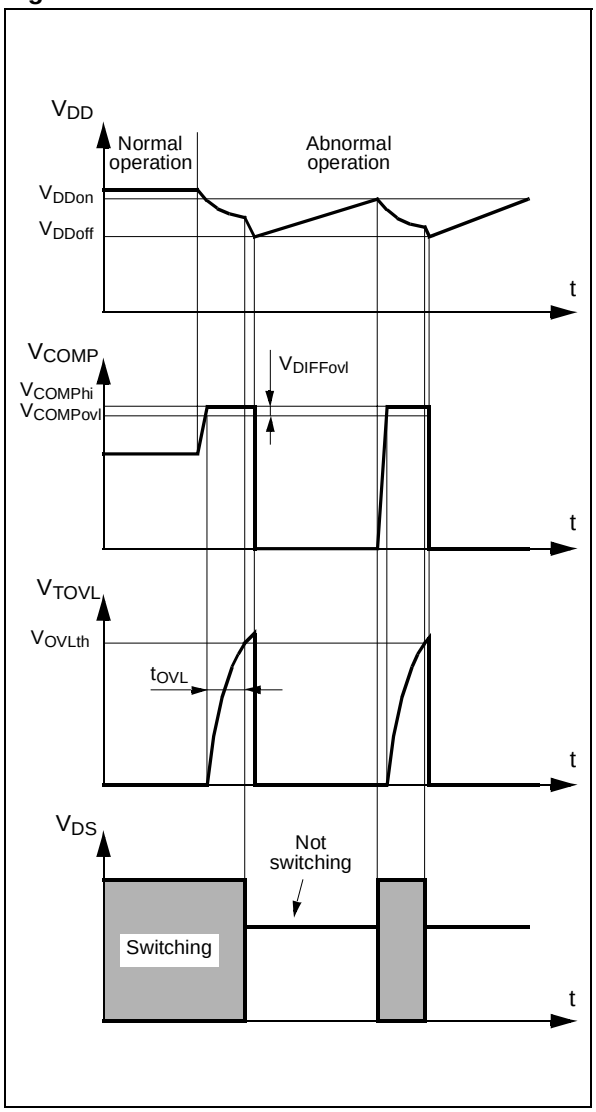


Figure 9: Thermal Shutdown

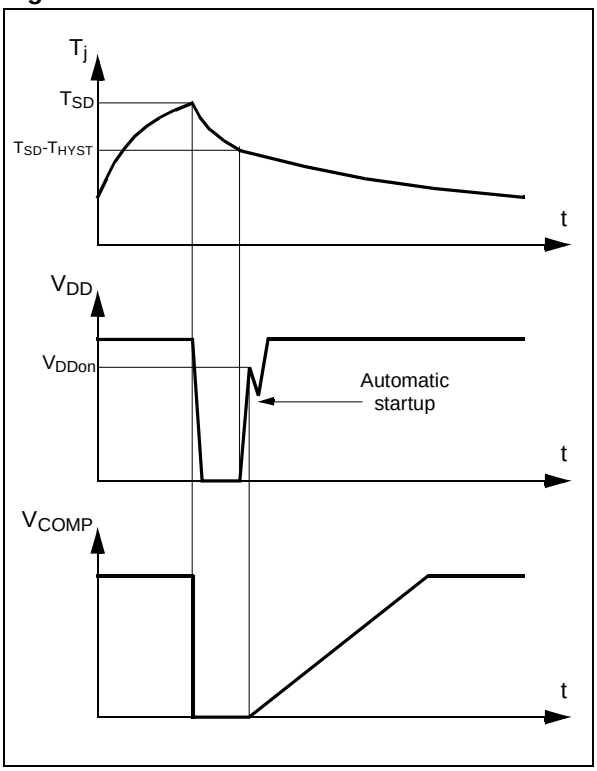


Figure 10: Shut Down Action

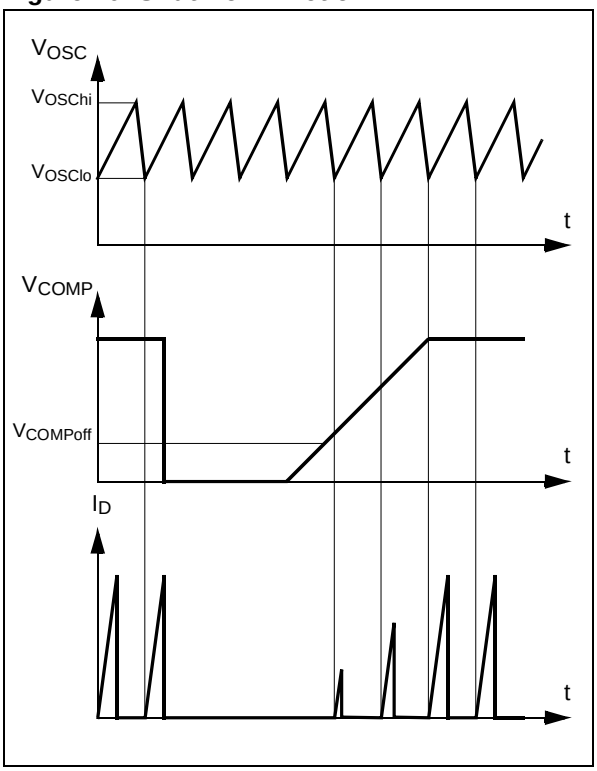


Figure 11: Overvoltage Event

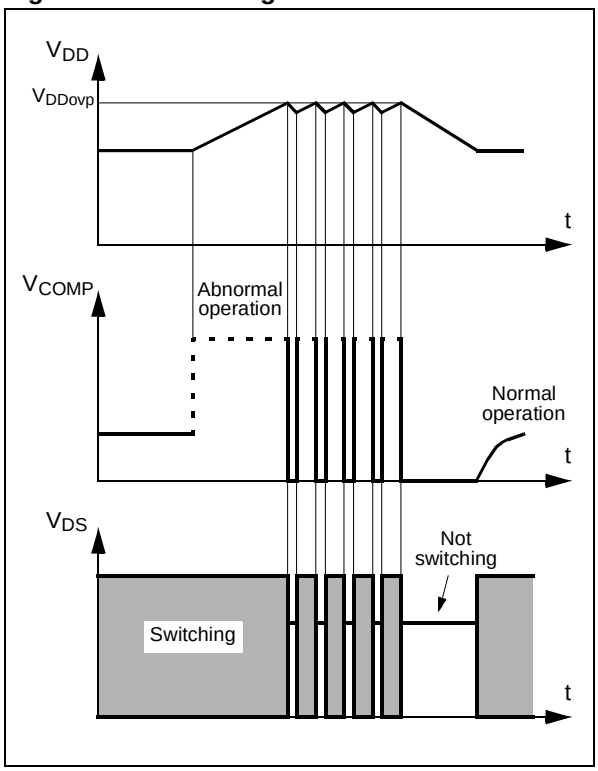


Figure 12: Comp Pin Gain and Offset

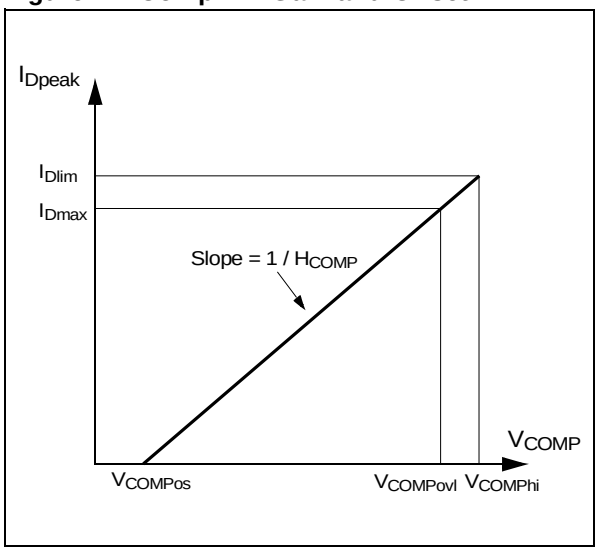
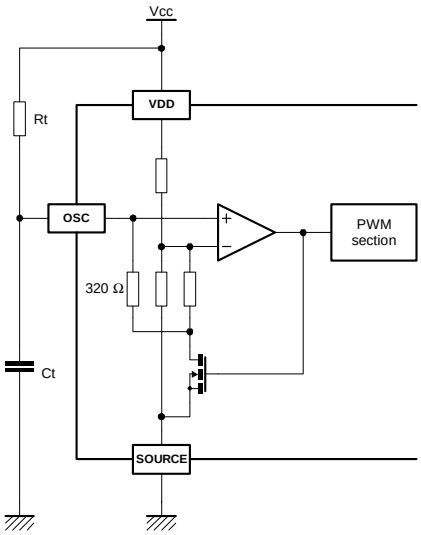


Figure 13: Oscillator Schematic and Settings



The switching frequency settings shown on the graphic here below is valid within the following boundaries:

$R_t > 2k\Omega$

$F_{SW} < 300kHz$

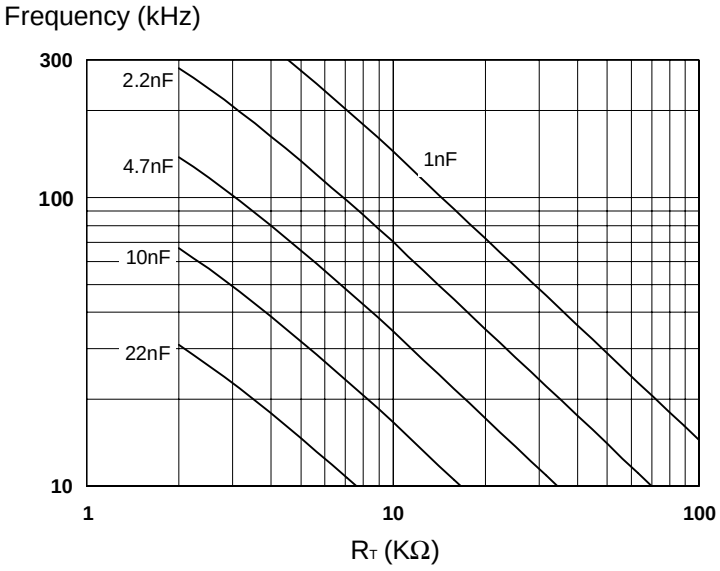


Figure 14: Typical Frequency Variation Vs. Junction Temperature

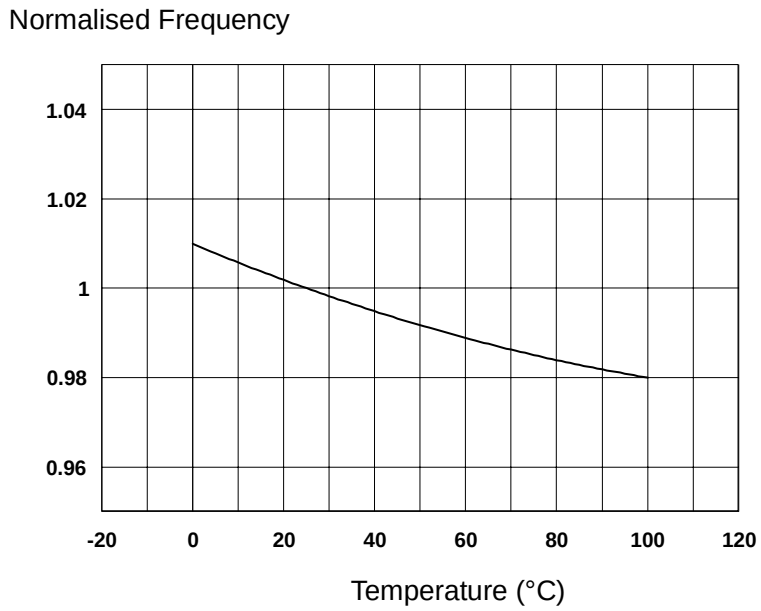


Figure 15: Typical Current Limitation Vs. Junction Temperature

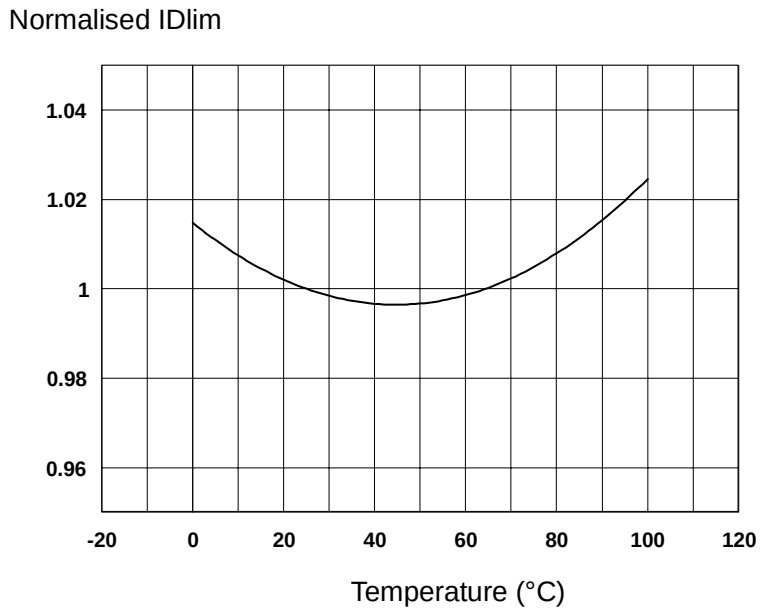
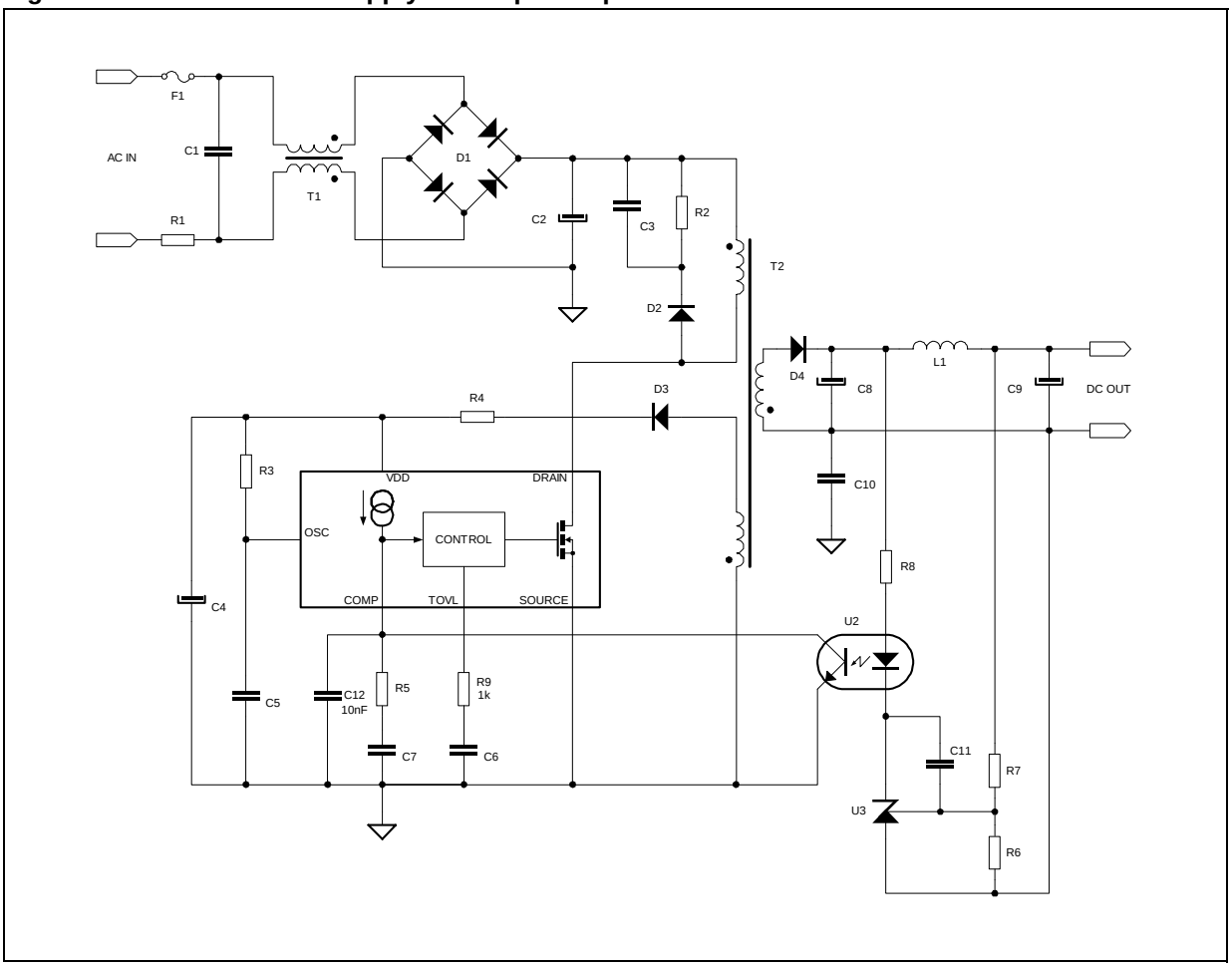


Figure 16: Off Line Power Supply With Optocoupler Feedback



SECONDARY FEEDBACK CONFIGURATION EXAMPLE

The secondary feedback is implemented through an optocoupler driven by a programmable zener of the TL431 type as shown on figure 11.

The optocoupler is connected in parallel with the compensation network on the COMP pin which delivers a constant biasing current of 0.6 mA to the optotransistor. This current doesn't depend on the compensation voltage, and so it doesn't depend on the output load either. The gain of the optocoupler ensures consequently a constant biasing of the TL431 device (U3) which is in charge of secondary regulation. If the optocoupler gain is sufficiently low, no additional components are required to ensure a minimum current biasing of U3. Also, the low biasing current value avoid any ageing of the optocoupler.

The constant current biasing can be used to simplify the secondary circuit: Instead of a TL431, a simple zener and resistance network in series with the optocoupler diode can insure a good secondary regulation. As the current flowing in this branch remains constant for the same reason as above, typical load regulation of 1% can be achieved from zero to full output current with this simple configuration.

Since the dynamic characteristics of the converter are set on the secondary side through components associated to U3, the compensation network has only a role of gain stabilization for the optocoupler, and its value can be freely chosen. R5 can be set to a fixed value of 2.2 kΩ, offering the possibility of using C7 as a soft start capacitor: When starting up the converter, the VIPer53E device delivers a constant current of 0.6 mA on the COMP pin, creating a constant voltage of 1.3 V in R5 and a rising slope across C7. This voltage shape together with the operating range of 0.5 V to 4.5 V provides a soft startup of the converter. The rising speed of the output voltage can be set through the value of C7. C4 and C6 values must be adjusted accordingly in order to ensure a correct startup.

CURRENT MODE TOPOLOGY

The VIPer53E implements the conventional current mode control method for regulating the output voltage. This kind of feedback includes two nested regulation loops:

The inner loop controls the peak primary current cycle by cycle. When the Power MOSFET output transistor is on, the inductor current (primary side of the transformer) is monitored with a SenseFET technique and converted into a voltage Vs. When Vs reaches V_{COMP}, the power switch is turned off. This structure is completely integrated as shown on the Block Diagram of page 2, with the current amplifier, the PWM comparator, the blanking time function and the PWM latch. The following formula gives the peak current in the Power MOSFET according to the compensation voltage:

$$I_{Dpeak} = \frac{V_{COMP} - V_{COMPos}}{H_{COMP}}$$

The outer loop defines the level at which the inner loop regulates peak current in the power switch. For this purpose, V_{COMP} is driven by the output of the regulation loop (A TL431 through an optocoupler in secondary feedback configuration, see figure 11) and sets accordingly the peak drain current for each switching cycle.

As the inner loop regulates the peak primary current in the primary side of the transformer, all input voltage changes are compensated for before impacting the output voltage. This results in an improved line regulation, instantaneous correction to line changes and better stability for the voltage regulation loop.

Current mode topology also provides a good converter startup control. As the compensation voltage can be controlled to increase slowly during the startup phase, the peak primary current will follow this soft voltage slope to provide a smooth output voltage rise, without any overshoot. The simpler voltage mode structure which only controls the duty cycle, leads generally to high currents at startup with the risk of transformer saturation.

An integrated blanking filter inhibits the PWM comparator output for a short time after the integrated Power MOSFET is switched on. This function prevents anomalous or premature termination of the switching pulse in the case of current spikes caused by primary side transformer capacitance or secondary side rectifier reverse recovery time when working in continuous mode.

STANDBY MODE

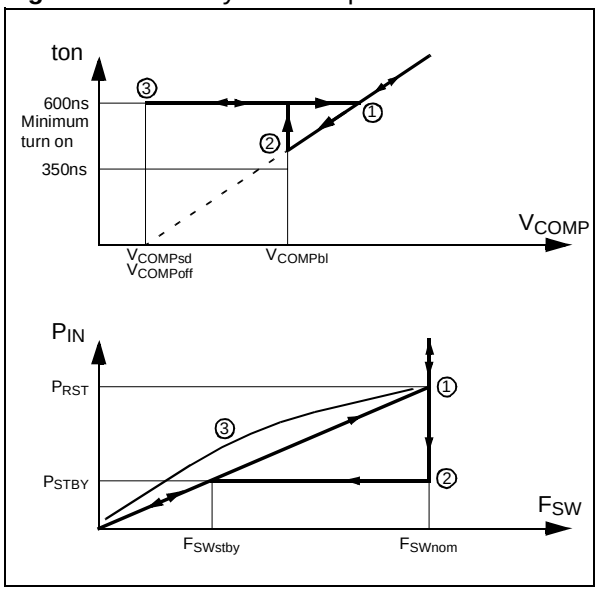
The device implements a special feature to address the low load condition. The corresponding function described hereafter consists of reducing the switching frequency by going into burst mode, with the following benefits:

– It reduces the switching losses, thus providing low consumption on the mains lines. The device is compliant with “Blue Angel” and other similar standards, requiring less than 0.5 W of input power when in standby.
– It allows the regulation of the output voltage, even if the load corresponds to a duty cycle that the device is not able to generate because of the internal blanking time, and associated minimum turn on.

For this purpose, a comparator monitores the COMP pin voltage, and maintains the PWM latch and the Power MOSFET in the off state as long as V_{COMP} remains below 0.5 V (See Block Diagram on page 2). If the output load requires a duty cycle below the one defined by the minimum turn on of the device, the regulation loop drives the COMP voltage until it reaches this 0.5 V threshold ($V_{COMPoff}$). The Power MOSFET can be completely off for some cycles, and resumes normal operation as soon as V_{COMP} is higher than 0.5 V. The output voltage is regulated in burst mode. The corresponding ripple is not higher than the nominal one at full load.

In addition, the minimum turn on time which defines the frontier between normal operation and burst mode changes according to V_{COMP} value. Below 1 V (V_{COMPbl}), the blanking time increases to 400 ns, whereas it is 150 ns for higher voltages (See figure 7). The minimum turn on times resulting from these values are respectively 600 ns and 350 ns, when taking into account internal propagation time. This brutal change induces an hysteresis between normal operation and burst mode as shown on figure 12.

Figure 17: Standby Mode Implementation



When the output power decreases, the system reaches point 2 where V_{COMP} equals V_{COMPbl}. The minimum turn on time passes immediately from 350 ns to 600 ns, exceeding the effective turn on time that should be needed at such output power level. Therefore the regulation loop will quickly drive V_{COMP} to $V_{COMPoff}$ (Point 3) in order to pass into burst mode and to control the output voltage. The corresponding hysteresis can be seen on the switching frequency which passes from F_{SWnom} which is the normal switching frequency set by the components connected to the OSC pin, to F_{SWstby}. Note that this frequency is actually an equivalent number of switching pulses per second, rather than a fixed switching frequency, as the device is working in burst mode.

As long as the power remains below P_{RST} the output of the regulation loop remains stuck at V_{COMPsd} and the converter works in burst mode. Its "density" increases (i.e. the number of missing cycles decreases) as the power approaches P_{RST}, and resumes finally normal operation at point 1. The hysteresis cannot be seen on the switching frequency, but the COMP pin voltage which passes brutally at that power level from point 3 to point 1.

The power points value P_{RST} and P_{STBY} are defined by the following formulas:

$$P_{RST} = \frac{1}{2} \cdot F_{SWnom} \cdot (tb_1 + td)^2 \cdot V_{IN}^2 \cdot \frac{1}{Lp}$$

$$P_{STBY} = \frac{1}{2} \cdot F_{SWnom} \cdot Ip^2(V_{COMPbl}) \cdot Lp$$

Where $Ip(V_{COMPbl})$ is the peak Power MOSFET current corresponding to a compensation voltage of V_{COMPbl} (1V), that is to say about 250 mA. Note that the power point P_{STBY} where the converter is going into burst mode doesn't depend on the input voltage.

The standby frequency $F_{SWstb\,y}$ is given by:

$$F_{SWstby} = \frac{P_{STBY}}{P_{RST}} \cdot F_{SWnom}$$

The ratio between the nominal switching frequency and the standby one can be as high as 4, depending on the Lp value and input voltage.

HIGH VOLTAGE STARTUP CURRENT SOURCE

An integrated high voltage current source provides a bias current from the DRAIN pin during the startup phase. This current is partially absorbed by internal control circuits in standby mode with reduced consumption and also supplies the external capacitor connected to the VDD pin. As soon as the voltage on this pin reaches the high voltage threshold V_{DDon} of the UVLO logic, the device turns into active mode and starts switching. The startup current generator is switched off, and the converter should normally provide the needed current on the VDD pin through the auxiliary winding of the transformer, as shown on figure 11.

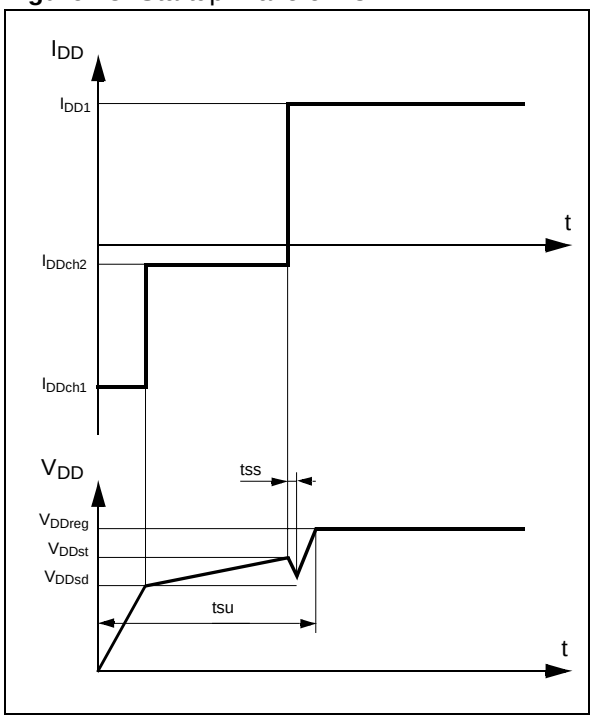
The external capacitor C_{VDD} on the VDD pin must be sized according to the time needed by the converter to startup, when the device starts switching. This time tss depends on many parameters, among which transformer design, output capacitors, soft start feature and compensation network implemented on the COMP pin and the secondary feedback circuit. The following formula can be used for defining the minimum capacitor needed:

$$C_{VDD} > \frac{I_{DD1} \cdot tss}{V_{DDhyst}}$$

Figure 13 shows a typical startup event. V_{DD} starts from 0 V with a charging current I_{DDch1} at about 9 mA. When about V_{DDoff} is reached, the charging current is reduced down to I_{DDch2} which is about 0.6 mA. This lower current leads to a slope change on the V_{DD} rise. The device starts switching for a V_{DD} equal to V_{DDon}, and the auxiliary winding delivers some energy to the V_{DD} capacitor after the startup time tss.

The charging current change at V_{DDoff} allows a fast complete startup time tsu, and maintains a low restart duty cycle. This is especially useful for short circuits and overloads conditions, as described in the following section.

Figure 18: Startup Waveforms



SHORT-CIRCUIT AND OVERLOAD PROTECTION

A $V_{COMPovl}$ threshold of about 4.4 V has been implemented on the COMP pin. When V_{COMP} goes above this level, the capacitor connected on the TOVL pin begins to charge. When reaching typically 4 V (V_{OVLth}), the internal mosfet driver is disabled and the device stops switching. This state is latched thanks to the regulation loop which maintains the COMP pin voltage above the $V_{COMPovl}$ threshold. Since the VDD pin doesn't receive any more energy from the auxiliary winding, its voltage drops down until it reaches VDDoff and the device is reset, recharging the VDD capacitor for a new restart cycle. Note that if VCOMP drops down below the $V_{COMPovl}$ threshold for any reason during the VDD drop, the device resumes switching immediately.

The device enters an endless restart sequence if the overload or short circuit condition is maintained. The restart duty cycle D_{RST} is defined as the time ratio for which the device tries to restart, thus delivering its full power capability to the output. In order to keep the whole converter in a safe state during this event, D_{RST} must be kept as low as possible, without compromising the real start up of the converter. A typical value of about 10 % is generally sufficient. For this purpose, both VDD and TOVL capacitors can be used to satisfy the following conditions:

$$C_{OVL} > 12.5 \cdot 10^{-6} \cdot tss$$

$$VDD > 8 \cdot 10^{4} \cdot \left(\frac{1}{D_{RST}} - 1\right) \cdot \frac{C_{OVL} \cdot I_{DDch2}}{V_{DDhyst}}$$

Refer to the previous startup section for the definition of tss, and C_{VDD} must also be checked against the limit given in this section. The maximum value of the two calculus will be adopted.

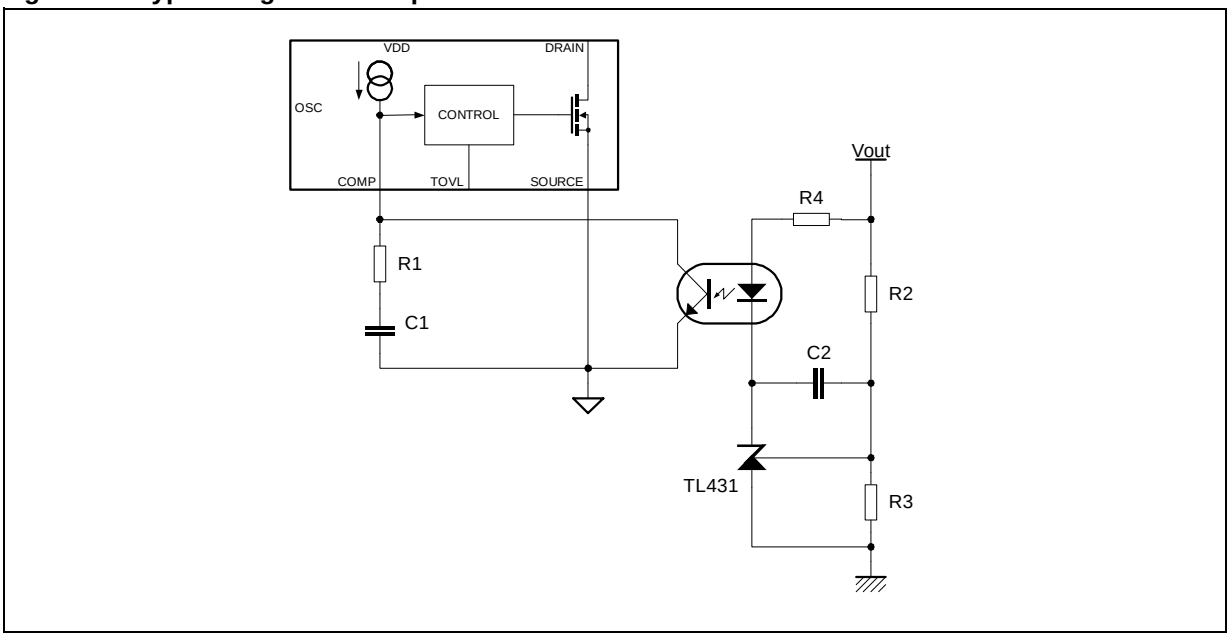
All this behavior can be observed on figure 4. In Figure 8 the value of the drain current Id for $V_{COMP}=V_{COMPovl}$ is shown. The corresponding parameter I_{Dmax} is the drain current to take into account for design purpose. Since I_{Dmax} represents the maximum value for which the overload protection is not triggered, it defines the power capability of the power supply.

REGULATION LOOP STABILITY

The complete converter open loop transfer function can be built from both power cell and regulation loop transfer functions. A theoretical example can be seen in figure 16 for a discontinuous mode flyback loaded by a simple resistor, regulated from secondary side through an optocoupler. A typical schematic corresponding to this situation can be seen on figure 11.

The transfer function of the power cell is represented as G(s) in figure 16. It exhibits a pole which depends on the output load and on the output capacitor value. As the load of a converter may change, two curves are shown for two different values of output resistance value, R_{L1} and R_{L2}. A zero at higher frequency values also appears, due to the output capacitor ESR. Note that the overall transfer function doesn't depend on the input voltage, thanks to the current mode control.

Figure 19: Typical regulation loop



A typical regulation loop is shown on figure 14 and has a fixed behavior represented by F(s) on figure 16. A double zero due to the R_1-C_1 network on the COMP pin and to the integrator built around the TL431 and R_2-C_2 is set at the same value as the maximum load R_{L2} pole.

The total transfer function is shown as F(s).G(s) at the bottom of figure 16. For maximum load (plain line), the load pole begins exactly where the zeros of the COMP pin and the TL431 stop, and this results in a first order decreasing slope until it reaches the zero of the output capacitor ESR. The point where the complete transfer function has a unity gain is known as the regulation bandwidth and has a double interest:

– The higher it is the faster will be the reaction to an eventual load change, and the smaller will be the output voltage change.
– The phase shift in the complete system at this point has to be less than 135 ° to ensure a good stability. Generally, a first order gives 90 ° of phase shift, and 180 ° for a second order.

In figure 16, the unity gain is reached in a first order slope, so the stability is ensured.

The dynamic load regulation is improved by increasing the regulation bandwidth, but some limitations have to be respected: As the transfer function above the zero due the capacitor ESR is not reliable (The ESR itself is not well specified, and other parasitic effects may take place), the bandwidth should always be lower than the minimum of F_C and ESR zero.

As the highest bandwidth is obtained with the highest output power (Plain line with R_{L2} load in figure 16), the above criteria will be checked for this condition and allows to define the value of R_4, if R1 is set fixed (2.2 kΩ, for instance). The following formula can be derived:

$$R_4 = \sqrt{\frac{P_{MAX}}{P_{OUT2}}} \cdot \frac{G_O \cdot R_1}{F_{BW2} \cdot R_{L2} \cdot C_{OUT}}$$

With: $P_{OUT2} = \frac{V_{OUT}^2}{R_{L2}}$

And: $P_{MAX} = \frac{1}{2} \cdot L_P \cdot I_{LIM}^2 \cdot F_{SW}$

Go is the current transfer ratio of the optocoupler.

The lowest load gives another condition for stability: The frequency F_{BW1} must not encounter the third order slope generated by the load pole, the R1-C1 network on the COMP pin and the R2-C2 network at the level of the TL431 on secondary side. This condition can be met by adjusting both C_1 and C2 values:

$$C_1 > \frac{R_{L1} \cdot C_{OUT}}{6.3 \cdot \frac{G_O}{R_4} \cdot R_1^2} \cdot \sqrt{\frac{P_{OUT1}}{P_{MAX}}}$$

$$C_2 > \frac{R_{L1} \cdot C_{OUT}}{6.3 \cdot \frac{G_O}{R_4} \cdot R_1 \cdot R_2} \cdot \sqrt{\frac{P_{OUT1}}{P_{MAX}}}$$

With: $P_{OUT1} = \frac{V_{OUT}^2}{R_{L1}}$

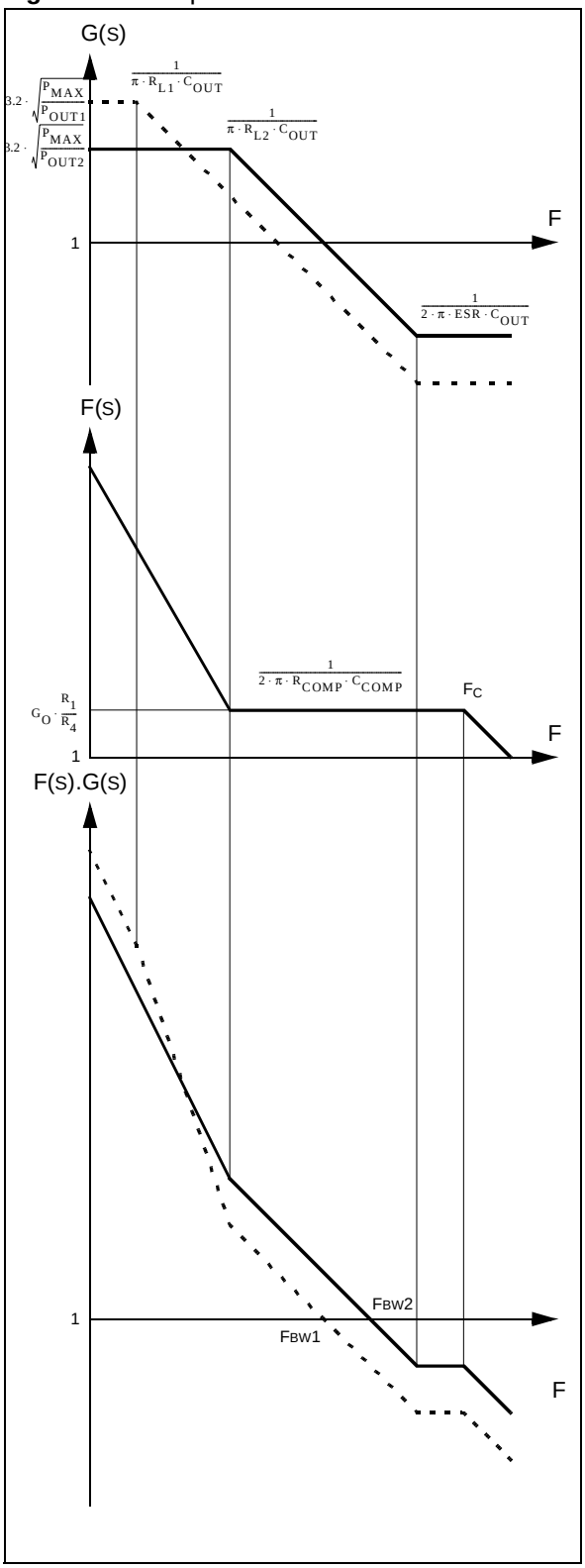
The above formula gives a minimum value for C_1. It can be then increased to provide a natural soft start function as this capacitor is charged by the error amplifier current capacity I_{COMP} at start-up.

SPECIAL RECOMMENDATIONS

A capacitor of 10 nF (minimum value: 8 nF) should always be connected to the COMP pin to insure a correct stability of the internal current source. This is represented on figure 11.

In order to improve the ruggedness of the device versus eventual drain overvoltages, a resistance of 1 kΩ should be inserted in series with the TOVL pin, as shown on figure 11. Note that this resistance doesn't impact the overload delay, as its value is negligeable in front of the internal pull up resistance (about 125 kΩ).

Figure 20: Complete Converter Transfer Function



SOFTWARE IMPLEMENTATION

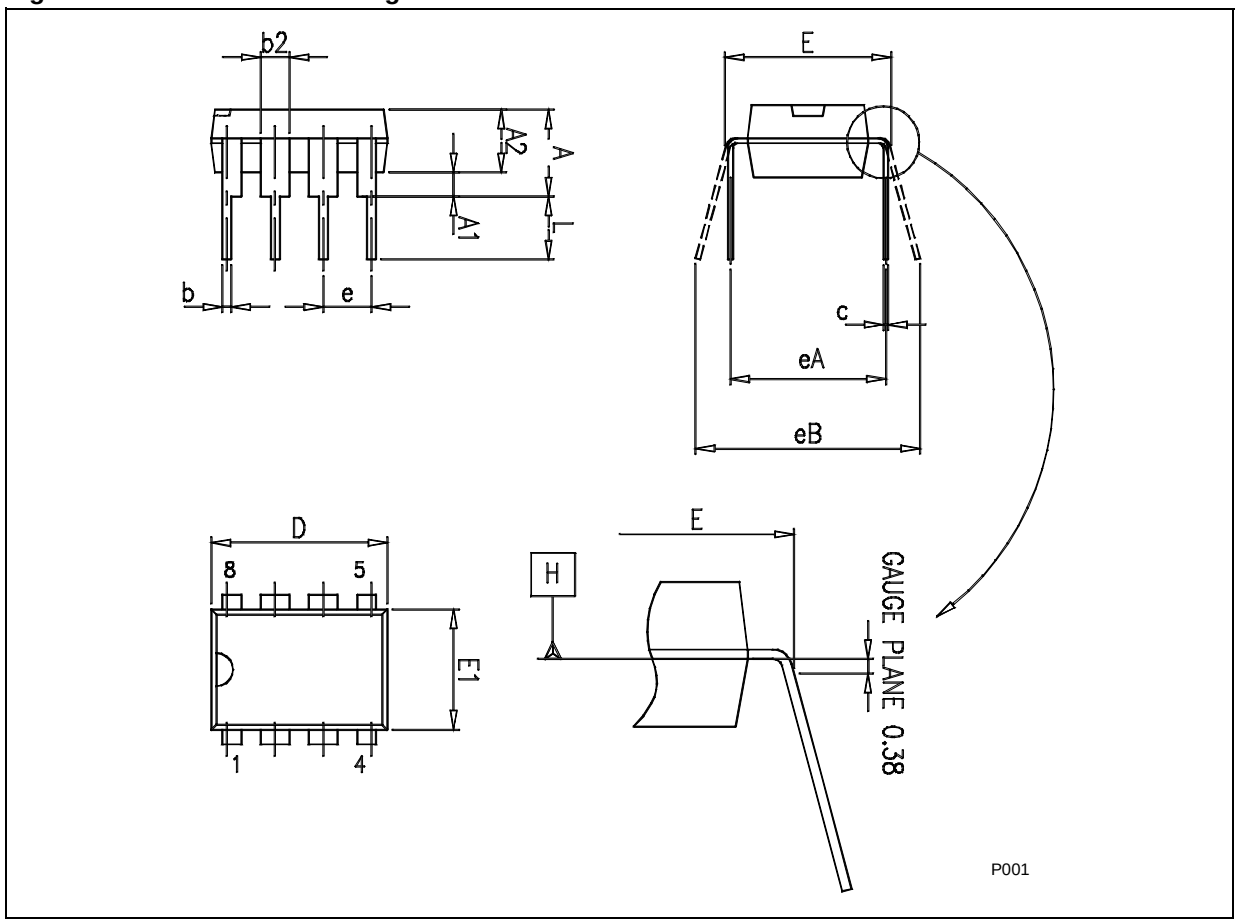
All the above considerations and some others are included in a design software which provides all the needed components around the VIPer device for a specified output configuration. This software is available in download on the ST internet site.

PACKAGE MECHANICAL

Table 12. Plastic DIP-8 Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.26
E1	6.10	6.35	7.11
e		2.54	
eA		7.62	
eB			10.92
L	2.92	3.30	3.81
Package Weight	Gr. 470		

Figure 21. Plastic DIP-8 Package Dimensions



PACKAGE MECHANICAL

Table 13. PowerSO-10™ Mechanical Data

Symbol	millimeters		
	Min	Typ	Max
A	3.35		3.65
A (*)	3.4		3.6
A1	0.00		0.10
B	0.40		0.60
B (*)	0.37		0.53
C	0.35		0.55
C (*)	0.23		0.32
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E2	7.20		7.60
E2 (*)	7.30		7.50
E4	5.90		6.10
E4 (*)	5.90		6.30
e		1.27	
F	1.25		1.35
F (*)	1.20		1.40
H	13.80		14.40
H (*)	13.85		14.35
h		0.50	
L	1.20		1.80
L (*)	0.80		1.10
a	0º		8º
α (*)	2º		8º

Note: (*) Muar only POA P013P

Figure 22. PowerSO-10™ Package Dimensions

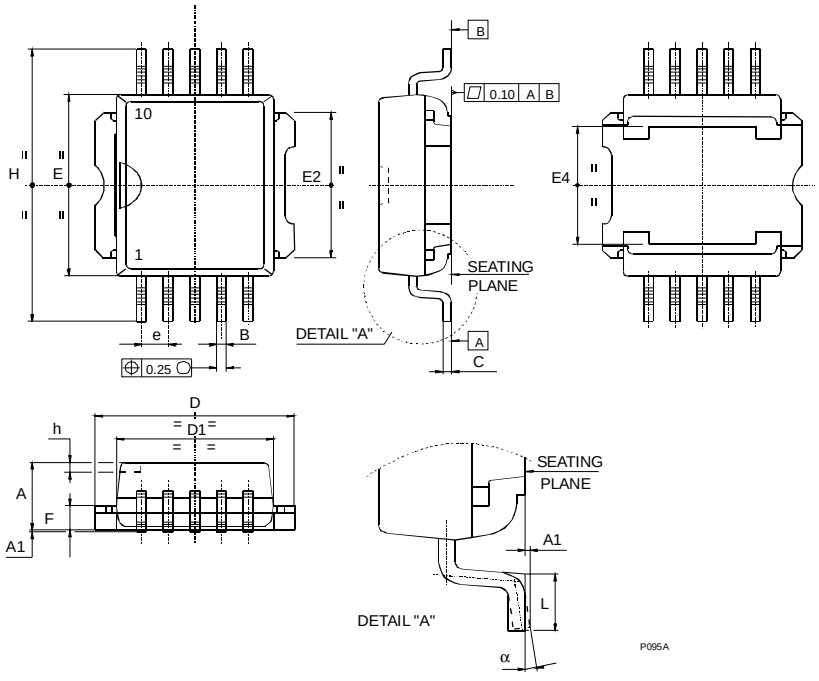
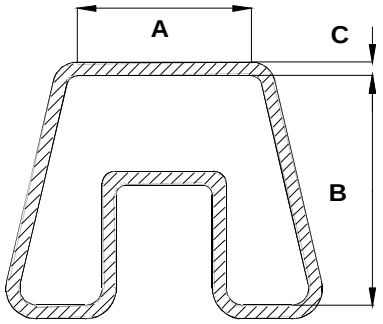


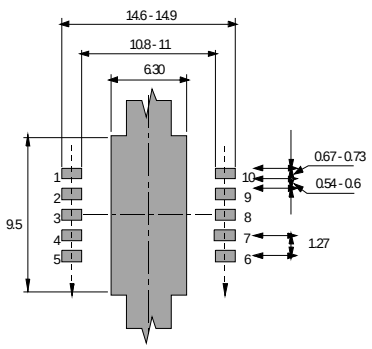
Figure 23. Plastic DIP-8 Tube Shipment (No Suffix)

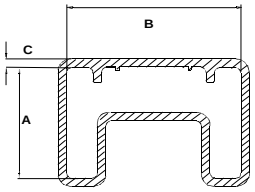


Base Q.ty	20
Bulk Q.ty	1000
Tube length (± 0.5)	532
A	8.4
B	11.2
C (± 0.1)	0.8

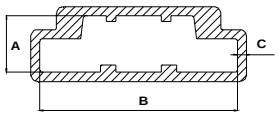
All dimensions are in mm.

Figure 24. PowerSO-10™ Suggested Pad Layout And Tube Shipment (No Suffix)





CASABLANCA

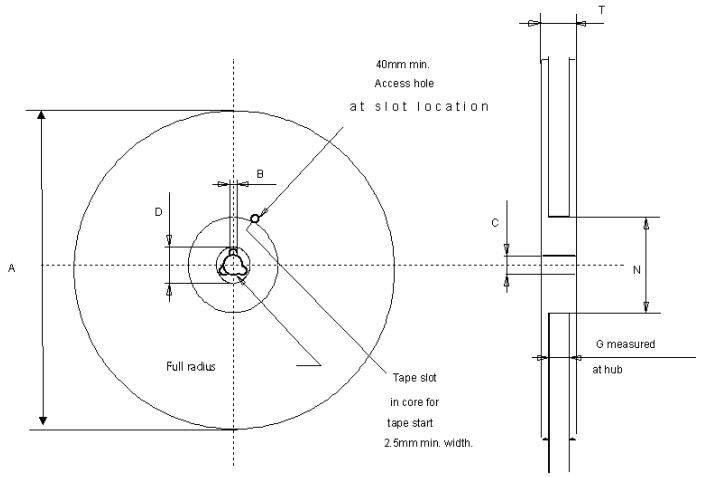


MUAR

All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

Figure 25. Tape And Reel Shipment (suffix "13TR")



REEL DIMENSIONS

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

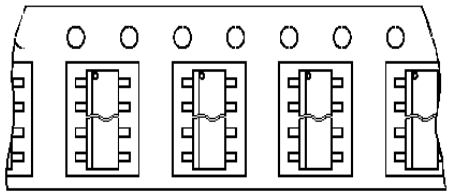
All dimensions are in mm.

TAPE DIMENSIONS

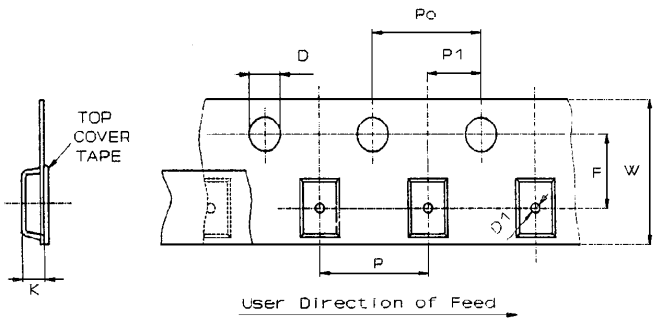
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb. 1986

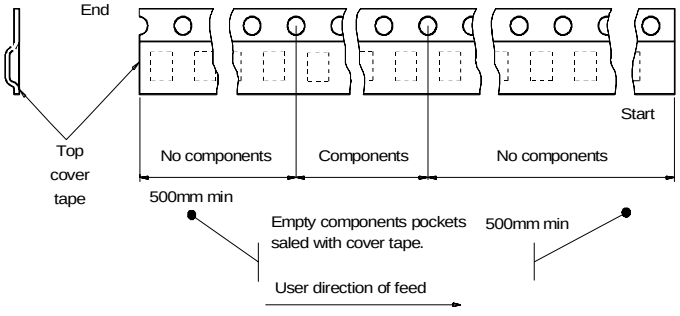
Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	24
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.



User Direction of Feed





REVISION HISTORY

Table 14. Revision History

Date	Revision	Description of Changes
31-Aug-2004	1	- First Issue