Advanced Power MOSFET

SSH80N06A

FEATURES

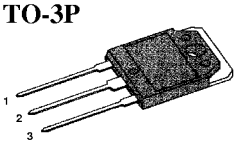
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- 175°C Operating Temperature
- Lower Leakage Current : 10 μA (Max.) @ V_{DS} = 60V
- Lower $R_{DS(ON)}$: 0.008 Ω (Typ.)

BV_{DSS} = 60 V

$R_{DS(on)}$ = 0.01 Ω

I_D = 85 A

TO-3P



1.Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	60	V
I_D	Continuous Drain Current (T_C=25°C)	85	A
	Continuous Drain Current (T_C=100°C)	60	
I_{DM}	Drain Current-Pulsed ¤	297	A
V_{GS}	Gate-to-Source Voltage	¡ 20	V
E_{AS}	Single Pulsed Avalanche Energy ¤ Ł	3700	mJ
I_{AR}	Avalanche Current ¤	85	A
E_{AR}	Repetitive Avalanche Energy ¤	18	mJ
dv/dt	Peak Diode Recovery dv/dt ¤ Ø	5.5	V/ns
P_D	Total Power Dissipation (T_C=25°C)	180	W
	Linear Derating Factor	1.2	W/°C
T_J , T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +175	°C
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8£ ¢from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	0.83	°C/W
$R_{\theta CS}$	Case-to-Sink	0.24	--	
$R_{\theta JA}$	Junction-to-Ambient	--	40	

SAMSUNG ELECTRONICS

Electrical Characteristics (T_C=25¡ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	60	--	--	V	V_{GS}=0V,I_D=250¥ A
¥ BV/¥ T_J	Breakdown Voltage Temp. Coeff.	--	0.046	--	V/¡	I_D=250¥ A ***See Fig 7***
$V_{GS(th)}$	Gate Threshold Voltage	2.0	--	4.0	V	V_{DS}=5V,I_D=250¥ A
I_{GSS}	Gate-Source Leakage , Forward	--	--	100	nA	V_{GS}=20V
	Gate-Source Leakage , Reverse	--	--	-100		V_{GS}=-20V
I_{DSS}	Drain-to-Source Leakage Current	--	--	10	¥ A	V_{DS}=60V
		--	--	100		V_{DS}=48V,T_C=150¡
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.01	§	V_{GS}=10V,I_D=42.5A ¤ Œ
g_{fs}	Forward Transconductance	--	49	--	§	V_{DS}=30V,I_D=42.5A ¤ Œ
C_{iss}	Input Capacitance	--	4630	6020	pF	V_{GS}=0V,V_{DS}=25V,f =1MHz ***See Fig 5***
C_{oss}	Output Capacitance	--	1220	1400		
C_{rss}	Reverse Transfer Capacitance	--	375	440		
$t_{d(on)}$	Turn-On Delay Time	--	22	55	ns	V_{DD}=30V,I_D=85A, R_G=4.8§ ***See Fig 13*** ¤ Œ º
t_r	Rise Time	--	15	40		
$t_{d(off)}$	Turn-Off Delay Time	--	163	335		
t_f	Fall Time	--	64	140		
Q_g	Total Gate Charge	--	153	200	nC	V_{DS}=48V,V_{GS}=10V, I_D=85A ***See Fig 6 & Fig 12*** ¤ Œ º
Q_{gs}	Gate-Source Charge	--	33	--		
Q_{gd}	Gate-Drain(£ Miller£)¢ Charge	--	61	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	85	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ¤	--	--	297		
V_{SD}	Diode Forward Voltage ¤ Œ	--	--	1.5	V	T_J=25¡ ,I_S=85A,V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	92	--	ns	T_J=25¡ ,I_F=85A
Q_{rr}	Reverse Recovery Charge	--	0.3	--	¥ C	di_F/dt=100A/¥ s ¤ Œ

Notes ;

¤ Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature

¤ ŁL=0.6mH, I_{AS}=85A, V_{DD}=25V, R_G=27§ , Starting T_J=25¡

¤ Ø$_{SD}$¡ ´85A, di/dt¡ ´400A/¥ s, V_{DD}¡ ´BV_{DSS}, Starting T_J=25¡

¤ ŒPulse Test : Pulse Width = 250¥ s, Duty Cycle ¡ ´2%

¤ ºEssentially Independent of Operating Temperature

Fig 1. Output Characteristics

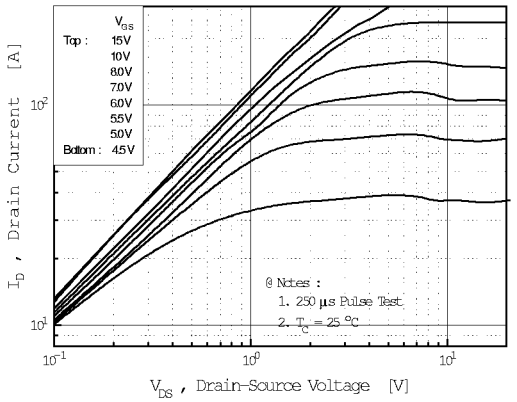


Fig 2. Transfer Characteristics

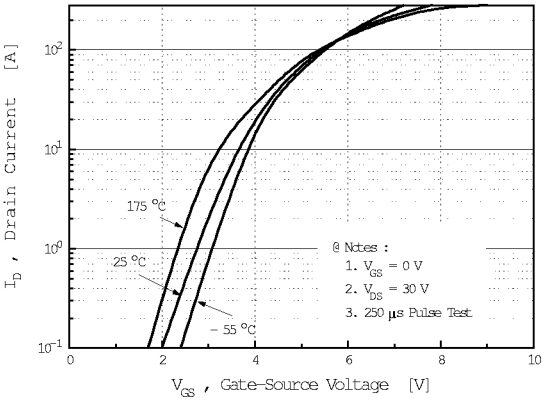


Fig 3. On-Resistance vs. Drain Current

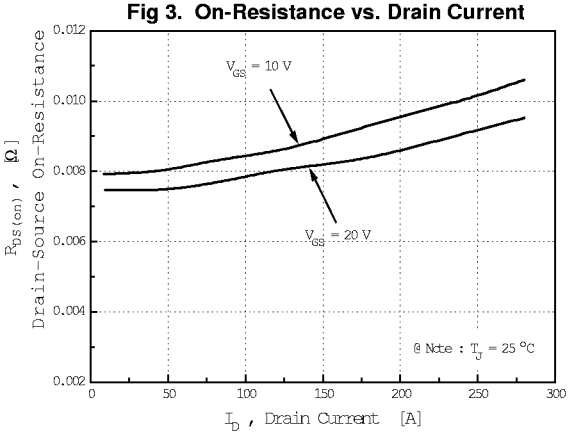


Fig 4. Source-Drain Diode Forward Voltage

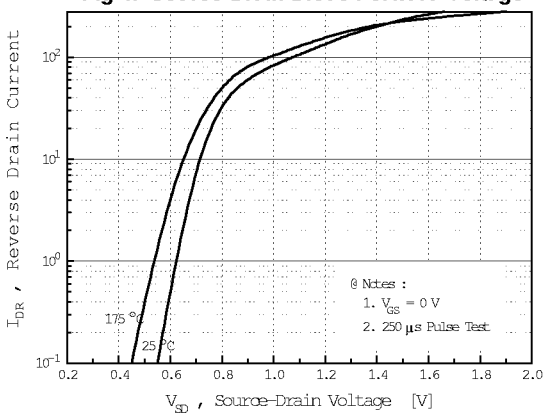


Fig 5. Capacitance vs. Drain-Source Voltage

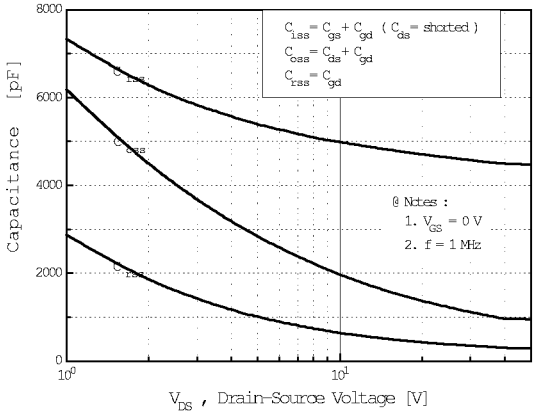


Fig 6. Gate Charge vs. Gate-Source Voltage

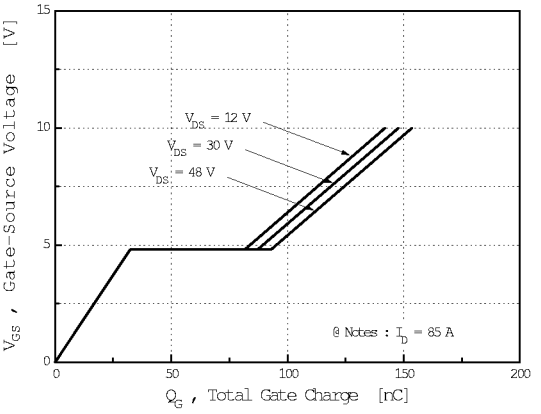


Fig 7. Breakdown Voltage vs. Temperature

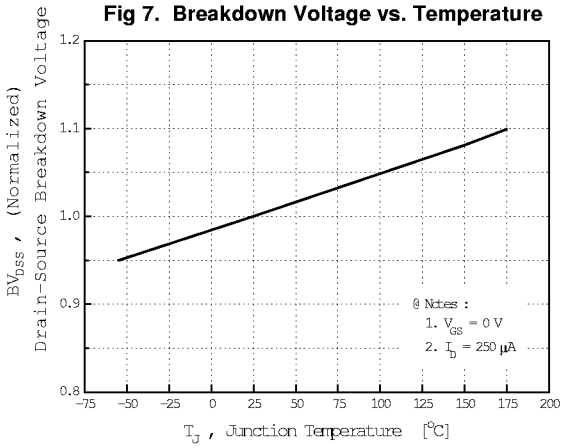


Fig 8. On-Resistance vs. Temperature

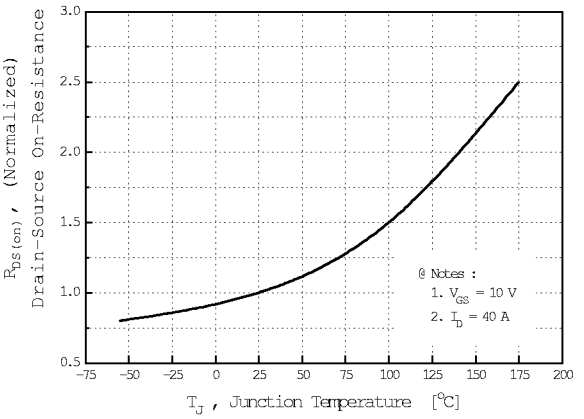


Fig 9. Max. Safe Operating Area

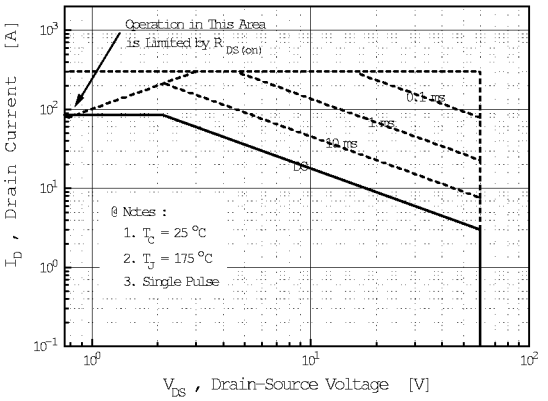


Fig 10. Max. Drain Current vs. Case Temperature

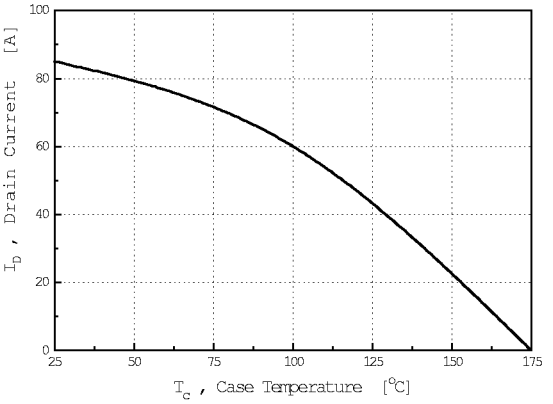


Fig 11. Thermal Response

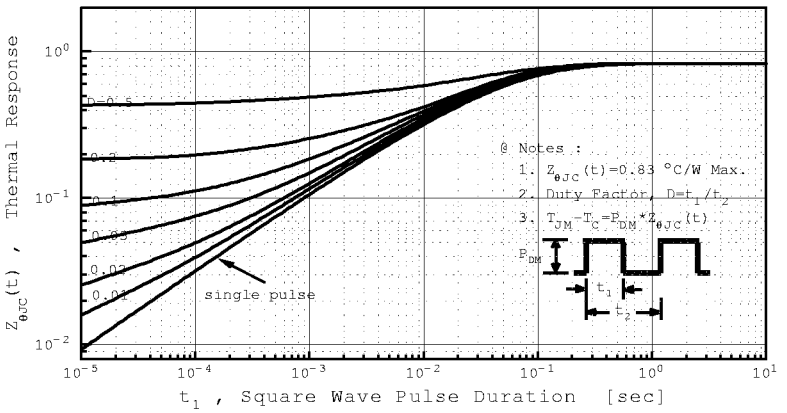


Fig 12. Gate Charge Test Circuit & Waveform

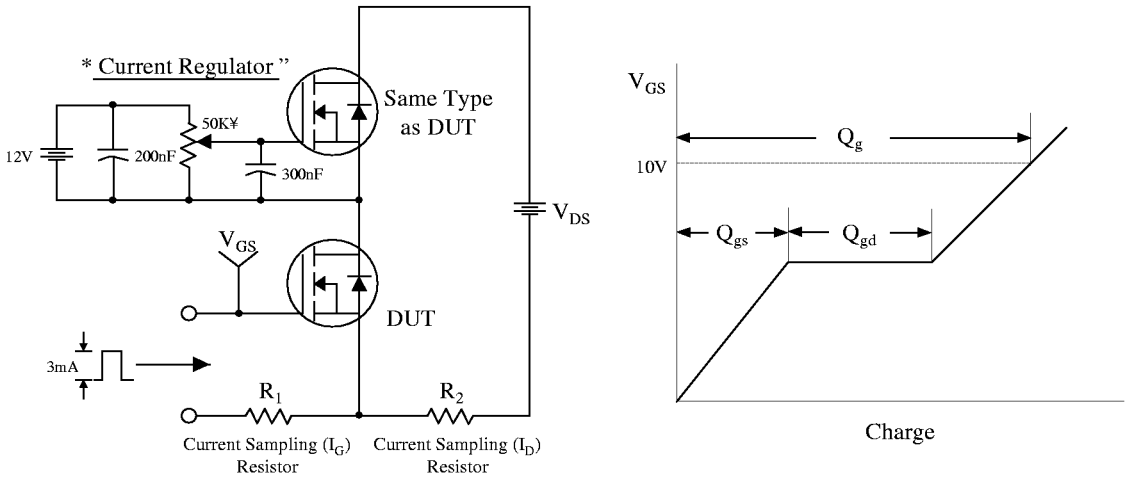


Fig 13. Resistive Switching Test Circuit & Waveforms

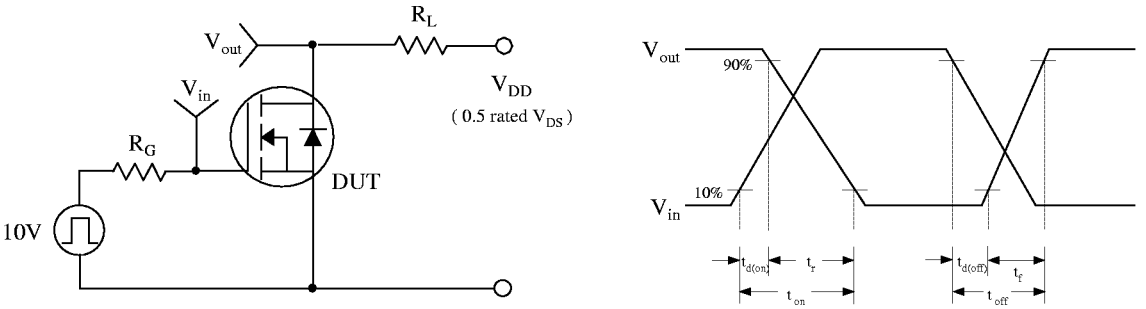


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

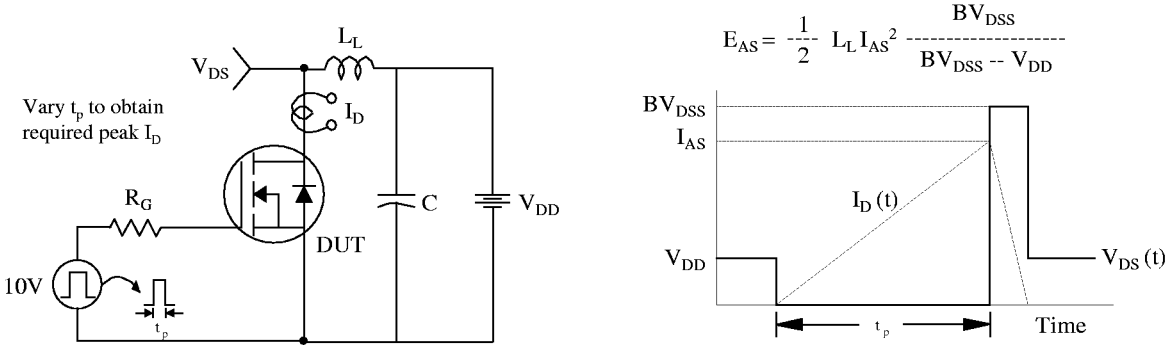


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms