Digital servo processor and Compact Disc decoder (CD7)

SAA7370A

FEATURES

- CD-ROM mode
- Up to 8 times-speed mode
- Lock-to-disc mode
- Full error correction strategy, t = 2 and e = 4
- Full CD graphics interface
- All standard decoder functions implemented digitally on chip
- FIFO overflow concealment for rotational shock resistance
- Digital audio interface (EBU), audio and data
- 2 and 4 times oversampling integrated digital filter, including f_s mode
- Audio data peak level detection
- Kill interface for DAC deactivation during digital silence
- All TDA1301 (DSIC2) digital servo functions, plus extra high level functions
- Low focus noise
- Improved playability on ABEX TCD-721R, TCD-725 and TCD-714 discs
- Automatic closed-loop gain control available for focus and radial loops
- Pulsed sledge support
- Up to 80 kHz (8.4672 MHz crystal) or 16 MHz (16.9344 MHz crystal) jump performance
- Electronic damping of fast radial actuator during long jump
- Microcontroller loading LOW
- High level servo control option
- High level mechanism monitor
- Communication may be via TDA1301/SAA7345 compatible bus or I²C-bus
- On-chip clock multiplier allows the use of 8.4672 MHz crystal for up to 4 times speed mode or 16.9344 MHz crystal for up to 8 times-speed mode.

GENERAL DESCRIPTION

The SAA7370A (CD7) is a single chip combining the functions of a CD decoder IC and digital servo IC. The decoder part is based on the SAA7345 (CD6) with an improved error correction strategy. The servo part is based on the TDA1301T (DSIC2) with improvements incorporated, extra features have also been added.

Supply of this Compact Disc IC does not convey an implied license under any patent right to use this IC in any Compact Disc application.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		4.75	5.0	5.25	V
I_{DD}	supply current	n = 1 mode	–	49	–	mA
f_{xtal}	crystal frequency		8	8.4672	35	MHz
T_{amb}	operating ambient temperature		0	–	+70	°C
T_{stg}	storage temperature		–55	–	+125	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7370A	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 × 14 × 2.7 mm	SOT393-1

FOR MORE DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC01 OR DATA SHEET

BLOCK DIAGRAM

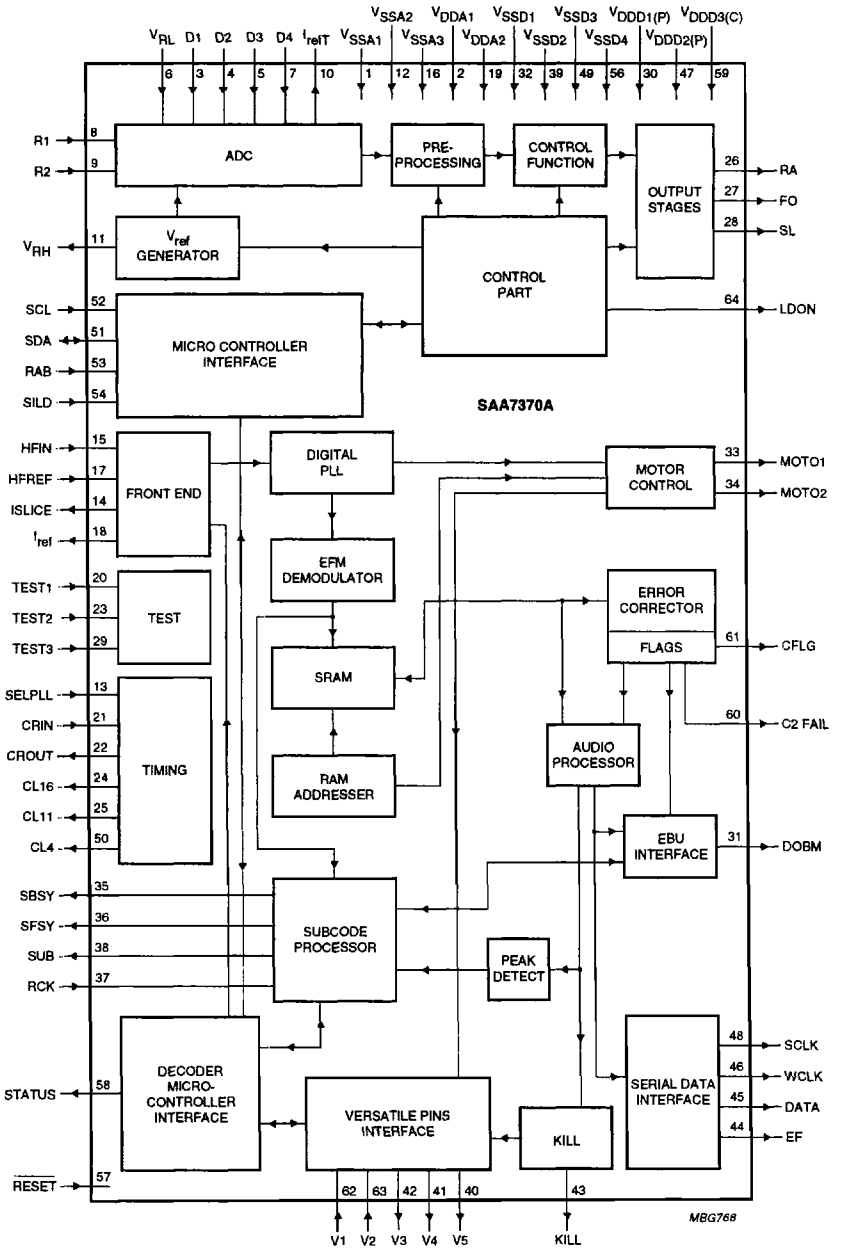

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{SSA1}	1[1]	analog ground 1
V_{DDA1}	2[1]	analog supply voltage 1
D1	3	unipolar current input (central diode signal input)
D2	4	unipolar current input (central diode signal input)
D3	5	unipolar current input (central diode signal input)
V_{RL}	6	reference voltage input for ADC
D4	7	unipolar current input (central diode signal input)
R1	8	unipolar current input (satellite diode signal input)
R2	9	unipolar current input (satellite diode signal input)
I_{refT}	10	current reference output for ADC calibration
V_{RH}	11	reference voltage output from ADC
V_{SSA2}	12[1]	analog ground 2
SELPLL	13	selects whether internal clock multiplier PLL is used
ISLICE	14	current feedback output from data slicer
HFIN	15	comparator signal input
V_{SSA3}	16[1]	analog ground 3
HFREF	17	comparator common mode input
I_{ref}	18	reference current output pin (nominally $0.5V_{DD}$)
V_{DDA2}	19[1]	analog supply voltage 2
TEST1	20	test control input 1; this pin should be tied LOW
CRIN	21	crystal/resonator input
CROUT	22	crystal/resonator output
TEST2	23	test control input 2; this pin should be tied LOW
CL16	24	16.9344 MHz (or 33.8688 MHz) system clock output
CL11	25	11.2896 or 5.6448 MHz (or 22.5792 MHz) clock output (3-state)
RA	26	radial actuator output
FO	27	focus actuator output
SL	28	sledge control output
TEST3	29	test control input 3; this pin should be tied LOW
$V_{DDD1(P)}$	30[1]	digital supply voltage 1 for periphery
DOBM	31	bi-phase mark output (externally buffered; 3-state)
V_{SSD1}	32[1]	digital ground 1
MOTO1	33	motor output 1; versatile (3-state)
MOTO2	34	motor output 2; versatile (3-state)
SBSY	35	subcode block sync output (3-state)
SFSY	36	subcode frame sync output (3-state)
RCK	37	subcode clock input
SUB	38	P-to-W subcode bits output (3-state)
V_{SSD2}	39[1]	digital ground 2
V5	40	versatile output pin 5

SYMBOL	PIN	DESCRIPTION
V4	41	versatile output pin 4
V3	42	versatile output pin 3 (open-drain)
KILL	43	kill output (programmable; open-drain)
EF	44	C2 error flag; output only defined in CD ROM modes (3-state)
DATA	45	serial data output (3-state)
WCLK	46	word clock output (3-state)
$V_{DDD2(P)}$	47[1]	digital supply voltage 2 for periphery
SCLK	48	serial bit clock output (3-state)
V_{SSD3}	49[1]	digital ground 3
CL4	50	4.2336 MHz (or 8.4672 MHz) microcontroller clock output
SDA	51	microcontroller interface data I/O line (open-drain output)
SCL	52	microcontroller interface clock line input
RAB	53	microcontroller interface R/$\overline{W}$ and load control line input (4-wire bus mode)
SILD	54	microcontroller interface $\overline{R}$/W and load control line input (4-wire-bus mode)
n.c.	55	not connected
V_{SSD4}	56[1]	digital ground 4
$\overline{RESET}$	57	power-on reset input (active LOW)
STATUS	58	servo interrupt request line/decoder status register output (open-drain)
$V_{DDD3(C)}$	59[1]	digital supply voltage 3 for core
C2FAIL	60	indication of correction failure output (open-drain)
CFLG	61	correction flag output (open-drain)
V1	62	versatile input pin 1
V2	63	versatile input pin 2
LDON	64	laser drive on output (open-drain)

Note

1. All supply pins must be connected to the same external power supply voltage.

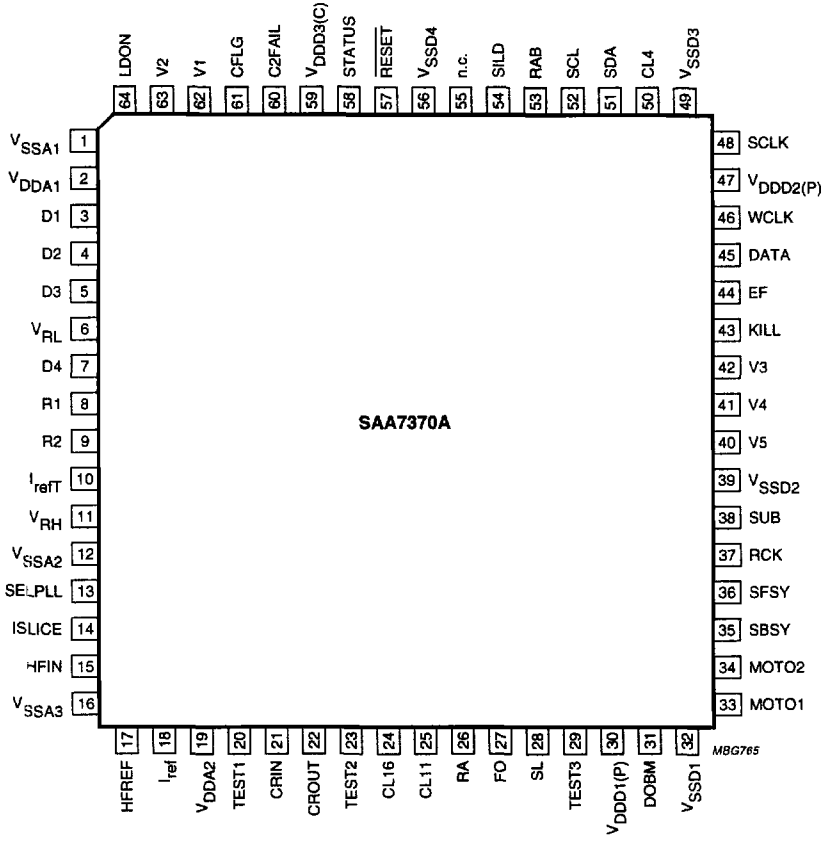

Fig.2 Pin configuration.