

OKI SemiconductorThis version: Jan. 1998
Previous version: Nov. 1996**Preliminary****MSM66585/586/587/P587/Q587****Built-in 16 bit PWM and 8 bit A/D Converter, High-speed High-performance 16 bit Microcontroller****GENERAL DESCRIPTION**

MSM66585/586/587 are high-performance CMOS 16-bit microcontrollers that integrate a 16-bit CPU, ROM, RAM, 8-bit A/D converter, serial port, timers, and PWM. They also allow ROM and RAM to be expanded externally.

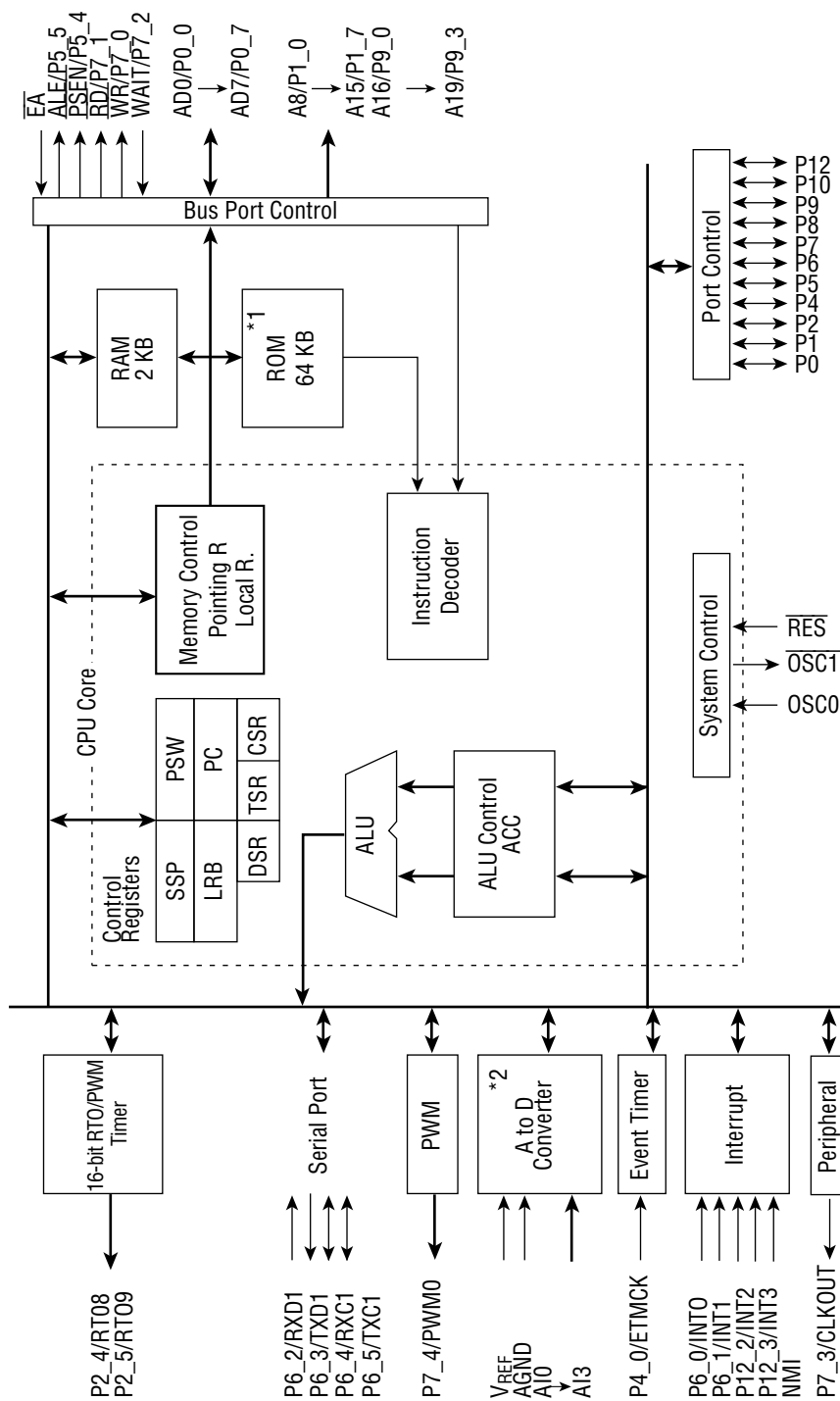
The MSM66P587 is of OTP (One-Time PROM) version and the MSM66Q587 is of Flash EEPROM version.

FEATURES

- Powerful instruction set
 - Instruction set superior in orthogonal matrices
 - 8/16-bit arithmetic instructions
 - Multiply/divide instructions
 - Bit manipulation instructions
 - Bit logical operation instructions
 - ROM table reference instructions
- Abundant addressing modes
 - Register addressing
 - Page addressing
 - Pointer register indirect addressing
 - Stack addressing
 - Immediate addressing
- Minimum instruction cycle
 - 100 ns at 20 MHz (4.5V-5.5V)
 - 200 ns at 10 MHz (2.7V-5.5V)
- Program memory (ROM)
 - Internal: 64 KB (M66587/M66P587/M66Q587), 48 KB (M66585/586)
 - External: 1 MB, EA pin active
- Data memory (RAM)
 - Internal: 2 KB
 - External: 1022 KB
- I/O ports
 - Analog input-only port: 4 lines (test pins for M66585)
 - Input/output port: Maximum 80 lines (40 lines with programmable pull-up)
- Timers
 - Free-running counter: 16-bit × 1
 - Realtime output: 16-bit × 2
 - General autoreload timer: 8-bit × 1
- 16-bit PWM
 - Input clock divider: 1 divider
- 8-bit serial port
 - Synchronous with BRG: 1 port

- A/D converter
 - 8-bit resolution: 4 channels
- Interrupts
 - Non-maskable: 1 interrupt
 - Maskable: 9 internal, 4 external (12 vectors)
 - 3-level priority
- ROM window function
- Standby modes
 - Halt mode
 - Stop mode
- Package
 - 100-pin TQFP (TQFP100-P-1414-0.50-K) (Product name : MSM66585TS-K)
 - (Product name : MSM66586TS-K)
 - (Product name : MSM66587TS-K)
 - (Product name : MSM66P587TS-K)
 - (Product name : MSM66Q587TS-K)

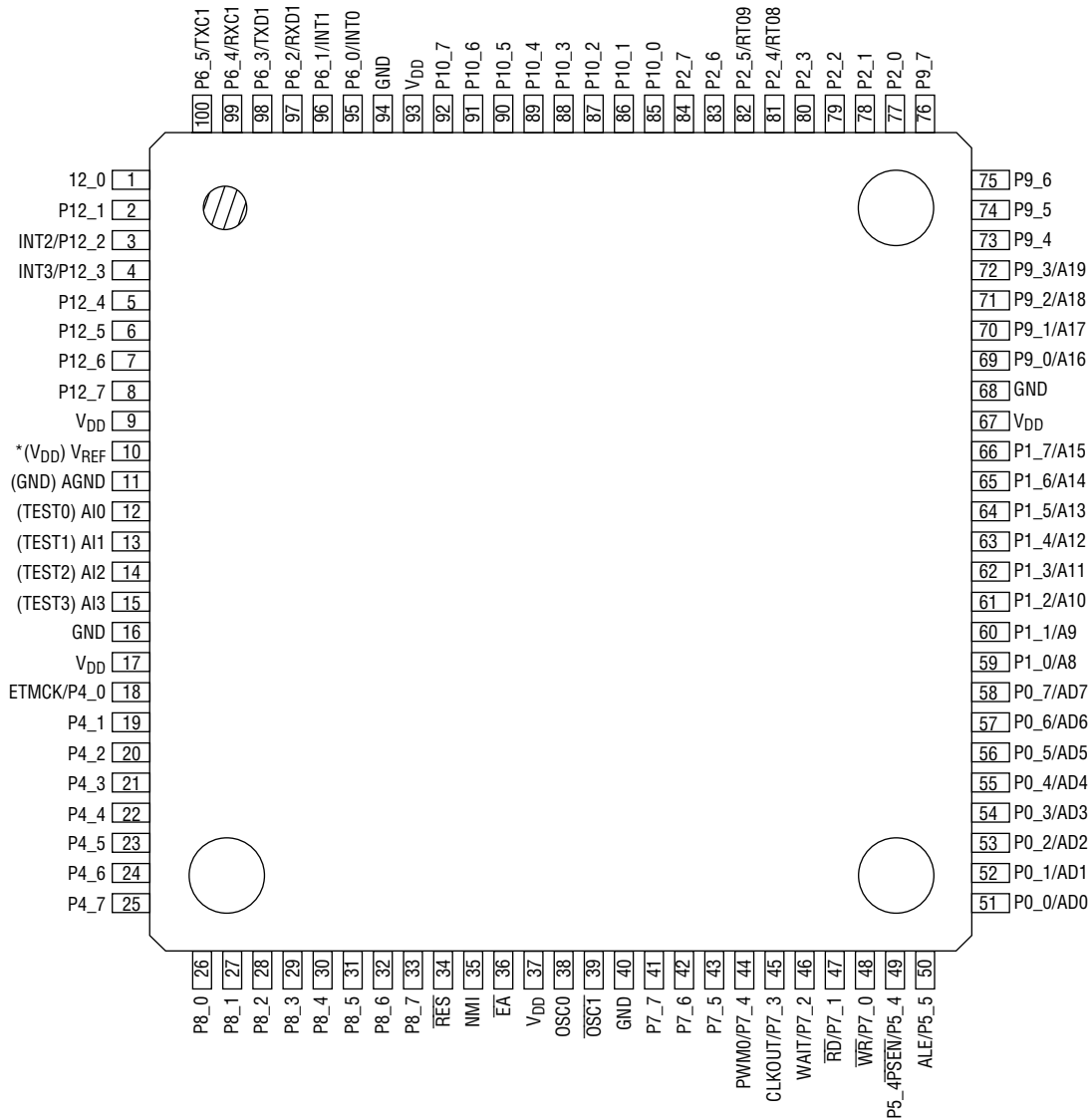
BLOCK DIAGRAM



*1. 48KB for M66585 and M66586.

*2. M66585 has no internal A/D converter.

PIN CONFIGURATION (TOP VIEW)



* For MSM66585, pin name is in parentheses ().

PIN DESCRIPTIONS

Symbol	Type	Description
P0_0-P0_7/ AD0-AD7	I/O	Port 0 is 8 input/output pins. Input or output can be specified for each bit with the Port 0 Mode Register (P0IO). Pull-up resistors can be specified for each bit with the Port 0 Pull-Up Register (P0PUP). These pins also function as time-multiplexed address outputs and data input/output pins (AD0-AD7) when accessing memory that has been expanded externally (program or data memory). After reset (by RES signal input, BRK instruction execution, or op code trap), P0 will be high-impedance inputs.
P1_0-P1_7/ A8-A15	I/O	Port 1 is 8 input/output pins. Input or output can be specified for each bit with the Port 1 Mode Register (P1IO). Pull-up resistors can be specified for each bit with the Port 1 Pull-Up Register (P1PUP). P1_0-P1_7 also have a secondary function as input/output pins for internal operation. Their secondary function can be set for each bit with the Port 1 Secondary Function Control Register (P1SF). The input/output settings by P1IO will be ignored for pins that have been set to the secondary function by P1SF. These pins function as output pins for address A8-A15 when accessing program memory or data memory that has been expanded externally. When the EA pin is low, A8-A15 will be output regardless of P1SF settings. After reset (by RES signal input, BRK instruction execution, or op code trap), P1 will be high-impedance inputs.
P2_0-P2_3 P2_4-P2_5/ RT08-RT09 P2_6-P2_7	I/O	P2_4 and P2_5 also have a secondary function as input/output pins for internal operation. Their secondary function can be set for each bit with the Port 2 Secondary Function Control Register (P2SF). The input/output settings of P2IO will be ignored for pins that have been set to the secondary function by P2SF. These pins output a previously set level when the value of Timer Registers 8 and 9 match a selected counter value. After reset (by RES signal input, BRK instruction execution, or op code trap), P2 will be high-impedance inputs.
P4_0/ETMCK P4_1-P4_7	I/O	Port 4 is 8 input/output pins. Input or output can be specified for each bit with the Port 4 Mode Register (P4IO). Pull-up resistors can be specified for each bit with the Port 4 Pull-Up Register (P4PUP). P4_0 also has a secondary function as an input pin for internal operation. Its secondary function can be set for the bit with the Port 4 Secondary Function Control Register (P4SF). The input/output settings by P4IO will be ignored for pins that have been set to the secondary function by P4SF. This is the external clock input pin for the counter of a general 8-bit timer. After reset (by RES signal input, BRK instruction execution, or op code trap), P4 will be high-impedance inputs.
P5_4/PSEN P5_5/ALE	I/O	Port 5 is 2 input/output pins. Input or output can be specified for each bit with the Port 5 Mode Register (P5IO). P5_4 and P5_5 also have a secondary function as output pins for internal operation. Their secondary function can be set for each bit with the Port 5 Secondary Function Control Register (P5SF). The input/output settings of P5IO will be ignored for pins that have been set to the secondary function by P5SF. PSEN (P5_4): This pin outputs the strobe signal for read operations when external program memory is accessed. Operation will automatically switch to the secondary function when the EA pin is low. This pin will be pulled up when both the EA pin and RESET pin are low. ALE (P5_5): This pin outputs the strobe for externally latching the lower 8 address bits output from P0 when external memory is accessed. Operation will automatically switch to the secondary function when the EA pin is low. This pin will be pulled up when both the EA pin and RESET pin are low. After reset (by RES signal input, BRK instruction execution, or op code trap), P5 will be high-impedance inputs.

PIN DESCRIPTIONS (Continued)

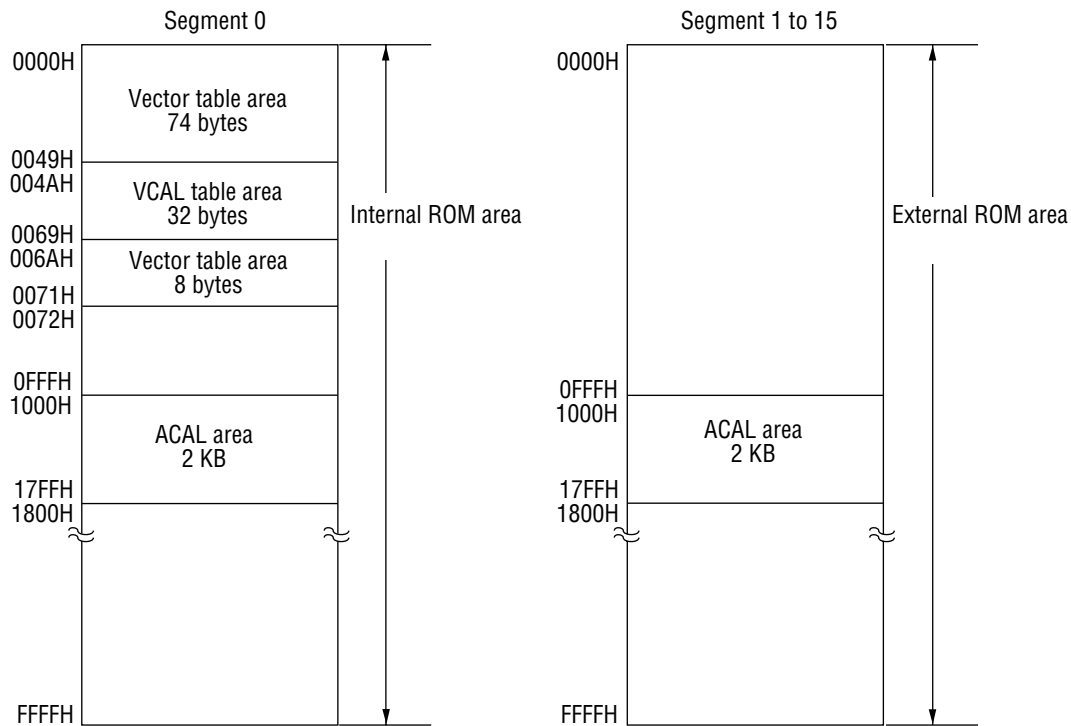
Symbol	Type	Description
P6_0/INT0 P6_1/INT1 P6_2/RXD1 P6_3/TXD1 P6_4/RXC1 P6_5/TXC1	I/O	Port 6 is 6 input/output pins. Input or output can be specified for each bit with the Port 6 Mode Register (P6IO). P6_0-P6_5 also have a secondary function as input/output pins for internal operation. Their secondary function can be set for each bit with the Port 6 Secondary Function Control Register (P6SF). The input/output settings of P6IO will be ignored for pins that have been set to the secondary function by P6SF. INT0 (P5_0), INT1 (P6_1): These pins input external interrupts 0 and 1. RXD1 (P6_2): This pin inputs receive data to the Serial Port 1 receive circuit. TXD1 (P6_3): This pin outputs transmit data to the Serial Port 1 transmit circuit. RXC1 (P6_4): This pin outputs the shift clock when the Serial Port 1 receive circuit is in master mode. It inputs the shift clock when the receive circuit is in slave mode. TXC1 (P6_4): This pin outputs the shift clock when the Serial Port 1 transmit circuit is in master mode. It inputs the shift clock when the transmit circuit is in slave mode. After reset (by RES signal input, BRK instruction execution, or op code trap), P6 will be high-impedance inputs.
P7_0/ $\overline{WR}$ P7_1/ $\overline{RD}$ P7_2/WAIT P7_3/CLKOUT P7_4/PWM0 P7_5-P7_7	I/O	Port 7 is 8 input/output pins. Input or output can be specified for each bit with the Port 7 Mode Register (P7IO). P7_0-P7_4 also have a secondary function as input/output pins for internal operation. Their secondary function can be set for each bit with the Port 7 Secondary Function Control Register (P7SF). The input/output settings of P7IO will be ignored for pins that have been set to the secondary function by P7SF. $\overline{WR}$ (P7_0): This pin outputs the strobe signal for write operations when external data memory is accessed. $\overline{RD}$ (P7_1): This pin outputs the strobe signal for read operations when external data memory is accessed. WAIT (P7_2): This pin inputs a wait to the internal CPU when external data memory with a slow access time is accessed. CPU is driven to "WAIT" state during WAIT pin high. CLKOUT (P7_3): This pin outputs the clock pulses set by the Peripheral Control Register (PRPHF). PWM0 (P7_4): This pin outputs PWM0. After reset (by RES signal input, BRK instruction execution, or op code trap), P7 will be high-impedance inputs. When P7_0 and P7_1 are used as their secondary functions ($\overline{WR}$, $\overline{RD}$), they need to be connected externally to pull-up resistors.
P8_0-P8_7	I/O	Port 8 is 8 input/output pins. Input or output can be specified for each bit with the Port 8 Mode Register (P8IO). After reset (by RES signal input, BRK instruction execution, or op code trap), P8 will be high-impedance inputs.

PIN DESCRIPTIONS (Continued)

Symbol	Type	Description
P9_0-P9_3/ A16-A19 P9_4-P9_7	I/O	Port 9 is 8 input/output pins. Input or output can be specified for each bit with the Port 9 Mode Register (P9IO). Pull-up resistors can be specified for each bit with the Port 9 Pull-Up Register (P9PUP). P9_0-P9_3 also have a secondary function as output pins for internal operation. Their secondary function can be set for each bit with the Port 9 Secondary Function Control Register (P9SF). The input/output settings of P9IO will be ignored for pins that have been set to the secondary function by P9SF. A16-A19 (P9_0-P9_3): These pins function as output pins for address A16-A19 when accessing program memory or data memory that has been expanded externally. Note that program memory address A16-A19 will be output even when accessing data memory that has been expanded externally. When the $\overline{EA}$ pin is low and program memory that has been expanded externally is accessed, A16-A19 will be output regardless of P9SF settings. After reset (by $\overline{RES}$ signal input, BRK instruction execution, or op code trap), P9 will be high-impedance inputs.
P10_0-P10_7	I/O	Port 10 is 8 input/output pins. Input or output can be specified for each bit with the Port 10 Mode Register (P10IO). Pull-up resistors can be specified for each bit with the Port 10 Pull-Up Register (P10PUP). After reset (by $\overline{RES}$ signal input, BRK instruction execution, or op code trap), P10 will be high-impedance inputs.
P12_0-P12_1 P12_2-P12_3/ INT2-INT3 P12_4-P12_7	I/O	Port 12 is 8 input/output pins. Input or output can be specified for each bit with the Port 12 Mode Register (P12IO). P12_2 and P12_3 also have a secondary function as input pins for internal operation. Their secondary function can be set for each bit with the Port 12 Secondary Function Control Register (P12SF). The input/output settings of P12IO will be ignored for pins that have been set to the secondary function by P12SF. INT2 (P12_2), INT3 (P12_3): These pins input external interrupts 2 and 3. After reset (by $\overline{RES}$ signal input, BRK instruction execution, or op code trap), P12 will be high-impedance inputs.
AI0-AI3	I	These are analog input pins for the A/D converter (test pins for MSM66585).
V_{REF}	I	This is the reference voltage pin for the A/D converter (V_{DD} for MSM66585).
AGND	I	This is the ground input pin for the A/D converter (GND for MSM66585).
OSC0	I	This pins connect to a crystal oscillator, ceramic oscillator, or capacitors for base clock oscillation. When the base clock is to be supplied externally, it should be input on the OSC0 pin with the OSC1 pin left open.
$\overline{OSC1}$	O	
NMI	I	This input pin requests a non-maskable interrupt.
$\overline{RES}$	I	This is an active-low reset input pin.
$\overline{EA}$	I	When this pin is high, program addresses 0H-FFFFH will access internal program memory and program addresses 10000H-FFFFFH will access external program memory. To access external program memory, P1, P5, and P9 must be set with their secondary function control registers. When this pin is low, all program addresses will access external program memory.
V_{DD}	I	These are voltage pins. All V_{DD} pins (9, 17, 37, 67, 93) should be connected to the supply voltage (for MSM66585 connect pins 9, 10, 17, 37, 67, 93).
GND	I	These are ground pins. All GND pins (16, 40, 68, 94) should be connected to ground (for MSM66585 connect pins 11, 16, 40, 68, 94).

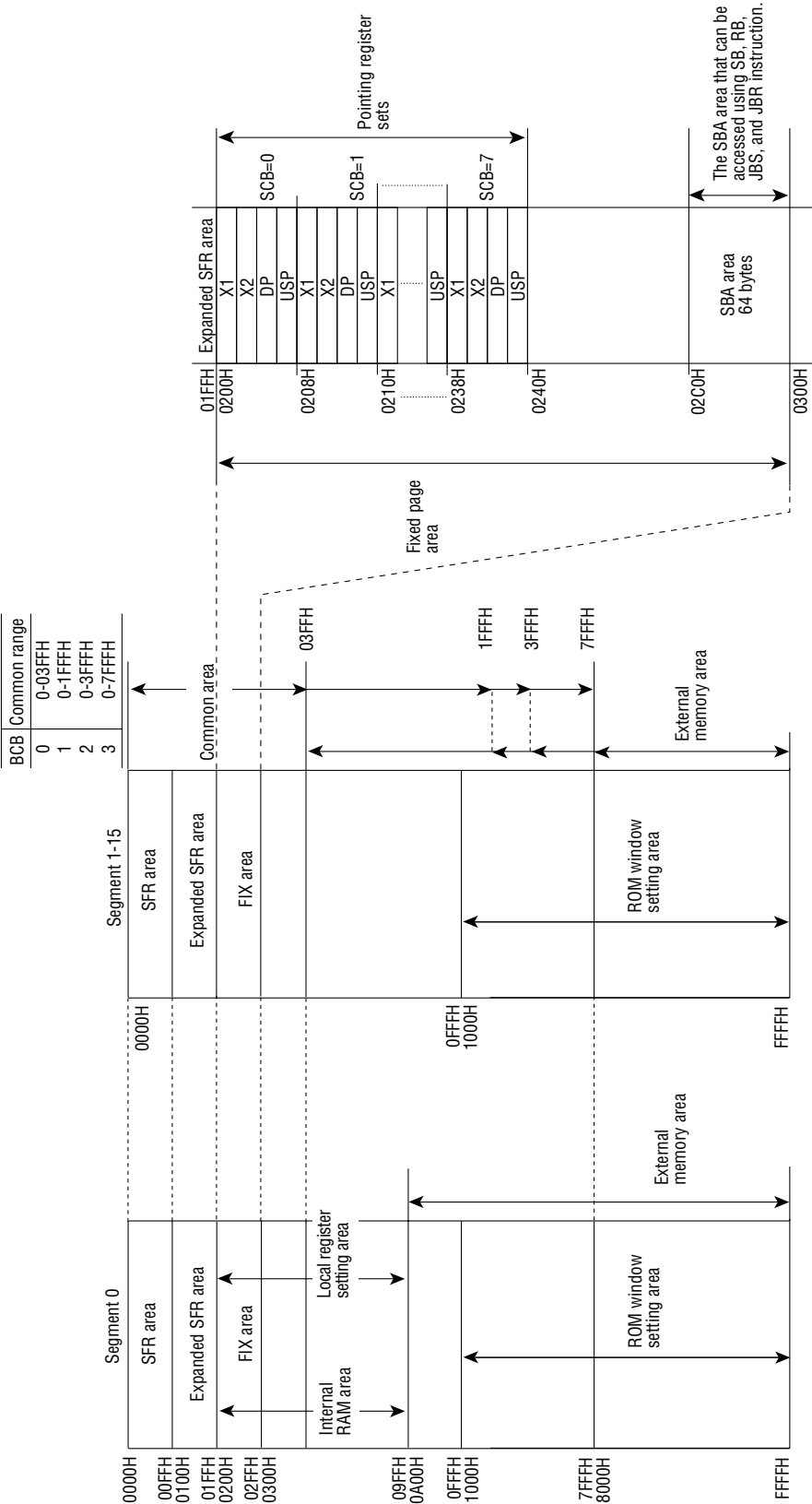
MEMORY MAP

Program Area

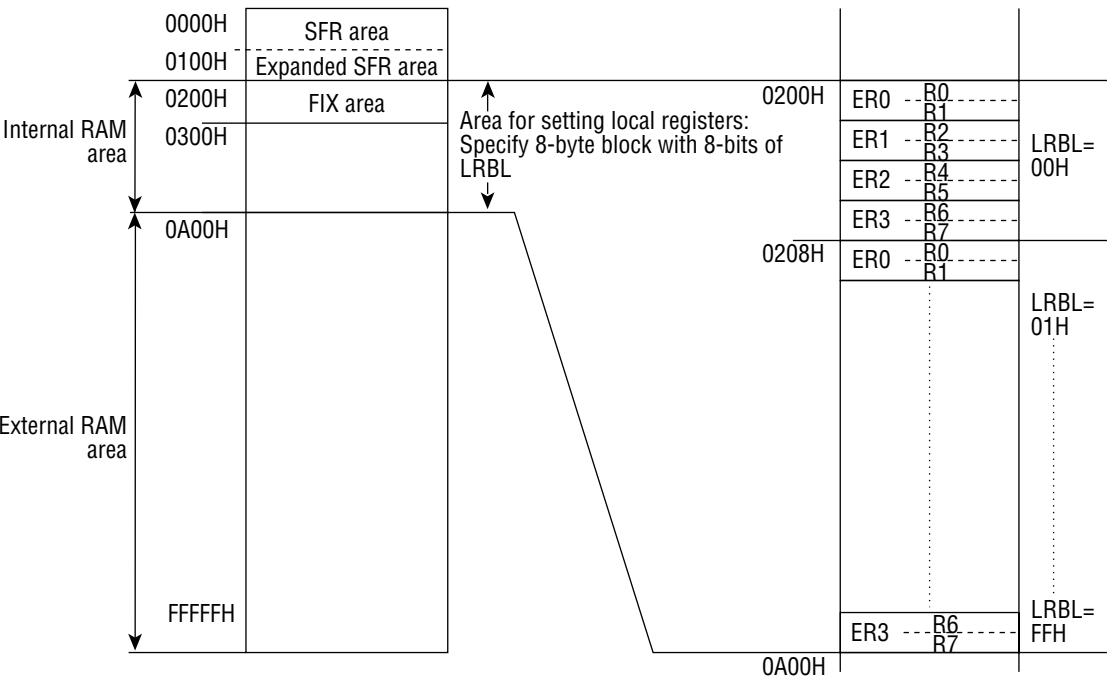


* For M66585 and M66586 addresses 0C000H to 0FFFFFH of segment 0 are external ROM area.

Data Area



Area For Setting Local Registers



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions		Rating	Units
Digital power supply voltage	V_{DD}	GND=AGND=0V $T_a=25^{\circ}\text{C}$		-0.3 to +7.0	V
Input voltage	V_I			-0.3 to $V_{DD}+0.3$	V
Output voltage	V_O			-0.3 to $V_{DD}+0.3$	V
Analog power supply voltage	AV_{DD}			-0.3 to $V_{DD}+0.3$	V
Analog reference voltage	V_{REF}			-0.3 to $AV_{DD}+0.3$	V
Analog input voltage	V_{AI}			-0.3 to V_{REF}	V
Power dissipation	PD	$T_a=70^{\circ}\text{C}$	Per package	650	mW
			Per output	8	mW
Storage temperature	T_{STG}	—		-50 to +150	$^{\circ}\text{C}$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions		Range	Units
Digital power supply voltage	V_{DD}	$f_{OSC} \leq 20\text{MHz}$		4.5 to 5.5	V
		$f_{OSC} \leq 10\text{MHz}$		2.7 to 5.5	
Analog reference voltage	V_{REF}	—		$AV_{DD}-0.3$ to AV_{DD}	V
Analog input voltage	V_{AI}	—		AGND to V_{REF}	V
Memory hold voltage	V_{DDH}	$f_{OSC}=0\text{Hz}$		2.0 to 5.5	V
Operating frequency	f_{OSC}	$V_{DD}=5V \pm 10\%$		2 to 20	MHz
		$V_{DD}=2.7$ to 5.5V		2 to 10	MHz
Temperature range	T_a	—		-30 to +70	$^{\circ}\text{C}$
Fan-out	N	MOS loads		20	—
		TTL loads	P0, P5_4, P5_5, P7_0, P7_1	2	—
			P1, P2, P4, P6, P7_2-P7_7, P8-P10, P12	1	—

ALLOWABLE OUTPUT CURRENT

 $(V_{DD}=2.7$ to 5.5V , $T_a=-30$ to $+70^{\circ}\text{C}$)

Parameter	Pin	Symbol	Min.	Typ.	Max.	Units
"H" output pin (1 pin)	All output pins	I _{OH}	—	—	−2	mA
"H" output pin (total)	Total of all output pins	ΣI _{OH}	—	—	−40	
"L" output pin (1 pin)	All output pins	I _{OL}	—	—	5	
"L" output pin (total)	Total of P0, P1, P5 and P7	ΣI _{OL}	—	—	50	
	Total of P2, P9 and P10					
	Total of P4 and P8					
	Total of P6 and P12					
	Total of all output pins				100	

Note: Power and ground connections must be made to all external V_{DD} and GND pins.

ELECTRICAL CHARACTERISTICS

DC Characteristics ($V_{DD}=5V\pm 10\%$)

(Ta=-30 to +70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input high voltage	V_{IH}	—	0.44V _{DD}	—	V _{DD} +0.3	V
Input high voltage			0.80V _{DD}	—	V _{DD} +0.3	
Input low voltage	V_{IL}	—	-0.3	—	0.16V _{DD}	
Input low voltage			-0.3	—	0.2V _{DD}	
Output high voltage	V_{OH}	I _O =-400μA	V _{DD} -0.4	—	—	
		I _O =-2.0 mA	V _{DD} -0.6	—	—	
Output high voltage		I _O =-200μA	V _{DD} -0.4	—	—	
		I _O =-2.0 mA	V _{DD} -0.6	—	—	
Output low voltage	V_{OL}	I _O =3.2mA	—	—	0.4	
		I _O =5.0mA	—	—	0.8	
Output low voltage		I _O =1.6mA	—	—	0.4	
		I _O =5.0mA	—	—	0.8	
Input leakage current	I_{IH}/I_{IL}	V _I =V _{DD} /0V	—	—	1/-1	μA
Input current			—	—	1/-250	
Input current			—	—	15/-15	
Output leakage current	I_{LO}	V _O =V _{DD} /0V	—	—	±10	μA
Pull-up resistor	R _{pull}	V _I =0V	25	50	100	kΩ
Input capacitance	C _I	f=1MHz, Ta=25°C	—	5	—	pF
Output capacitance	C _O		—	7	—	
Analogue reference power supply current	I _{REF}	A/D conversion operating	—	—	4	mA
		A/D conversion stopped	—	—	10	μA
Supply current (stop mode)	I _{DDS}	V _{DD} =2V, Ta=25°C*	—	0.2	10	μA
		*	—	1	100	
Supply Current (halt mode)	I _{DDH}	f _{OSC} =20MHz, No Load	—	10	25	mA
Supply Current	I _{DD}		—	45	70	

1. Applies to P0.
 2. Applies to P1, P2, P4, P6, P7_2-P7_7, P8-P10, P12.
 3. Applies to A_{in}.
 4. Applies to P5_4, P5_5, P7_0, P7_1.
 5. Applies to $\overline{RES}$.
 6. Applies to $\overline{EA}$, NMI.
 7. Applies to OSC0.
- * For input ports, V_{DD} or 0 V. For other cases, unloaded.

DC Characteristics ($2.7V \leq V_{DD} \leq 5.5V$)

($T_a = -30$ to $+70^\circ\text{C}$)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input high voltage	V_{IH}	—	$0.44V_{DD}$	—	$V_{DD}+0.3$	V
Input high voltage			$0.80V_{DD}$	—	$V_{DD}+0.3$	
Input low voltage	V_{IL}	—	-0.3	—	$0.16V_{DD}$	
Input low voltage			-0.3	—	$0.2V_{DD}$	
Output high voltage	V_{OH}	$I_O = -400\mu\text{A}$	$V_{DD}-0.4$	—	—	V
		$I_O = -2.0\text{ mA}$	$V_{DD}-0.6$	—	—	
Output high voltage		$I_O = -200\mu\text{A}$	$V_{DD}-0.4$	—	—	
		$I_O = -2.0\text{ mA}$	$V_{DD}-0.8$	—	—	
Output low voltage	V_{OL}	$I_O = 3.2\text{mA}$	—	—	0.5	
		$I_O = 5.0\text{mA}$	—	—	0.9	
Output low voltage		$I_O = 1.6\text{mA}$	—	—	0.5	
		$I_O = 5.0\text{mA}$	—	—	1.2	
Input leakage current	I_{IH}/I_{IL}	$V_I = V_{DD}/0V$	—	—	1/-1	μA
Input current			—	—	1/-250	
Input current			—	—	15/-15	
Output leakage current	I_{LO}	$V_O = V_{DD}/0V$	—	—	± 10	μA
Pull-up resistor	R_{pull}	$V_I = 0V, V_{DD} = 5V \pm 10\%$	25	50	100	$k\Omega$
		$V_I = 0V, V_{DD} = 3V \pm 10\%$	40	100	200	
Input capacitance	C_I	$f = 1\text{MHz}, T_a = 25^\circ\text{C}$	—	5	—	pF
Output capacitance	C_O		—	7	—	
Analog reference power supply current	I_{REF}	A/D conversion operating	$V_{DD} = 5.5V$	—	4	mA
			$V_{DD} = 3.3V$	—	2	
		A/D conversion stopped	$V_{DD} = 5.5V$	—	10	μA
			$V_{DD} = 3.3V$	—	5	
Supply current (stop mode)	I_{DDs}	$V_{DD} = 2V, T_a = 25^\circ\text{C}^*$	—	0.2	10	μA
		*	—	1	100	
Supply current (halt mode)	I_{DDH}	$f_{OSC} = 10\text{MHz},$ No Load	$V_{DD} = 5V \pm 10\%$	—	5	mA
			$V_{DD} = 3V \pm 10\%$	—	3	
			$V_{DD} = 5V \pm 10\%$	—	30	
Supply current	I_{DD}		$V_{DD} = 3V \pm 10\%$	—	13	

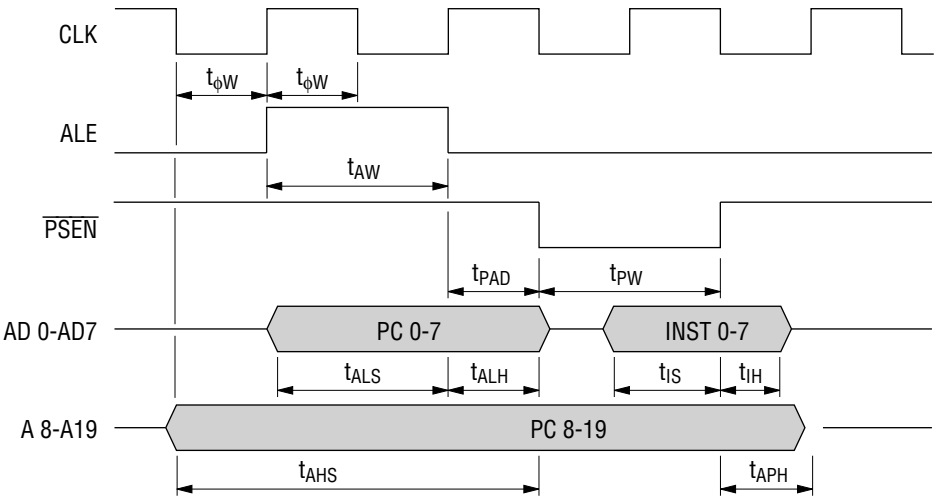
1. Applies to P0.
 2. Applies to P1, P2, P4, P6, P7_2-P7_7, P8-P10, P12.
 3. Applies to Ain.
 4. Applies to P5_4, P5_5, P7_0, P7_1.
 5. Applies to $\overline{RES}$.
 6. Applies to $\overline{EA}$, NMI.
 7. Applies to OSC0.
- * For input ports, V_{DD} or 0 V. For other cases, unloaded.

AC Characteristics (V_{DD}=5V±10%)

- External Program Memory Control

(Ta=−30 to +70°C)

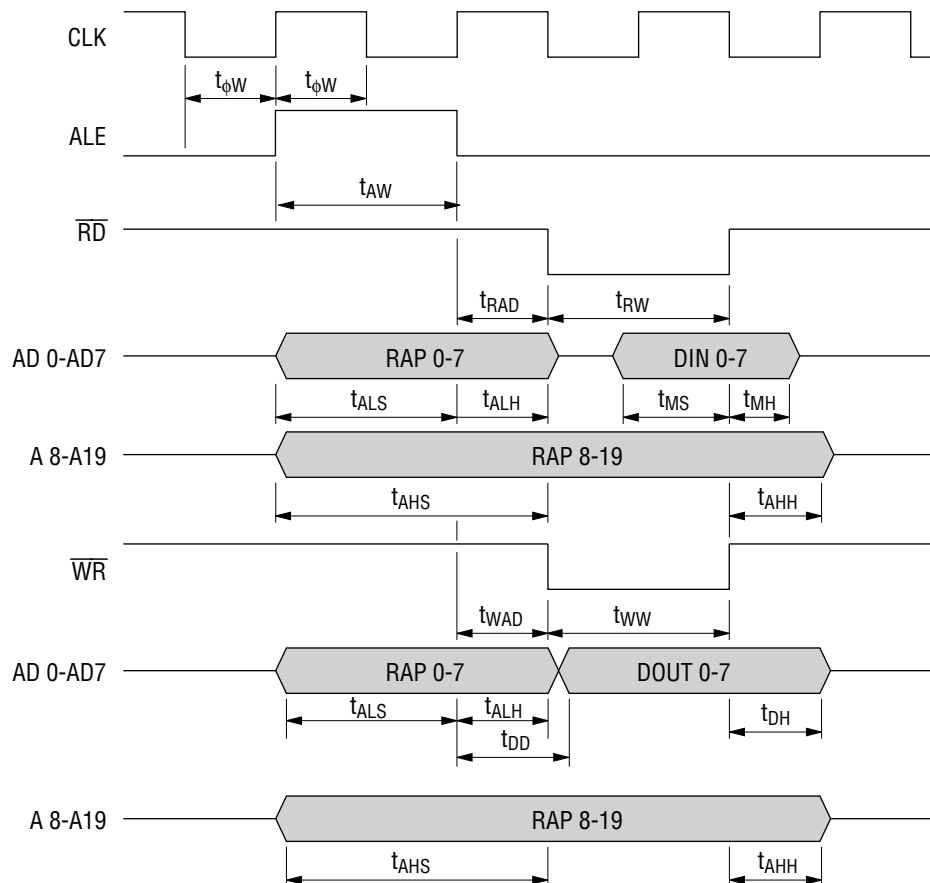
Parameter	Symbol	Conditions	Min	Max	Units
Clock (OSC) pulse width	t _{φW}	—	25	—	ns
ALE pulse width	t _{AW}	C _L =50pF	2t _{φW} −2	—	
PSEN pulse width	t _{PW}		2t _{φW} −5	—	
PSEN pulse delay time	t _{PAD}		t _{φW} −3	t _{φW} +3	
Low address setup time	t _{ALS}		2t _{φW} −3	2t _{φW} +3	
Low address hold time	t _{ALH}		t _{φW} −3	t _{φW} +3	
High address setup time	t _{AHS}		4t _{φW} −3	4t _{φW} +3	
High address hold time	t _{APH}		0	t _{φW} +3	
Instruction setup time	t _{IS}		15	—	
Instruction hold time	t _{IH}		0	t _{φW} −3	



• External Data Memory Control

(Ta=-30 to +70°C)

Parameter	Symbol	Conditions	Min	Max	Units
Clock (OSC) pulse width	$t_{\phi W}$	—	25	—	
ALE pulse width	t_{AW}	$C_L=50pF$	$2t_{\phi W}-2$	—	ns
$\overline{RD}$ pulse width	t_{RW}		$2t_{\phi W}-5$	—	
$\overline{WR}$ pulse width	t_{WW}		$2t_{\phi W}-5$	—	
$\overline{RD}$ pulse delay time	t_{RAD}		$t_{\phi W}-3$	$t_{\phi W}+3$	
$\overline{WR}$ pulse delay time	t_{WAD}		$t_{\phi W}-3$	$t_{\phi W}+3$	
Low address setup time	t_{ALS}		$2t_{\phi W}-3$	$2t_{\phi W}+3$	
Low address hold time	t_{ALH}		$t_{\phi W}-3$	$t_{\phi W}+3$	
High address setup time	t_{AHS}		$3t_{\phi W}-3$	$3t_{\phi W}+3$	
High address hold time	t_{AHH}		$t_{\phi W}-3$	$t_{\phi W}+3$	
Memory data setup time	t_{MS}		15	—	
Memory data hold time	t_{MH}		0	$t_{\phi W}-3$	
Data delay time	t_{DD}		$t_{ALH}-0$	$t_{ALH}+5$	
Data hold time	t_{DH}		$t_{\phi W}-3$	$t_{\phi W}+3$	

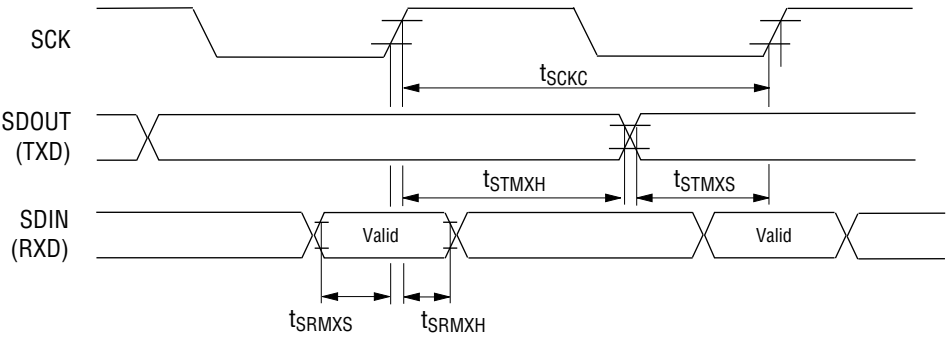


• Serial Port Contorl

Master mode

(Ta=−30 to +70°C)

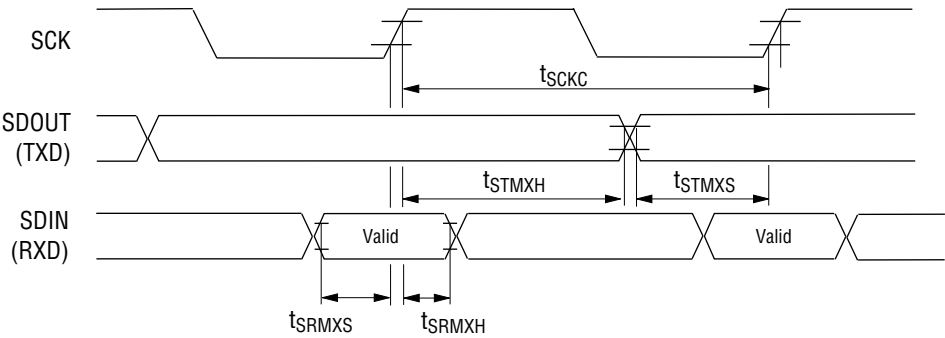
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Clock (OSC) pulse width	$t_{\phi W}$	—	25	—	—	ns
Serial clock cycle time	t_{SCKC}	$C_L=50pF$	$8t_{\phi W}$	—	—	
Output data setup time	t_{STMXS}		$4t_{\phi W}-5$	—	—	
Output data hold time	t_{STMXH}		$3t_{\phi W}-10$	—	—	
Input data setup time	t_{SRMXS}		20	—	—	
Input data hold time	t_{SRMXH}		0	—	—	



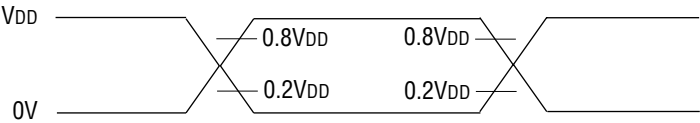
Slave mode

(Ta=-30 to +70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Clock (OSC) pulse width	$t_{\phi W}$	—	25	—	—	ns
Serial clock cycle time	t_{SCKC}	$C_L=50pF$	$8t_{\phi W}$	—	—	
Output data setup time	t_{STMXS}		$2t_{\phi W}-15$	—	—	
Output data hold time	t_{STMXH}		$4t_{\phi W}-10$	—	—	
Input data setup time	t_{SRMXS}		20	—	—	
Input data hold time	t_{SRMXH}		0	—	—	



AC timing mesurement point

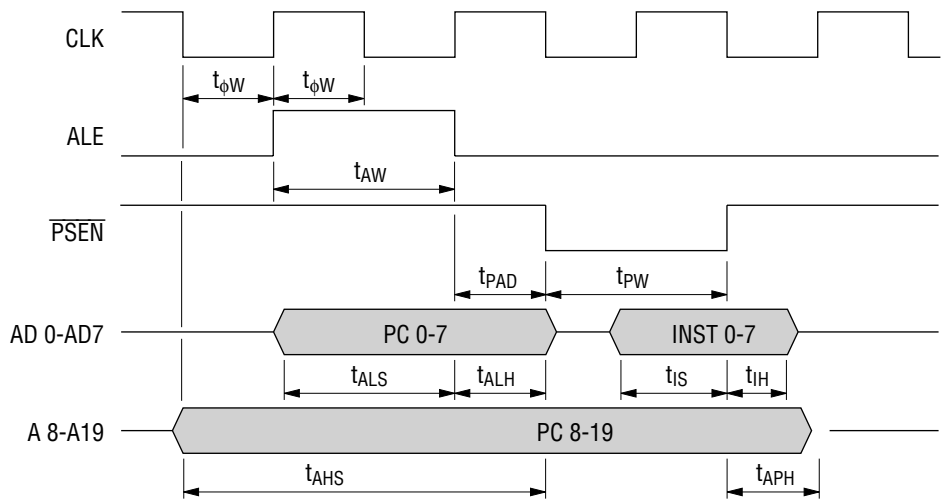


AC Characteristics (2.7V ≤ V_{DD} ≤ 5.5V)

- External Program Memory Control

(Ta= -30 to +70°C)

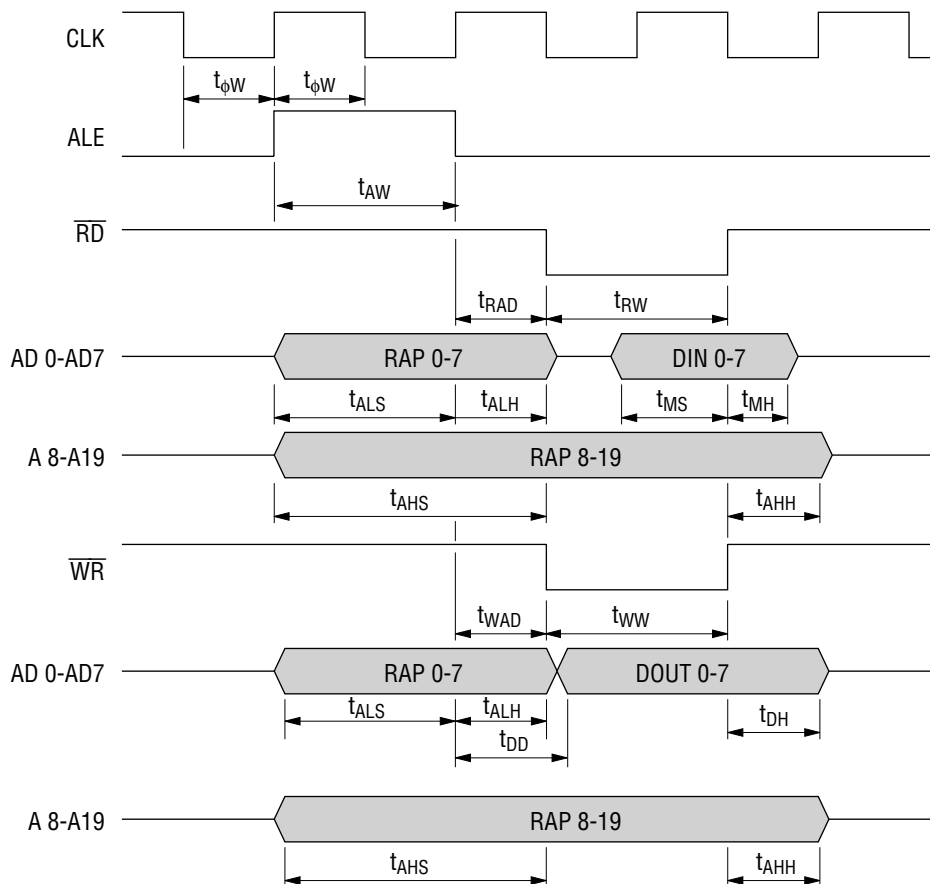
Parameter	Symbol	Conditions	Min	Max	Units
Clock (OSC) pulse width	t _{φW}	—	50	—	ns
ALE pulse width	t _{AW}	C _L =50pF	2t _{φW} -4	—	
PSEN pulse width	t _{PW}		2t _{φW} -10	—	
PSEN pulse delay time	t _{PAD}		t _{φW} -6	t _{φW} +6	
Low address setup time	t _{ALS}		2t _{φW} -6	2t _{φW} +6	
Low address hold time	t _{ALH}		t _{φW} -6	t _{φW} +6	
High address setup time	t _{AHS}		4t _{φW} -6	4t _{φW} +6	
High address hold time	t _{APH}		0	t _{φW} +6	
Instruction setup time	t _{IS}		30	—	
Instruction hold time	t _{IH}		0	t _{φW} -6	



• External Data Memory Control

(Ta= -30 to +70°C)

Parameter	Symbol	Conditions	Min	Max	Units
Clock (OSC) pulse width	$t_{\phi W}$	—	50	—	
ALE pulse width	t_{AW}	$C_L=50\text{pF}$	$2t_{\phi W}-4$	—	ns
$\overline{\text{RD}}$ pulse width	t_{RW}		$2t_{\phi W}-10$	—	
$\overline{\text{WR}}$ pulse width	t_{WW}		$2t_{\phi W}-10$	—	
$\overline{\text{RD}}$ pulse delay time	t_{RAD}		$t_{\phi W}-6$	$t_{\phi W}+6$	
$\overline{\text{WR}}$ pulse delay time	t_{WAD}		$t_{\phi W}-6$	$t_{\phi W}+6$	
Low address setup time	t_{ALS}		$2t_{\phi W}-6$	$2t_{\phi W}+6$	
Low address hold time	t_{ALH}		$t_{\phi W}-6$	$t_{\phi W}+6$	
High address setup time	t_{AHS}		$3t_{\phi W}-6$	$3t_{\phi W}+6$	
High address hold time	t_{AHH}		$t_{\phi W}-6$	$t_{\phi W}+6$	
Memory data setup time	t_{MS}		30	—	
Memory data hold time	t_{MH}		0	$t_{\phi W}-6$	
Data delay time	t_{DD}		$t_{ALH}-0$	$t_{ALH}+10$	
Data hold time	t_{DH}		$t_{\phi W}-6$	$t_{\phi W}+6$	

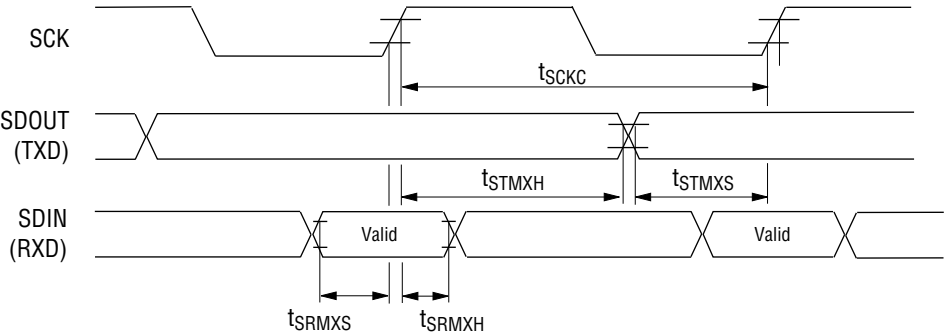


• Serial Port Control

Master mode

(Ta=-30 to +70°C)

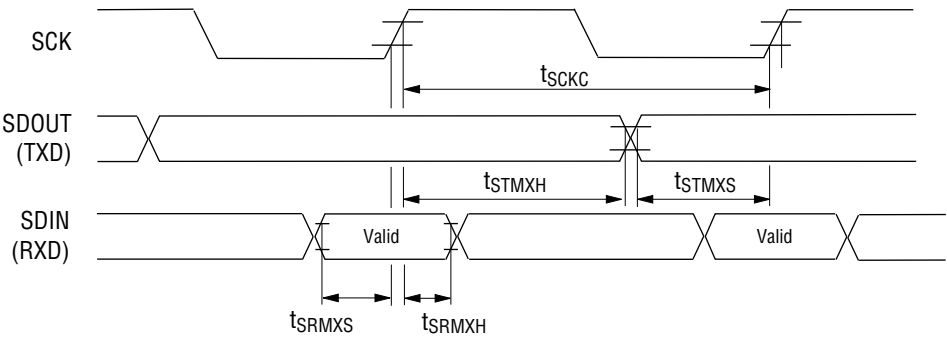
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Clock (OSC) pulse width	$t_{\phi W}$	—	50	—	—	ns
Serial clock cycle time	t_{SCKC}	$C_L=50\text{pF}$	$8t_{\phi W}$	—	—	
Output data setup time	t_{STMXS}		$4t_{\phi W}-10$	—	—	
Output data hold time	t_{STMXH}		$3t_{\phi W}-20$	—	—	
Input data setup time	t_{SRMXS}		30	—	—	
Input data hold time	t_{SRMXH}		0	—	—	



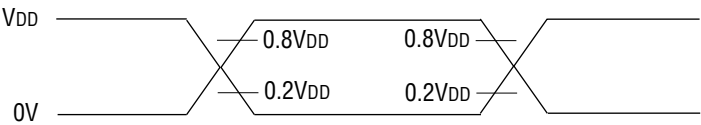
Slave mode

(Ta= -30 to +70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Clock (OSC) pulse width	$t_{\phi W}$	—	50	—	—	ns
Serial clock cycle time	t_{SCKC}	$C_L=50pF$	$8t_{\phi W}$	—	—	
Output data setup time	t_{STMXS}		$2t_{\phi W}-30$	—	—	
Output data hold time	t_{STMXH}		$4t_{\phi W}-20$	—	—	
Input data setup time	t_{SRMXS}		30	—	—	
Input data hold time	t_{SRMXH}		10	—	—	



AC timing measurement point

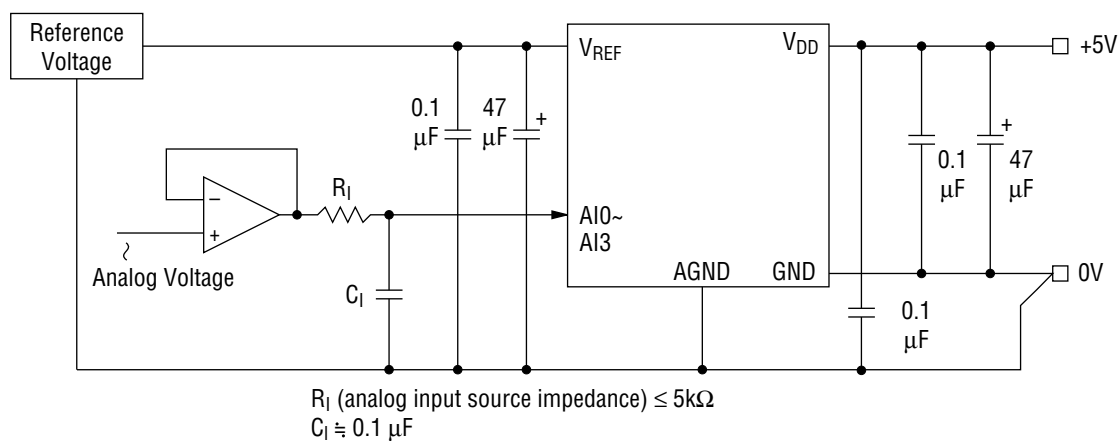


A/D Converter Characteristics(Ta=-30 to +70°C, V_{DD}=V_{REF}=5V±10%, AGND=GND=0V, f_{OSC}=20MHz)

Item	Symbol	Conditions	Min	Typ	Max	Units
Resolution	n	Refer to the recommended circuit Analog input source impedance R _I ≤5kΩ t _{CONV} =19.2μsec by ADTM set data	—	8	—	Bit
Linearity error	E _L		—	—	±2	LSB
Differential linearity error	E _D		—	—	±1	
Zero scale error	E _{ZS}		—	—	+2	
Full scale error	E _{FS}		—	—	-2	
Conversion time	t _{CONV}		6.4	—	19.2	μs/CH

A/D Converter Characteristics(Ta=-30 to +70°C, V_{DD}=V_{REF}=3V±10%, AGND=GND=0V, f_{OSC}=10MHz)

Item	Symbol	Conditions	Min	Typ	Max	Units
Resolution	n	Refer to the recommended circuit Analog input source impedance R _I ≤5kΩ t _{CONV} =38.4μsec ADTM=00b (384CLK selection)	—	8	—	Bit
Linearity error	E _L		—	—	±1	LSB
Differential linearity error	E _D		—	—	±0.5	
Zero scale error	E _{ZS}		—	—	+1	
Full scale error	E _{FS}		—	—	-1	
Conversion time	t _{CONV}		—	38.4	—	μs/CH

**Recommended Circuit**

Definition of terms

- Resolution

Resolution is the minimum input analog value that can be resolved. With 8 bits, $2^8=256$ so resolution can be to $(V_{REF}-AGND) \div 256$.

- Linearity error

Linearity error is the difference between actual conversion characteristics and ideal conversion characteristics of an 8-bit A/D converter (so this does not include quantization error).

Ideal conversion characteristics would be to divide the voltage between V_{REF} and AGND into 256 equal steps.

- Differential linearity error

Differential linearity error indicates slope of conversion characteristics. The change in analog input voltage value that would change the digital output by one bit is ideally 1 LSB = $(V_{REF}-AGND) \div 256$, so differential linearity error is the difference between this ideal bit size and the actual bit size anywhere in the conversion range.

- Zero scale error

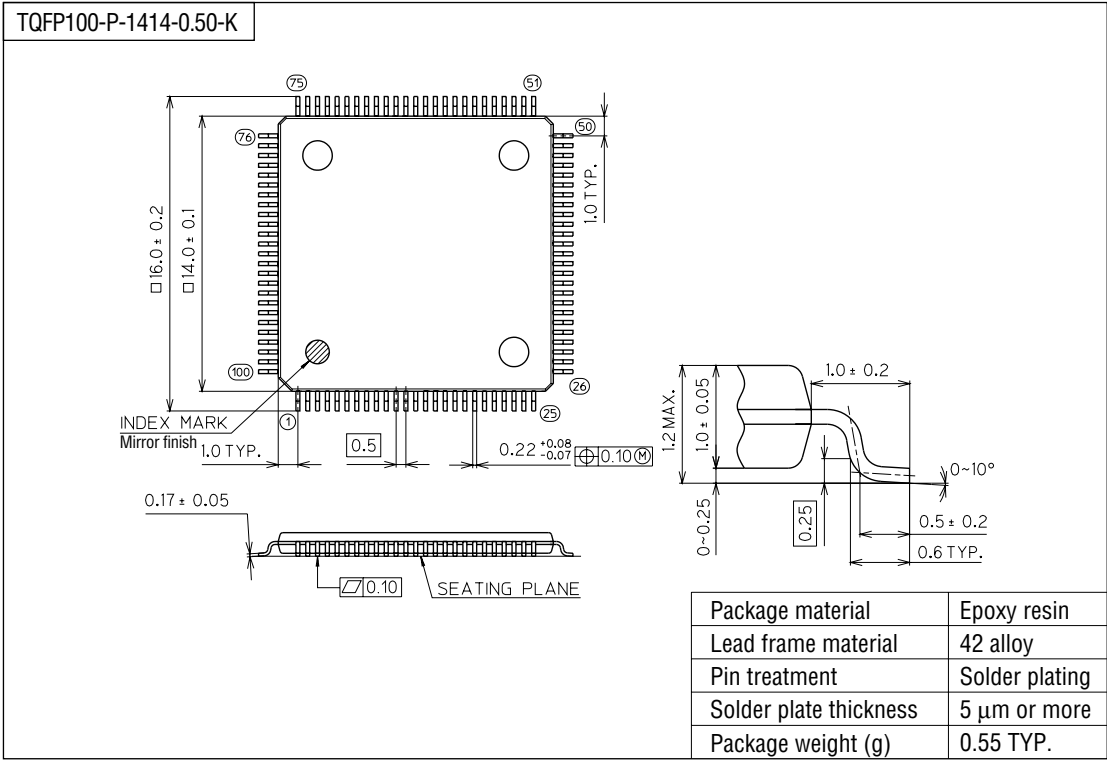
Zero scale error is the difference between actual conversion characteristics and ideal conversion characteristics at the point where digital output switches from 00H to 01H.

- Full scale error

Full scale error is the difference between actual conversion characteristics and ideal conversion characteristics at the point where digital output switches from FEH to FFH.

PACKAGE DIMENSIONS

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).