MCM36232

2 x 32K x 36 Bit Static Random Access Memory Module

The MCM36232 is a 2.35M bit static random access memory module organized as two banks of 32,768 words of 36 bits. The module is a 76-lead zig-zag in-line memory module (ZIP) consisting of eight MCM6205C fast static RAMs packaged in 32 J-lead small outline packages (SOJ) and mounted on a printed circuit board along with eight decoupling capacitors.

The MCM6205C is a high-performance CMOS fast static RAM organized as 32,768 words of 9 bits, fabricated using high-performance silicon-gate CMOS technology. Static design eliminates the need for external clocks or timing strobes, while CMOS circuitry reduces power consumption and provides for greater reliability.

The MCM36232 is equipped with four separate byte write enable ($\overline{W1}$ – $\overline{W4}$) inputs, two separate bank enable ($\overline{E1}$ – $\overline{E2}$) inputs and two separate bank output enable ($\overline{G1}$ – $\overline{G2}$) inputs allowing for greater system flexibility. The $\overline{Gx}$ input, when high, will force the outputs of bank x to high impedance.

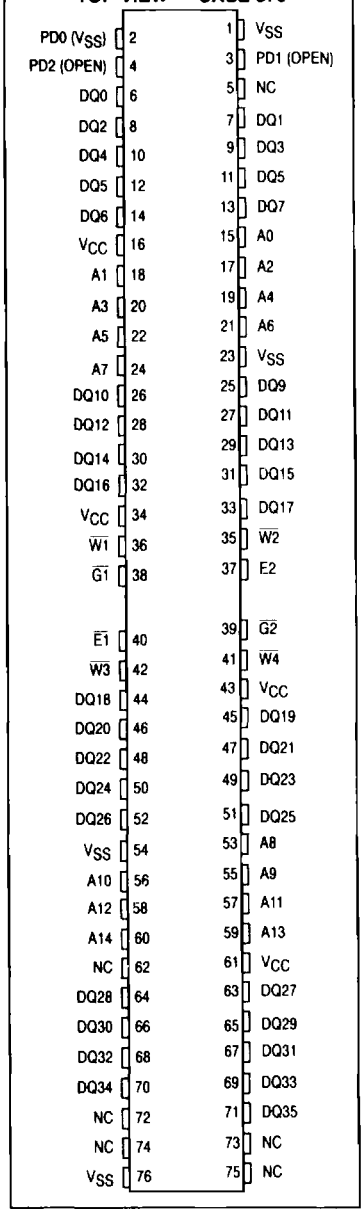
PD0 through PD2 are reserved for density identification. PD0 is connected to ground and PD1 and PD2 are not connected (open). These pins can be used to identify the density of the memory module compared with future versions.

- Single 5 V ± 10% Power Supply
- Fast Access Time: 15/20 ns
- Three-State Outputs
- Fully TTL Compatible
- Power Operation: 880/800 mA Maximum, Active AC
- High Board Density ZIP Package
- Byte Operation: Four Separate Write Enables, One for Each Byte (Nine Bits)
- High Quality Four-Layer FR4 PWB with Separate Internal Power and Ground Planes
- Incorporates Motorola's State-of-the-Art Fast Static RAMs

PIN NAMES	
A0 – A14	Address Inputs
DQ0 – DQ35	Data Inputs/Outputs
$\overline{E1}$ – $\overline{E2}$	Byte Enables
$\overline{W1}$ – $\overline{W4}$	Byte Write Enables
$\overline{G1}$ – $\overline{G2}$	Bank Output Enables
PD0 – PD2	Package Density Identifiers
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground

For proper operation of the device, V_{SS} must be connected to ground.

PIN ASSIGNMENT
76 LEAD ZIG-ZAG IN-LINE PACKAGE
TOP VIEW — CASE 879



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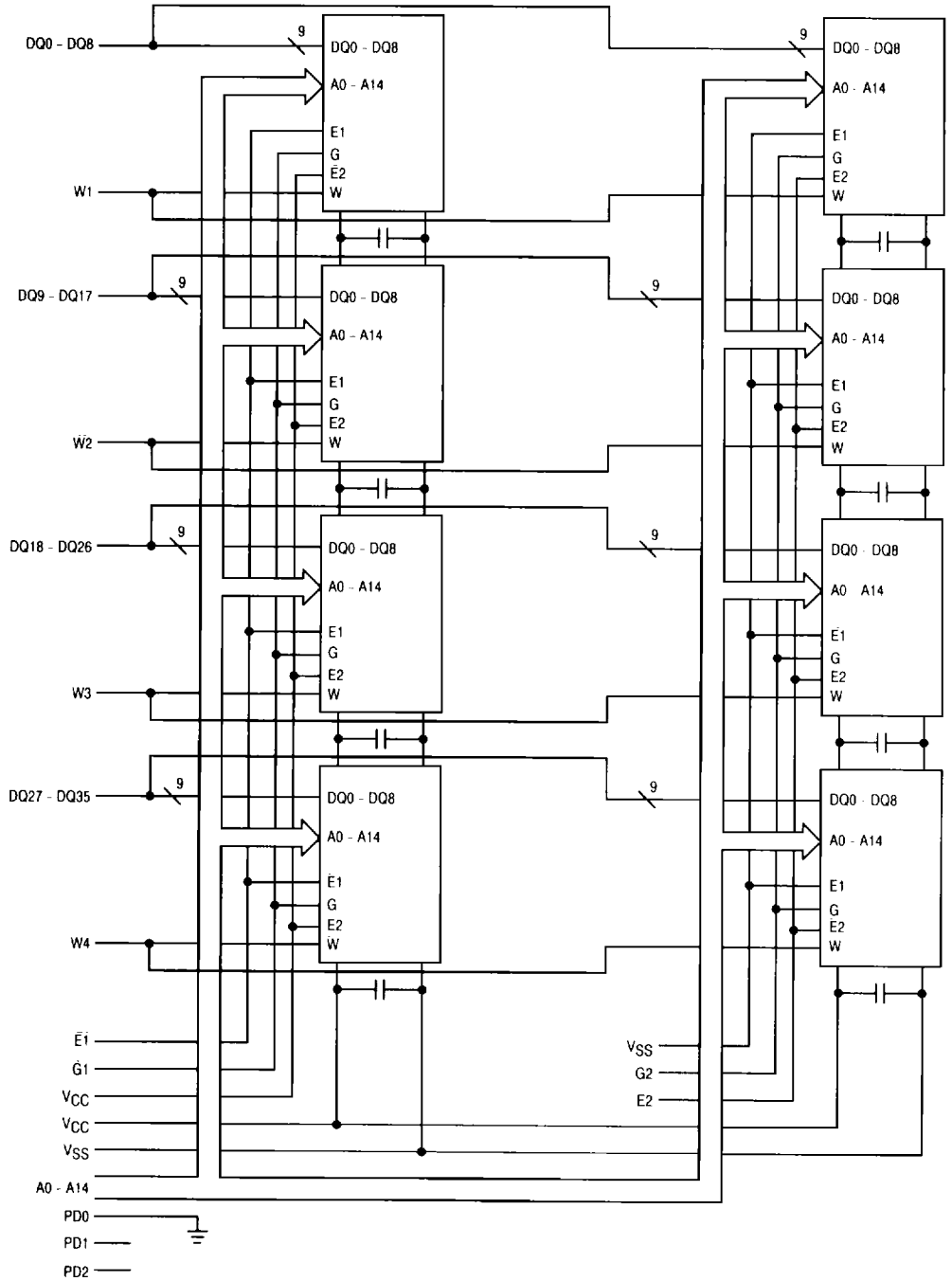
FUNCTIONAL BLOCK DIAGRAM



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TRUTH TABLE (X = Don't Care)

E1	E2	G1	G2	Wx	Mode	V_{CC} Current	Output	Cycle
H	L	X	X	X	Not Selected	I_{SB1} or I_{SB2}	High-Z	—
L	L	H	X	H	Read Bank 1	I_{CCA}, I_{SB1}	High-Z	—
L	L	L	X	H	Read Bank 1	I_{CCA}, I_{SB1}	D_{out}	Read Cycle
L	L	X	X	L	Write Bank 1	I_{CCA}, I_{SB1}	D_{in}	Write Cycle
H	H	X	H	H	Read Bank 2	I_{SB1}, I_{CCA}	High-Z	—
H	H	X	L	H	Read Bank 2	I_{SB1}, I_{CCA}	D_{out}	Read Cycle
H	H	X	X	L	Write Bank 2	I_{SB1}, I_{CCA}	D_{in}	Write Cycle

ABSOLUTE MAXIMUM RATINGS (Voltages referenced to V_{SS} = 0 V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	V
Output Power Supply Voltage	V_{CCQ}	– 0.5 to V_{CC}	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current (per I/O)	I_{out}	+ 30	mA
Power Dissipation (T_A = 70°C, V_{CC} = 5 V)	P_D	5	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature	T_{stg}	– 25 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

The devices on this module contain circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high impedance circuits.

These CMOS memory circuits have been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The module is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages referenced to V_{SS} = 0 V)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	3.0	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	0.0	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2 V ac (pulse width < 20 ns)
**V_{IL} (min) = – 3.0 V ac (pulse width < 20 ns)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	—	± 8	µA
Output Leakage Current (G, Ex = V_{IH}, V_{out} = 0 to V_{CCQ})	$I_{lkg(O)}$	—	—	± 8	µA
AC Active Supply Current (G, Ex = V_{IL}, I_{out} = 0 mA, Cycle Time ≥ t_{AVAV} min, Only One Bank is Enabled) MCM36232-15: t_{AVAV} = 15 ns	I_{CCA15}	—	—	880	mA
MCM36232-20: t_{AVAV} = 20 ns	I_{CCA20}	—	—	800	
AC Standby Current (E1 = V_{IH}, E2 = V_{IL}, Cycle Time > t_{AVAV} min) MCM36232-15: t_{AVAV} = 15 ns	I_{SB1}		300	400	mA
MCM36232-20: t_{AVAV} = 20 ns		—	260	360	
CMOS Standby Current (Ex ≥ V_{CC} – 0.2 V, All Inputs ≥ V_{CC} – 0.2 V or ≤ 0.2 V)	I_{SB2}	—	100	160	mA
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	—	0.4	V
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	—	V

NOTE: Good decoupling of the local power supply should always be used.

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Typ	Max	Unit
Input Capacitance	Address	C_{in}	32	48	pF
	W1 – W4		14	16	
	E1, $\overline{E2}$, $\overline{G1}$, $\overline{G2}$		24	32	
Input/Output Capacitance (DQ0 – DQ35)		$C_{I/O}$	14	16	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to + 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 3 ns
Output Timing Reference Level ..... 1.5 V
Output Load ..... See Figure 1A Unless Otherwise Noted

READ CYCLE TIMING (See Notes 1 and 2)

Parameter	Symbol		MCM36232-15		MCM36232-20		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	15	—	20	—	ns	3
Address Access Time	t_{AVQV}	t_{AA}	—	15	—	20	ns	
Enable Access Time	t_{ELQV}	t_{ACS}	—	15	—	20	ns	
Output Enable Access Time	t_{GLQV}	t_{OE}	—	8	—	10	ns	
Output Hold from Address Change	t_{AXQX}	t_{OH}	4	—	5	—	ns	
Enable Low to Output Active	t_{ELQX}	t_{CLZ}	4	—	5	—	ns	4, 5, 6
Output Enable to Output Active	t_{GLQX}	t_{OLZ}	0	—	0	—	ns	4, 5, 6
Enable High to Output High-Z	t_{EHQZ}	t_{CHZ}	0	8	0	9	ns	4, 5, 6
Output Enable High to Output High-Z	t_{GHQZ}	t_{OHZ}	0	7	0	8	ns	4, 5, 6
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	ns	
Power Down Time	t_{EHICCL}	t_{PD}	—	15	—	20	ns	

NOTES:
1. W is high for read cycle.
2. $\overline{E}1$ – $\overline{E2}$ are represented by $\overline{E}$ in these timing specifications; only one of the $\overline{E}$xs may be asserted.
3. All read cycle timing is referenced from the last valid address to the first transitioning address.
4. At any given voltage and temperature, t_{EHQZ} max is less than t_{ELQX} min, and t_{GHQZ} max is less than t_{GHQX} min, both for a given device and from device to device.
5. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
6. This parameter is sampled and not 100% tested.
7. Device is continuously selected ($\overline{E}$ = V_{IL}, G = V_{IL}).

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AC TEST LOADS

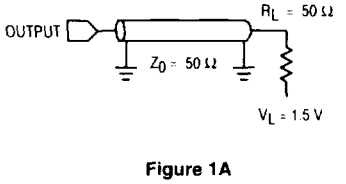


Figure 1A

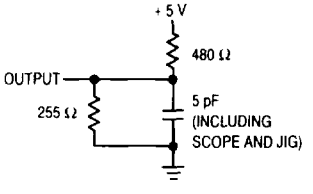
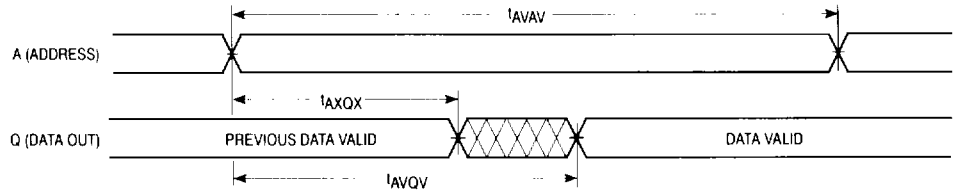


Figure 1B

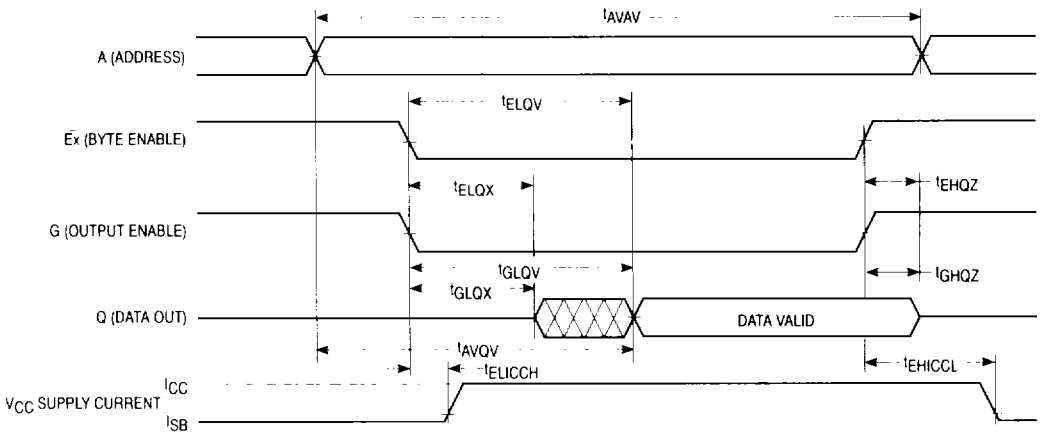
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 7)



READ CYCLE 2 (See Note)



NOTE: Addresses valid prior to or coincident with E going low.

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WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1 and 2)

Parameter	Symbol		MCM36232-15		MCM36232-20		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	20	—	ns	3
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	t_{AW}	12	—	15	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	t_{WP}	12	—	15	—	ns	
Write Pulse Width, G High	t_{WLWH}, t_{WLEH}	t_{WP}	10	—	12	—	ns	
Data Valid to End of Write	t_{DVWH}	t_{DW}	7	—	8	—	ns	
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	ns	
Write Low to Data High-Z	t_{WLQZ}	t_{WZ}	0	7	0	8	ns	4, 5, 6
Write High to Output Active	t_{WHQX}	t_{OW}	4	—	4	—	ns	4, 5, 6
Write Recovery Time	t_{WHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ – $\overline{E2}$ are presented by $\overline{E}$ in these timing specifications; any combination of Exs may be asserted. $\overline{G}$ is a don't care when W is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
5. This parameter is sampled and not 100% tested.
6. At any given voltage and temperature, t_{WLQZ} max is less than t_{WHQX} min both for a given device and from device to device.

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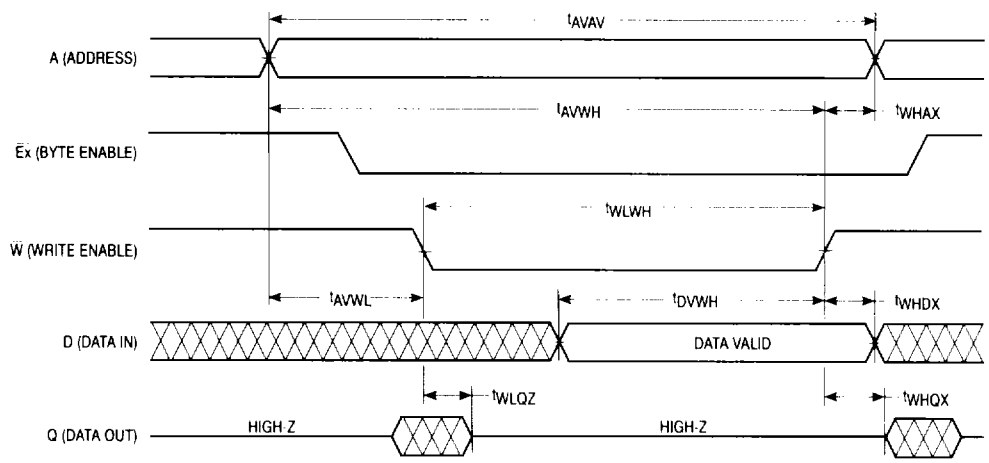
WRITE CYCLE 1

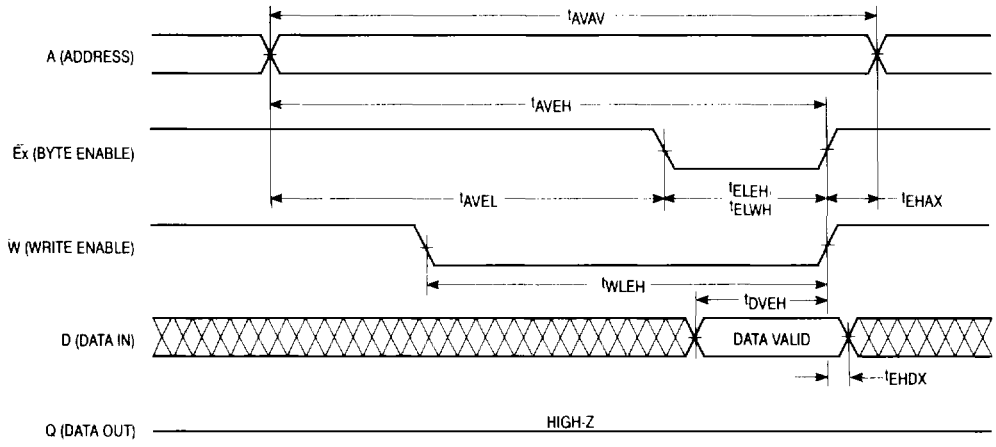


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1 and 2)

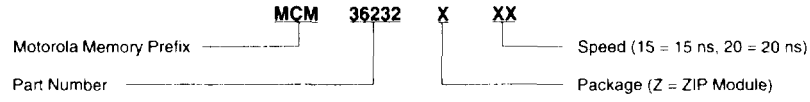
Parameter	Symbol		MCM36232-15		MCM36232-20		Unit	Notes
	Standard	Alternate	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	15	—	20	—	ns	3
Address Setup Time	t_{AVEL}	t_{AS}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	t_{AW}	12	—	15	—	ns	
Enable to End of Write	t_{ELEH} t_{ELWH}	t_{CW}	10	—	12	—	ns	2, 4, 5
Enable Valid to End of Write	t_{DVEH}	t_{DW}	7	—	8	—	ns	
Data Hold Time	t_{EHDX}	t_{DH}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	t_{WR}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. $\overline{E1}$ and $\overline{E2}$ are represented by $\overline{E}$ in these timing specifications; any combination of $\overline{E}$xs may be asserted. $\overline{G}$ is a don't care when $\overline{W}$ is low.
3. All write cycle timing is referenced from the last valid address to the first transitioning address.
4. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
5. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high-impedence condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM36232Z15 MCM36232Z20