Preliminary Data Sheet

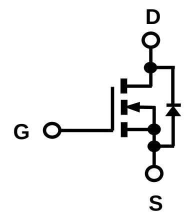
ICE8N70FP

ICE8N70FP N-Channel Enhancement Mode MOSFET

Product Summary			
I_D	T_A=25°C	8A	Max
$V_{(BR)DSS}$	I_D=250uA	700V	Min
$r_{DS(on)}$	V_{GS}=10V	0.38Ω	Typ
Q_g	V_{DS}=480V	41nC	Typ

Features

- Low $r_{DS(on)}$
- Ultra Low Gate Charge
- High d*v*/d*t* capability
- High Unclamped Inductive Switching (UIS) capability
- High peak current capability
- Increased transconductance performance
- Optimized design for high performance power systems



T0220 Full-PAK

Isolated (T0-220)

1=Gate, 2=Drain, 3=Source

ICEMOS AND ITS SISTER COMPANY 3D SEMI OWN THE FUNDAMENTAL PATENTS FOR SUPERJUNCTION MOSFETS. THE MAJORITY OF THESE PATENTS HAVE 17 to 20 YEARS OF REMAINING LIFE. THIS PORTFOLIO HAS GRANTED PATENTS ISSUED IN USA, CHINA, KOREA, JAPAN, TAIWAN & EUROPE.

Maximum ratings [b], at T_j=25°C, unless otherwise specified

Parameter	*Symbol*	*Conditions*	*Value*	*Unit*
Continuous drain current	I_D	T_c=25°C	8	A
Pulsed drain current	$I_{D,\ pulse}$	T_c=25°C	24	A
Avalanche energy, single pulse	E_{AS}	I_D=4A	340	mJ
Avalanche current, repetitive	I_{AR}	limited by $T_j$max	4	A
MOSFET d*v*/d*t* ruggedness	d*v*/d*t*	V_{DS}=480V, I_D=8A, T_j=125°C	50	V/ns
Gate source voltage	V_{GS}	Static	±20	V
		AC (*f*>1Hz)	±30	
Power dissipation	P_{tot}	T_c=25°C	35	W
Operating and storage temperature	T_j, T_{stg}		-55 to +150	°C
Mounting torque		M 2.5 screws	50	Ncm

a When mounted on 1inch square 2oz copper clad FR-4

b Preliminary Data Sheet – Specifications subject to change

Parameter	Symbol	Conditions	Values Min	Values Typ	Values Max	Unit

Thermal characteristics

Thermal resistance, junction-case [a]	R_{thJC}		-	-	3.5	°C/W
Thermal resistance, junction-ambient [a]	R_{thJA}	leaded	-	-	80	°C/W
Soldering temperature, wave soldering only allowed at leads	T_{sold}	1.6mm (0.063in.) from case for 10 s	-	-	260	°C

Electrical characteristics [b], at T_j=25°C, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=250µA	700	730	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250µA	2.1	3	3.9	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=700V, V_{GS}=0V, T_j=25°C	-	0.1	1	µA
		V_{DS}=700V, V_{GS}=0V, T_j=150°C	-	-	100	µA
Gate source leakage current	I_{GSS}	V_{GS}=±20 V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=4A, T_j=25°C	-	0.38	0.45	Ω
		V_{GS}=10V, I_D=4A, T_j=150°C	-	0.95	-	Ω
Gate resistance	R_G	f=1 MHZ, open drain	-	5	-	Ω

Dynamic characteristics

Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=25 V, f=1 MHz	-	1250	-	pF
Output capacitance	C_{oss}		-	600	-	pF
Reverse transfer capacitance	C_{rss}		-	5	-	pF
Transconductance	g_{fs}	V_{DS}>2*I_D*R_{DS}, I_D=4A	-	12	-	S
Turn-on delay time	$t_{d(on)}$	V_{DS}=480V, V_{GS}=10V, I_D=8A, R_G=4Ω (External)	-	6	-	ns
Rise time	t_r		-	3.5	-	ns
Turn-off delay time	$t_{d(off)}$		-	54	-	ns
Fall time	t_f		-	7	-	ns

Parameter	*Symbol*	*Conditions*	*Values*			*Unit*
			Min	*Typ*	*Max*	

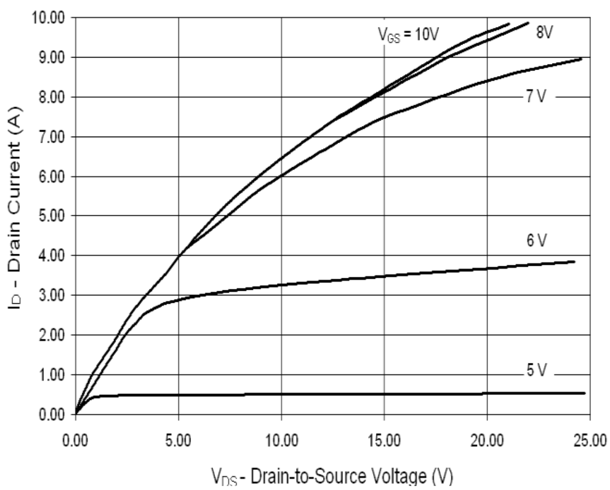
Gate charge characteristics

Gate to source charge	Q_{gs}	V_{DS}=480 V, I_D=8A, V_{GS}=0 to 10 V	-	7.1	-	nC
Gate to drain charge	Q_{gd}		-	14	-	
Gate charge total	Q_g		-	41	-	
Gate plateau voltage	$V_{plateau}$		-	5.2	-	V

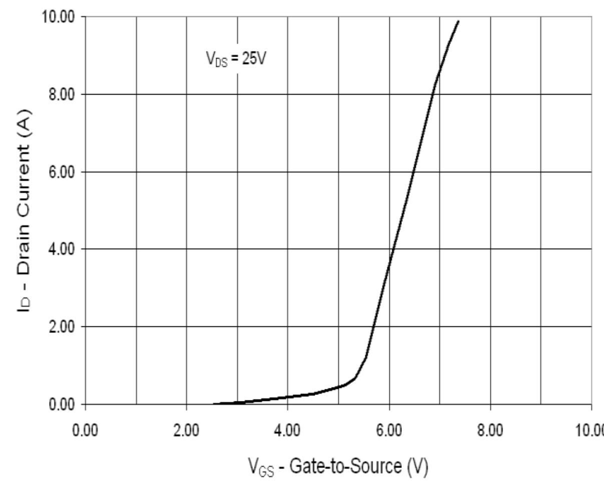
Reverse Diode

Diode forward voltage	V_{SD}	V_{GS}=0V, I_{S}=I_F	-	0.9	1.2	V
Reverse recovery time	t_{rr}	V_{RR}=480V, I_S=I_F, d_{iF}/d_t=100 A/µS	-	330	-	ns
Reverse recovery charge	Q_{rr}		-	4.4	-	µC
Peak reverse recovery current	I_{rm}		-	25	-	A

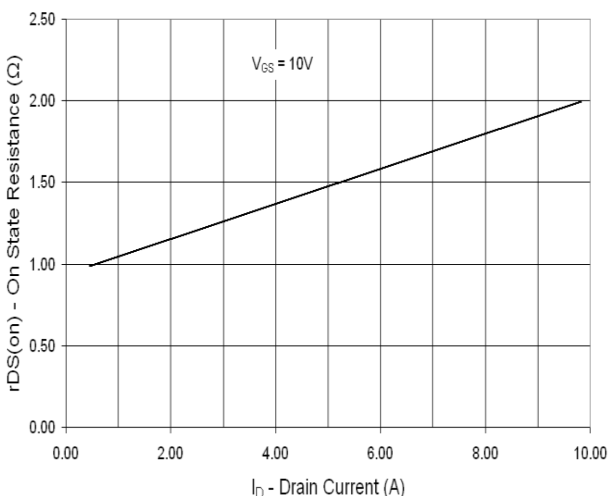
Output Characteristics



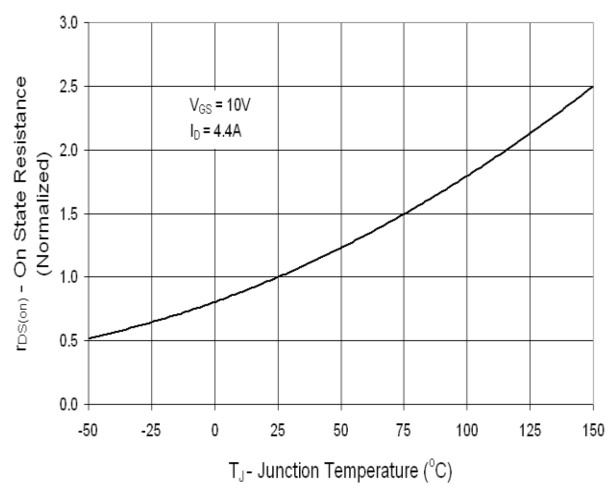
Transfer Characteristics



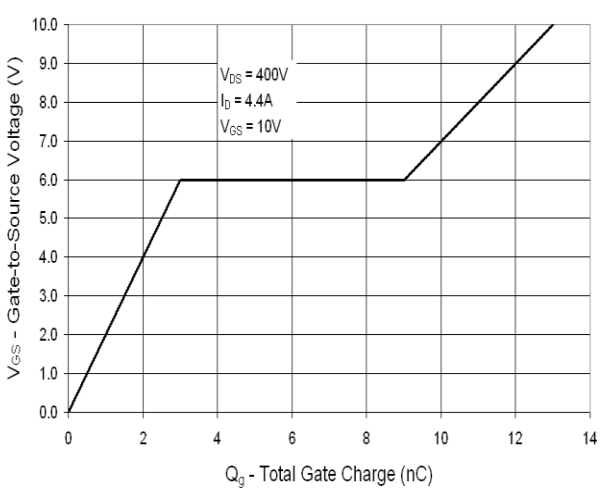
On State Resistance vs. Drain Current



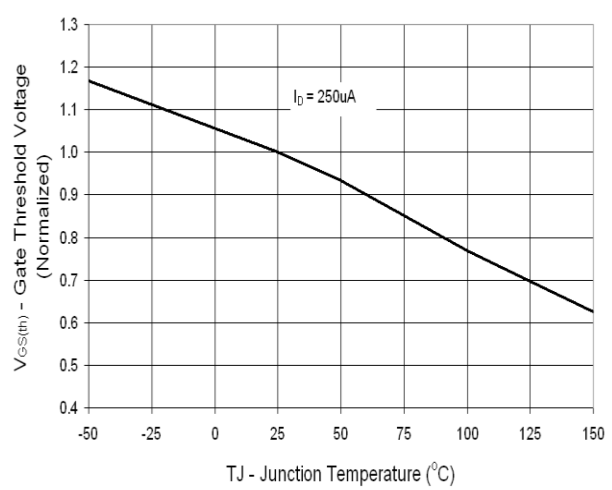
On State Resistance vs. Junction Temperature



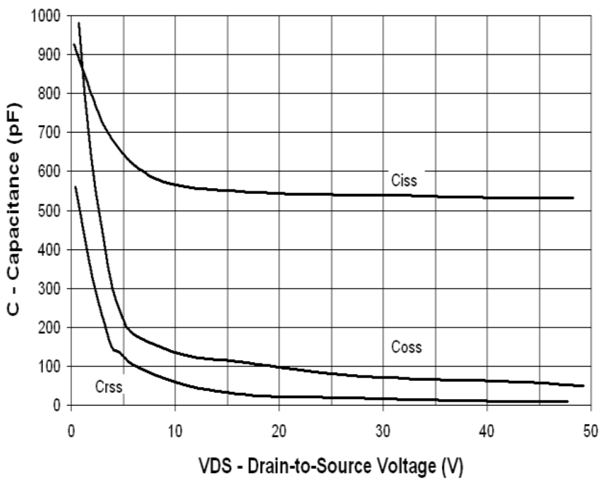
Gate Charge



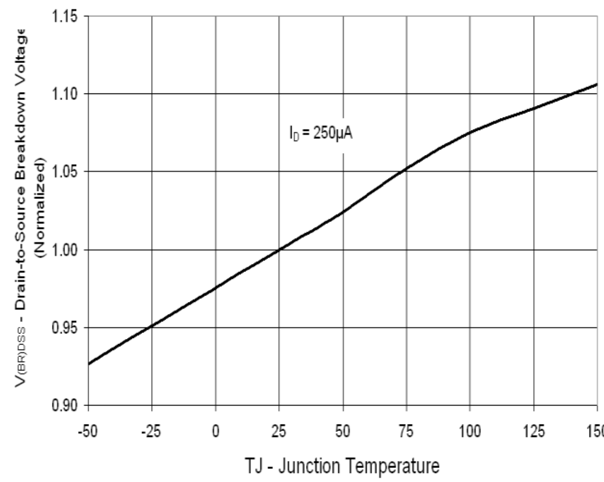
Gate Threshold Voltage vs. Junction Temperature



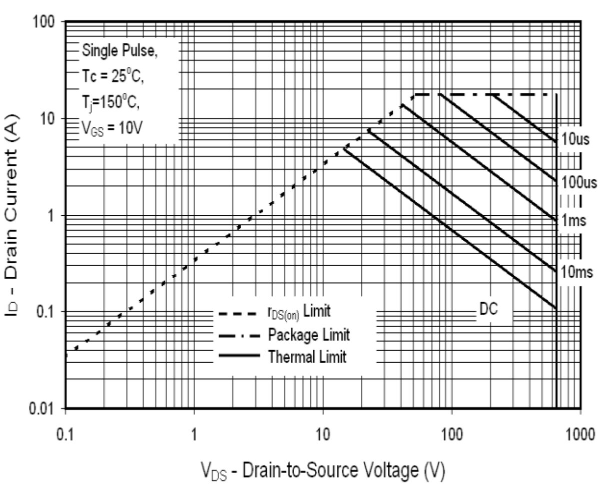
Capacitance



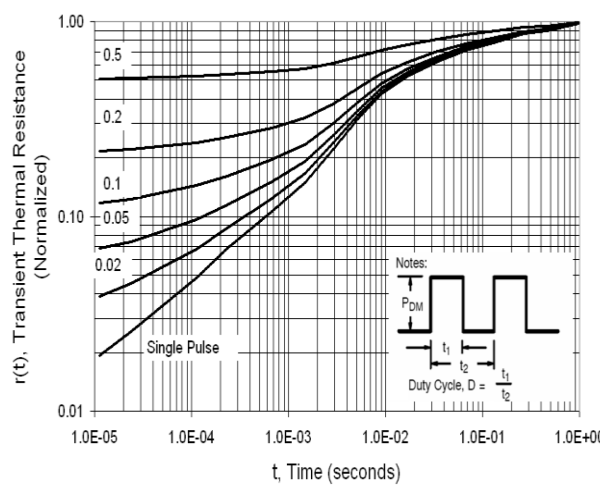
Drain-to-Source Breakdown Voltage vs. TJ

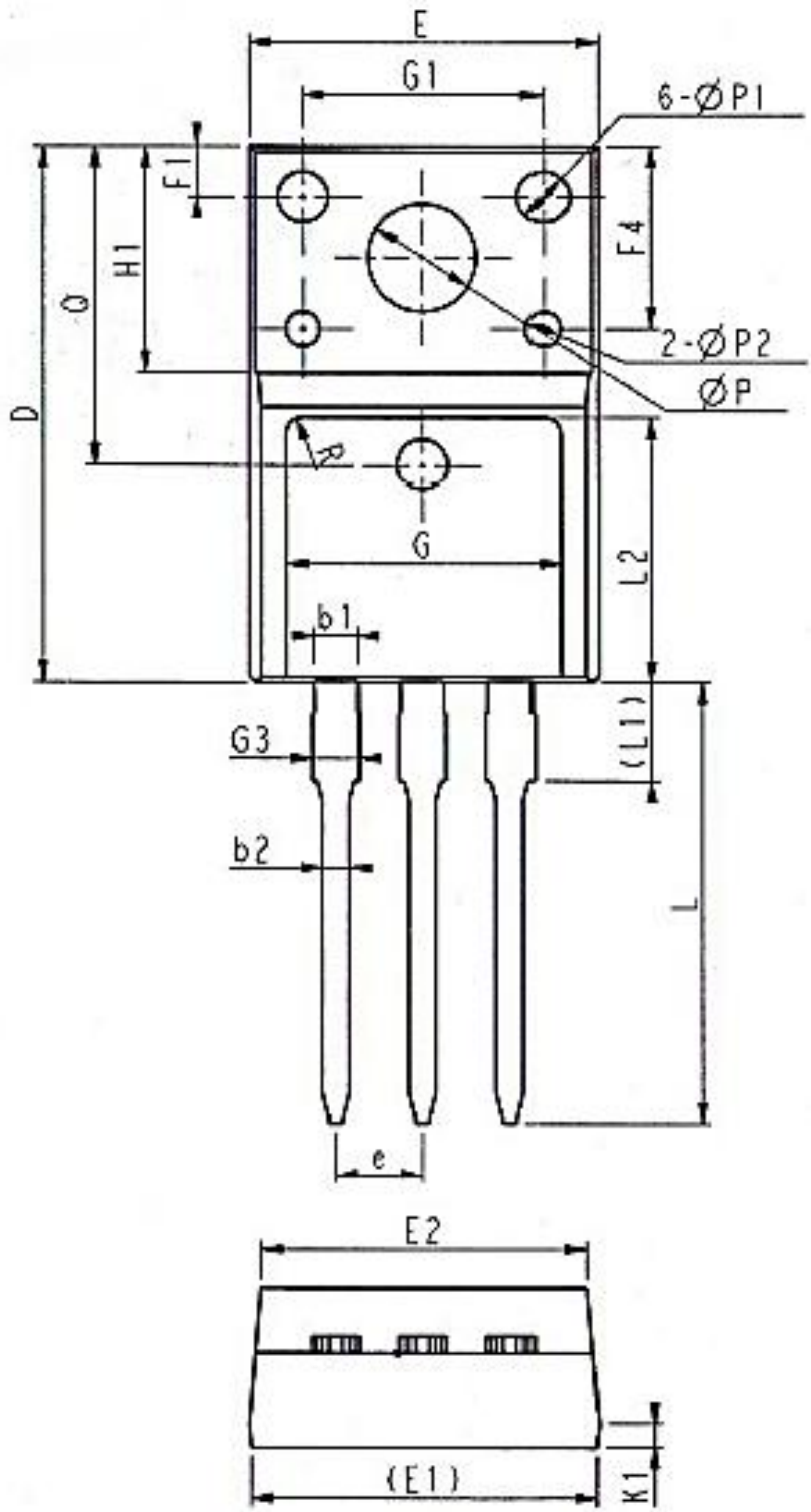


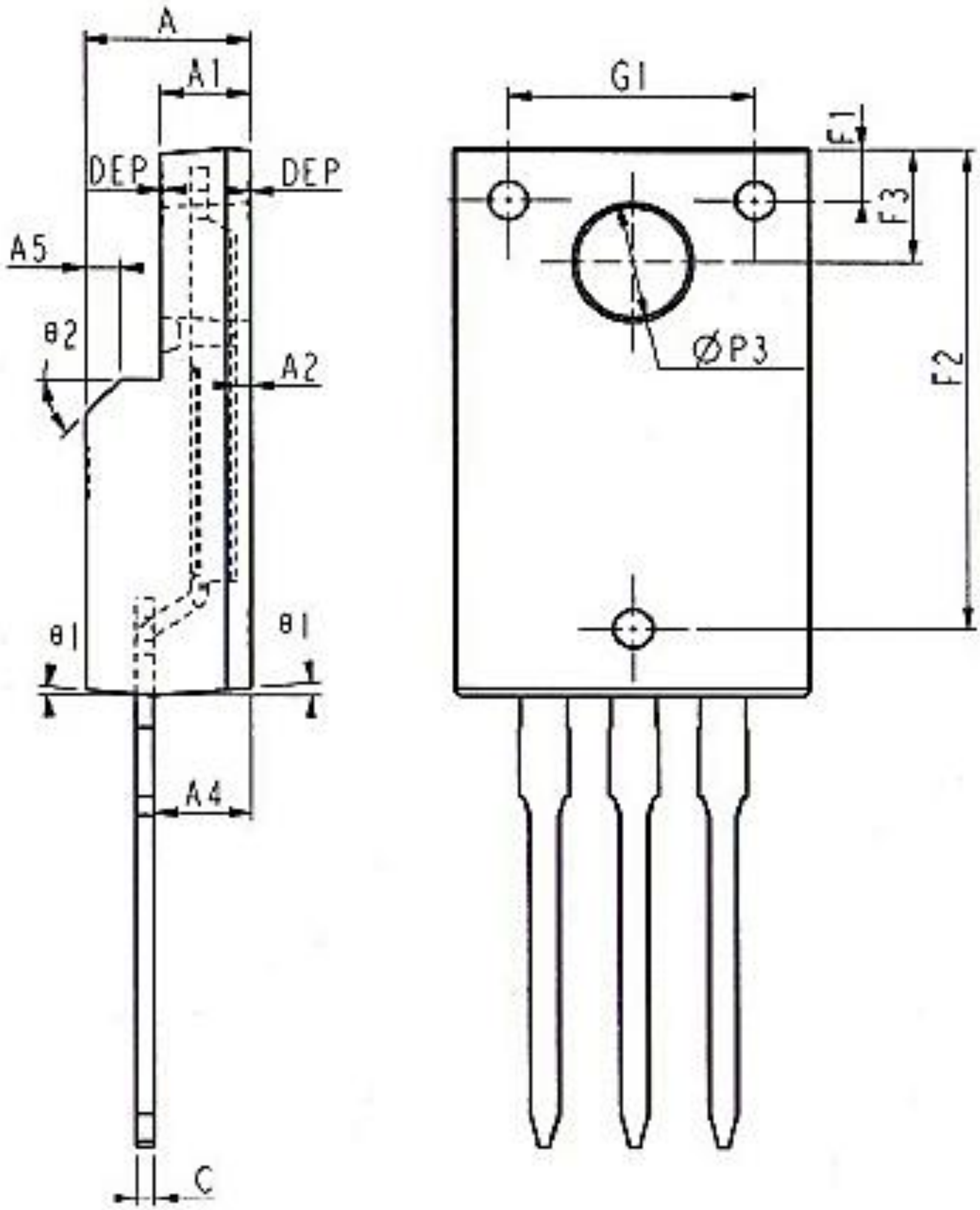
Maximum Rated Forward Biased Safe Operating Area



Transient Thermal Response, Junction-to-Case




E
G1
6-ØP1
F1
H1
Q
D
F4
2-ØP2
ØP
R
G
L2
b1
G3
(L1)
b2
L
e
E2
(E1)
K1


A
A1
DEP
DEP
A5
θ2
A2
θ1
θ1
A4
C
G1
F1
F3
ØP3
F2

COMMON DIMENSIONS

SYMBOL	MM		
	MIN	NOM	MAX
E	10.00	10.16	10.32
E1	9.94	10.04	10.14
E2	9.36	9.46	9.56
A	4.50	4.70	4.90
A1	2.34	2.54	2.74
A2	0.43	-	0.48
A4	2.66	2.76	2.86
A5		1.00REF	
c	0.45	0.50	0.60
D	15.67	15.87	16.07
Q		9.40REF	
H1		6.70REF	
e		2.54BSC	
ΦP		3.18REF	
L	12.78	12.98	13.18
L1	2.83	2.93	3.03
L2	7.70	7.80	7.90
ΦP1	1.40	1.50	1.60
ΦP2	1.15	1.20	1.25
ΦP3		3.45REF	
θ1	3°	5°	7°
θ2	-	45°	-
DEP	0.05	0.10	0.15
F1	1.00	1.50	2.00
F2	13.80	13.90	14.00
F3	3.20	3.30	3.40
F4	5.30	5.40	5.50
G	7.80	8.00	8.20
G1	6.90	7.00	7.10
G3	1.25	1.35	1.45
b1	1.23	1.28	1.38
b2	0.75	0.80	0.90
K1	0.65	0.70	0.75
R		0.50REF	

ICEMOS SUPERJUNCTION PATENT PORTFOLIO

ICEMOS GRANTED PATENTS

US7,429,772
US7,439,178
US7,446,018
US7,579,607
US7,723,172
US7,795,045
US7,846,821
US7,944,018
US8,012,806
US8,030,133

3D SEMI PATENTS LICENSED TO ICEMOS

US7,041,560B2
US7,023,069B2
US7,364,994
US7,227,197B2
US7,304,944B2
US7,052,982B2
US7,339,252
US7,410,891
US7,439,583
US7,227,197B2
US6,635,906
US6,936,867
US7,015,104
US9,109,110
US7,271,067
US7,354,818
US7,052,982,
US7,199,006B2

Note: additional patents in China, Korea, Japan, Taiwan, Europe have also been granted to IceMOS and 3D Semi for Superjunction MOSFETs with 70 additional Patent applications in process in the USA and the above listed countries.