# HYUNDAI

# HY5117404A Series

## 4M x 4-bit CMOS DRAM with Extended Data Out

## DESCRIPTION

The HY5117404A is the new generation and fast dynamic RAM organized 4,194,304 x 4-bit. The HY5117404A utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY5117404A to be packaged in a standard 24/26 pin plastic SOJ, TSOP-II and Reverse TSOP-II.
The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 5V ±10% tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

## FEATURES

- **Low power dissipation**
  **Max. battery back-up2.75mW (SL-part)**
  **Max. CMOS standby 2.2mW (SL-part)**
  **5.5mW**
  **Max. TTL standby 11.0mW**
  **Max. operating**

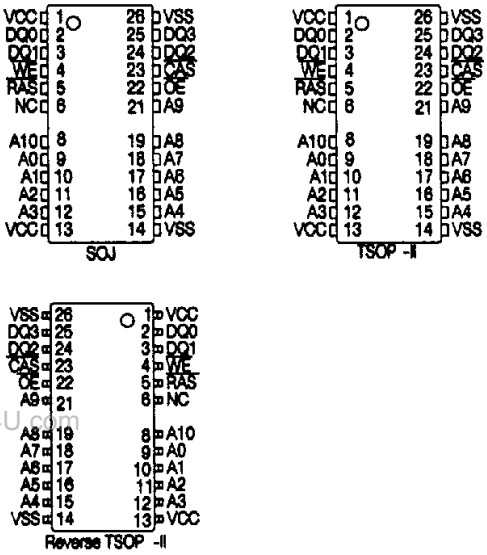
| Speed | Power |
|---|---|
| 60 | 660mW |
| 70 | 550mW |
| 80 | 495mW |

- **Single power supply of 5V±10%**
- **TTL compatible inputs and outputs**
- **Fast access and cycle time**

| Speed | tRAC | tCAC | tHPC |
|---|---|---|---|
| 60 | 60ns | 15ns | 25ns |
| 70 | 70ns | 18ns | 30ns |
| 80 | 80ns | 20ns | 35ns |

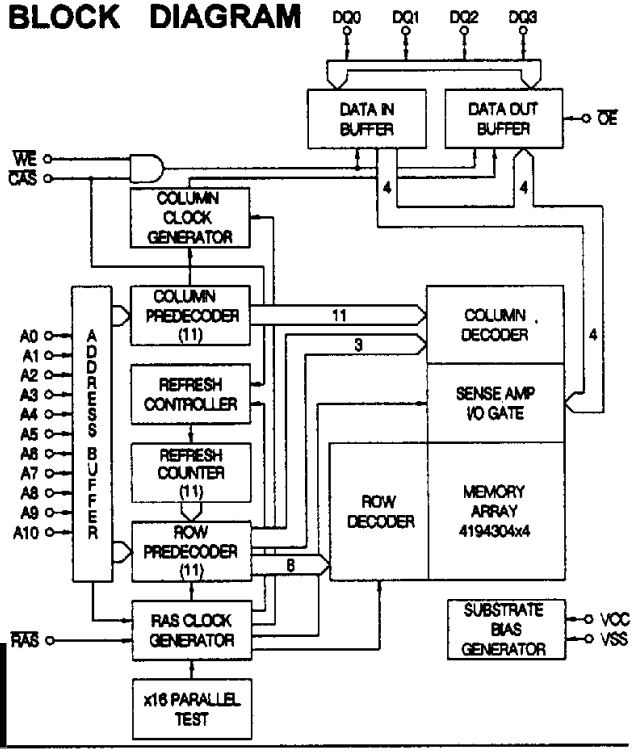
- **Extended Data Out Operation**
- **Multi-bit test capability**
- **Read-Modify-Write capability**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh and Self Refresh capability**
- **2048 refresh cycles / 256ms (SL-part)**
  **2048 refresh cycles / 32ms**

## PIN CONNECTION






## BLOCK DIAGRAM




## PIN DESCRIPTION

| | |
|---|---|
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |
| A0-A10 | Address input |
| DQ0-DQ3 | Data Input/Output |
| Vcc | Power (+5V) |
| Vss | Ground |

## ABSOLUTE MAXIMUM RATING

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_A$ | Ambient Temperature | 0 to 70 | °C |
| $T_{STG}$ | Storage Temperature | -55 to 125 | °C |
| $V_{IN}$, $V_{OUT}$ | Voltage on Any Pin Relative to Vss | -1.0 to 7.0 | V |
| $V_{CC}$ | Voltage on Vcc Relative to Vss | -1.0 to 7.0 | V |
| $I_{OS}$ | Short Circuit Output Current | 50 | mA |
| $P_D$ | Power Dissipation | 1.0 | W |
| $T_{SOLDER}$ | Soldering Temperature • Time | 260 • 10 | °C • sec |

NOTE: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

## RECOMMENDED DC OPERATING CONDITIONS

($T_A$ = 0°C to 70°C)

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | Input High Voltage | 2.4 | - | Vcc+1.0 | V |
| $V_{IL}$ | Input Low Voltage | -1.0 | - | 0.8 | V |

NOTE: All Voltage are referenced to Vss.

## DC CHARACTERISTICS

($T_A$=0°C to 70°C, $V_{CC}$=5V±10%, $V_{SS}$=0V, unless otherwise noted.)

| SYMBOL | PARAMETER | TEST CONDITIONS | SPEED/ POWER | MIN. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current (Any Input Pins) | $V_{SS} \le V_{IN} \le V_{CC}$+1.0, All other pins not under test = Vss | | -10 | 10 | µA | |
| $I_{LO}$ | Output Leakage Current (High impedance State) | $V_{SS} \le V_{OUT} \le V_{CC}$ $\overline{RAS}$ & $\overline{CAS}$ = $V_{IH}$ | | -10 | 10 | µA | 1 |
| $I_{CC1}$ | Vcc Supply Current, Operating | $\overline{RAS}$, $\overline{CAS}$ Address cycling $t_{RC}$ = $t_{RC}$ (min.) | 60<br>70<br>80 | -<br>-<br>- | 120<br>100<br>90 | mA | |
| $I_{CC2}$ | Vcc Supply Current, Operating. | $\overline{RAS}$ & $\overline{CAS}$ = $V_{IH}$(min.), other inputs ≥ Vss | | - | 2 | mA | 1 |
| $I_{CC3}$ | Vcc Supply Current, $\overline{RAS}$-only refresh | $t_{RC}$ = $t_{RC}$ (min.) | 60<br>70<br>80 | -<br>-<br>- | 120<br>100<br>90 | mA | 1 |
| $I_{CC4}$ | Vcc Supply Current, EDO mode | $\overline{RAS}$=$V_{IL}$, $\overline{CAS}$ Address cycling $t_{HPC}$ = $t_{HPC}$ (min.) | 60<br>70<br>80 | -<br>-<br>- | 100<br>90<br>80 | mA | |
| $I_{CC5}$ | Vcc Supply Current, CMOS Standby | $\overline{RAS}$ = $\overline{CAS}$ = Vcc-0.2V | <br>SL-part | -<br>- | 1<br>0.4 | mA | 1 |
| $I_{CC6}$ | Vcc Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh | $\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC}$=$t_{RC}$ (min.) | 60<br>70<br>80 | - | 120<br>100<br>90 | mA | |
| $I_{CC7}$ | Vcc Supply Current, Battery Back up (SL-part only) | $t_{RC}$ = 125µs $\overline{CAS}$ = CBR cycling or 0.2V $\overline{OE}$ & $\overline{WE}$ = Vcc-0.2V, A0-A10 = Vcc-0.2V or 0.2V DQ0-DQ3 = 0.2V, Vcc-0.2V or open | $t_{RAS}$ ≤ 300ns<br>$t_{RAS}$ ≤ 1µs | -<br>- | 300<br>500 | µ A | |
| $I_{CC8}$ | Vcc Supply Current Self Refresh (SL-part only) | $\overline{RAS}$ & $\overline{CAS}$ ≤ 0.2V $\overline{OE}$ & $\overline{WE}$ & A0-A10= Vcc-0.2V or o.2V, DQ0-DQ3=Vcc-0.2V,0.2V or open | | - | 300 | µA | |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 4.2mA | | - | 0.4 | V | |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = -5mA | | 2.4 | - | V | |

NOTE :

1. $I_{CC1}$, $I_{CC3}$, $I_{CC4}$ and $I_{CC6}$ depend on output loading and cycle rates. Specified values are obtained with the output open. In $I_{CC1}$, $I_{CC3}$, $I_{CC6}$, address can be changed only once or less while $\overline{RAS}$=$V_{IL}$. In $I_{CC4}$, address can be changed only once or less during a EDO mode cycle ($t_{HPC}$).

## AC CHARACTERISTICS

($T_A$=0°C to 70°C, $V_{CC}$=5V±10%, $V_{SS}$=0V, unless otherwise noted.) $V_{OH}$=2.0V, $V_{OL}$=0.8V

| # | SYMBOL | PARAMETER | HY5117404AJ/T/R/SLJ/SLT/SLR | | | | | | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | -60 | | -70 | | -80 | | | |
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| 1 | tRC | Random Read or Write Cycle Time | 110 | - | 130 | - | 150 | - | ns | |
| 2 | tRWC | Read-Modify-Write Cycle Time | 155 | - | 180 | - | 200 | - | ns | |
| 3 | tHPC | EDO Mode cycle Time | 25 | - | 30 | - | 35 | - | ns | |
| 4 | tHPRWC | EDO Mode Read-Modify-write Cycle Time | 75 | - | 85 | - | 95 | - | ns | |
| 5 | tRAC | Access Time form $\overline{RAS}$ | - | 60 | - | 70 | - | 80 | ns | 4,5 |
| 6 | tCAC | Access Time from $\overline{CAS}$ | - | 15 | - | 18 | - | 20 | ns | 4,5 |
| 7 | tAA | Access Time from Column Address | - | 30 | - | 35 | - | 40 | ns | 4,5 |
| 8 | tCPA | Access Time from $\overline{CAS}$ Precharge | - | 35 | - | 40 | - | 45 | ns | 4 |
| 9 | tCLZ | $\overline{CAS}$ to Output Low Impedance | 3 | - | 3 | - | 3 | - | ns | 4 |
| 10 | tOFF | Output Buffer Turn-off Delay from $\overline{CAS}$ | 3 | 15 | 3 | 18 | 3 | 20 | ns | 6 |
| 11 | tT | Transition Time (Rise and Fall) | 2 | 50 | 2 | 50 | 2 | 50 | ns | |
| 12 | tRP | $\overline{RAS}$ Precharge Time | 40 | - | 50 | - | 60 | - | ns | |
| 13 | tRAS | $\overline{RAS}$ Pulse Width | 60 | 10K | 70 | 10K | 80 | 10K | ns | |
| 14 | tRASP | $\overline{RAS}$ Pulse Width (EDO Mode) | 60 | 200K | 70 | 200K | 80 | 200K | ns | |
| 15 | tRSH | $\overline{RAS}$ Hold Time | 15 | - | 18 | - | 20 | - | ns | |
| 16 | tCSH | $\overline{CAS}$ Hold Time | 45 | - | 50 | - | 55 | - | ns | |
| 17 | tCAS | $\overline{CAS}$ Pulse width | 11 | 10K | 14 | 10K | 17 | 10K | ns | |
| 18 | tRCD | $\overline{RAS}$ to $\overline{CAS}$ Delay | 20 | 45 | 20 | 50 | 20 | 60 | ns | 5 |
| 19 | tRAD | $\overline{RAS}$ to Column Address Delay Time | 15 | 30 | 15 | 35 | 17 | 40 | ns | 5 |
| 20 | tCRP | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | 5 | - | 5 | - | 5 | - | ns | 7 |
| 21 | tCP | $\overline{CAS}$ Precharge Time | 10 | - | 12 | - | 14 | - | ns | |
| 22 | tASR | Row Address Set-up Time | 0 | - | 0 | - | 0 | - | ns | |
| 23 | tRAH | Row Address Hold time | 10 | - | 10 | - | 12 | - | ns | |
| 24 | tASC | Column Address Set-up Time | 0 | - | 0 | - | 0 | - | ns | |
| 25 | tCAH | Column Address Hold Time | 10 | - | 10 | - | 15 | - | ns | |
| 26 | tAR | Column Address Hold Time from $\overline{RAS}$ | 50 | - | 55 | - | 60 | - | ns | |
| 27 | tRAL | Column Address to $\overline{RAS}$ Lead Time | 30 | - | 35 | - | 40 | - | ns | |
| 28 | tRCS | Read Command Set-up Time | 0 | - | 0 | - | 0 | - | ns | |
| 29 | tRCH | Read Command Hold Time Referenced to $\overline{CAS}$ | 0 | - | 0 | - | 0 | - | ns | 8 |
| 30 | tRRH | Read Command Hold Time Referenced to $\overline{RAS}$ | 0 | - | 0 | - | 0 | - | ns | 8 |
| 31 | tWCH | Write Command Hold Time | 10 | - | 10 | - | 15 | - | ns | 9 |
| 32 | tWCR | Write Command Hold Time from $\overline{RAS}$ | 50 | - | 55 | - | 60 | - | ns | |
| 33 | tWP | Write Command Pulse Width | 10 | - | 10 | - | 15 | - | ns | 9 |
| 34 | tRWL | Write Command to $\overline{RAS}$ Lead Time | 15 | - | 18 | - | 20 | - | ns | |
| 35 | tCWL | Write Command to $\overline{CAS}$ Lead Time | 15 | - | 18 | - | 20 | - | ns | |
| 36 | tDS | Data-In Set-up Time | 0 | - | 0 | - | 0 | - | ns | 10 |
| 37 | tDH | Data-In Hold Time | 10 | - | 10 | - | 10 | - | ns | 10 |
| 38 | tDHR | Data-In Hold Time Referenced to $\overline{RAS}$ | 50 | - | 50 | - | 55 | - | ns | |
| 39 | tREF | Refresh Period (2048) | - | 32 | - | 32 | - | 32 | ms | 13 |
| | | SL-part | - | 256 | - | 256 | - | 256 | | |
| 40 | tWCS | Write Command Set-up Time | 0 | - | 0 | - | 0 | - | ns | 11 |

## AC CHARACTERISTICS

(continued)

| # | SYMBOL | PARAMETER | HY5117404AJ/T/R/SLJ/SLT/SLR | | | | | | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | -60 | | -70 | | -80 | | | |
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| 41 | tCWD | $\overline{CAS}$ to $\overline{WE}$ Delay Time | 40 | - | 45 | - | 50 | - | ns | 12 |
| 42 | tRWD | $\overline{RAS}$ to $\overline{WE}$ Delay Time | 80 | - | 95 | - | 105 | - | ns | 12 |
| 43 | tAWD | Column Address to $\overline{WE}$ Delay Time | 50 | - | 60 | - | 65 | - | ns | 12 |
| 44 | tCSR | $\overline{CAS}$ Set-up Time (CBR Cycle) | 5 | - | 5 | - | 5 | - | ns | |
| 45 | tCHR | $\overline{CAS}$ Hold Time (CBR Cycle) | 10 | - | 10 | - | 10 | - | ns | |
| 46 | tRPC | $\overline{RAS}$ to $\overline{CAS}$ Precharge Time | 5 | - | 5 | - | 5 | - | ns | |
| 47 | tCPT | $\overline{CAS}$ Precharge Time (CBR Counter Test) | 20 | - | 25 | - | 25 | - | ns | |
| 48 | tROH | $\overline{RAS}$ Hold Time Referenced to $\overline{OE}$ | 10 | - | 10 | | 10 | | ns | |
| 49 | tOEA | $\overline{OE}$ Access Time | - | 15 | - | 18 | - | 20 | ns | |
| 50 | tOED | $\overline{OE}$ to Data Delay | 15 | - | 18 | - | 20 | - | ns | |
| 51 | tOEZ | Output Buffer Turn Off Delay Time from $\overline{OE}$ | 3 | 15 | 3 | 18 | 3 | 20 | ns | 6 |
| 52 | tOEH | $\overline{OE}$ Command Hold Time | 15 | - | 18 | - | 20 | - | ns | |
| 53 | tCPWD | $\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge | 55 | - | 65 | - | 75 | - | ns | |
| 54 | tRHCP | $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge | 35 | - | 40 | - | 45 | - | ns | 12 |
| 55 | tWRP | $\overline{WE}$ to $\overline{RAS}$ Precharge Time(CBR Cycle) | 10 | - | 10 | - | 10 | - | ns | |
| 56 | tWRH | $\overline{WE}$ to $\overline{RAS}$ Hold Time(CBR Cycle) | 10 | - | 10 | - | 10 | - | ns | |
| 57 | tWTS | Write Command Set-up Time (Test Mode In) | 10 | - | 10 | - | 10 | - | ns | |
| 58 | tWTH | Write Command Hold Time (Test Mode In) | 10 | - | 10 | - | 10 | - | ns | |
| 59 | tRASS | $\overline{RAS}$ Pulse Width (Self Refresh Cycle) | 100 | - | 100 | - | 100 | - | µs | |
| 60 | tRPS | $\overline{RAS}$ Precharge Time (Self Refresh Cycle) | 90 | - | 110 | - | 130 | - | ns | |
| 61 | tCHS | $\overline{CAS}$ Hold Time (Self RefreshCycle) | -50 | - | -50 | - | -50 | | ns | |
| 62 | tDOH | Output Data Hold Time | 5 | - | 5 | - | 5 | - | ns | |
| 63 | tREZ | Output Buffer Turn Off Delay Time from $\overline{RAS}$ | 3 | 15 | 3 | 18 | 3 | 20 | ns | 6,14 |
| 64 | tWEZ | Output Buffer Turn Off Delay Time from $\overline{WE}$ | 3 | 15 | 3 | 18 | 3 | 20 | ns | 6 |
| 65 | tWED | $\overline{WE}$ to Data Delay Time | 15 | - | 18 | - | 20 | - | ns | |
| 66 | tOEP | $\overline{OE}$ High Pulse Width | 5 | - | 8 | - | 10 | - | ns | |
| 67 | tWPE | $\overline{WE}$ Pulse Width (EDO Cycle) | 5 | - | 8 | - | 10 | - | ns | |
| 68 | tOCH | $\overline{OE}$ to $\overline{CAS}$ Hold Time | 0 | - | 0 | - | 0 | - | ns | |
| 69 | tCHO | $\overline{CAS}$ Hold Time to $\overline{OE}$ | 5 | - | 8 | - | 10 | - | ns | |

## AC CHARACTERISTICS IN TEST MODE

NOTE 13

| # | SYMBOL | PARAMETER | HY5117404AJ/T/R/SLJ/SLT/SLR | | | | | | UNIT | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | -60 | | -70 | | -80 | | | |
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| 1 | tRC | Random Read or Write Cycle Time | 115 | - | 135 | - | 155 | - | ns | |
| 2 | tRWC | Read-Modify-Write Cycle Time | 160 | - | 185 | - | 215 | - | ns | |
| 3 | tHPC | EDO Mode Cycle Time | 30 | - | 35 | - | 40 | - | ns | |
| 4 | tHPRWC | EDO Mode Read-Modify-Write Cycle Time | 80 | - | 90 | - | 100 | - | ns | |
| 5 | tRAC | Access Time from $\overline{RAS}$ | - | 65 | - | 75 | - | 85 | ns | 4,5 |
| 6 | tCAC | Access Time from $\overline{CAS}$ | - | 20 | - | 23 | - | 25 | ns | 4,5 |
| 7 | tAA | Access Time from Column Address | - | 35 | - | 40 | - | 45 | ns | 4,5 |
| 8 | tCPA | Access Time from $\overline{CAS}$ Precharge | - | 40 | - | 45 | - | 50 | ns | 4 |
| 13 | tRAS | $\overline{RAS}$ Pulse Width | 65 | 10K | 75 | 10K | 85 | 10K | ns | |
| 14 | tRASP | $\overline{RAS}$ Pulse Width (Fast Page Mode) | 65 | 200K | 75 | 200K | 85 | 200K | ns | |
| 15 | tRSH | $\overline{RAS}$ Hold Time | 20 | - | 25 | - | 25 | - | ns | |
| 16 | tCSH | $\overline{CAS}$ Hold Time | 50 | - | 55 | - | 60 | - | ns | |
| 17 | tCAS | $\overline{CAS}$ Pulse Width | 20 | 10K | 23 | 10K | 25 | 10K | ns | |
| 27 | tRAL | Column Address to $\overline{RAS}$ Lead Time | 35 | - | 40 | - | 45 | - | ns | |
| 41 | tCWD | $\overline{CAS}$ to $\overline{WE}$ Delay Time | 45 | - | 50 | - | 55 | - | ns | |
| 42 | tRWD | $\overline{RAS}$ to $\overline{WE}$ Delay Time | 90 | - | 100 | - | 110 | - | ns | |
| 43 | tAWD | Column Address to $\overline{WE}$ Delay Time | 60 | - | 65 | - | 70 | - | ns | |
| 49 | tOEZ | $\overline{OE}$ Access Time | - | 20 | - | 23 | - | 25 | ns | |
| 50 | tOED | $\overline{OE}$ to Data Delay | 20 | - | 20 | - | 25 | - | µs | |
| 52 | tOEH | $\overline{OE}$ Command Hold Time | 20 | - | 23 | - | 25 | - | ns | |

NOTE:

1. An initial pause of 200μs is required after power-up followed by any 8 refresh ($\overline{RAS}$ only $\overline{CAS}$-before-$\overline{RAS}$ refresh) cycle before proper device operation is achieved.
2. If $\overline{RAS}$=Vss during power-up, the HY5117404A could begin an active cycle. These condition results in higher current than necessary which is demanded from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with Vcc during power-up or be held at a valid $V_{IH}$ in order to minimize the power-up current.
3. $V_{IH}$(min.) and $V_{IL}$(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$(min.) and $V_{IL}$(max.), and are assumed to be 3ns for all inputs.
4. Measured at $V_{OH}$=2.0V and $V_{OL}$=0.8V with a load equivalent to 2 TTL loads and 100pF.
5. These parameters define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and $\overline{WE}$ leading edge in Read-Modify-Write cycles.
8. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$, $t_{AWD}$ and $t_{CPWD}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.), and $t_{CPWD} \geq t_{CPWD}$(min.), the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the $t_{RCD}$(max.) limit insures that $t_{RAC}$(max.) can be met. $t_{RCD}$(max.) is specified as a reference point only. If $t_{RCD}$ is greater than the specified $t_{RCD}$(max.) limit, then access time is controlled by $t_{CAC}$.
10. Operation within the $t_{RAD}$(max.) limit insures that $t_{RAC}$(max.) can be met. $t_{RAD}$(max.) is specified as a reference point only. If $t_{RAD}$ is greater than the specified $t_{RAD}$(max.) limit, then access time is controlled by $t_{AA}$.
11. $t_{REF}$(max.)=256ms is applied to SL-Parts (HY5117404ASLJ, HY5117404ASLT and HY5117404ASLR).
12. A burst of 2048 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles must be executed within 64ms(256ms for SL-part) after exiting self refresh.
13. These specifications are applied to the test Mode.
14. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high befoer $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
15. $t_{ASC} \geq t_{CP}$ (min.), Assume tT= 2ns



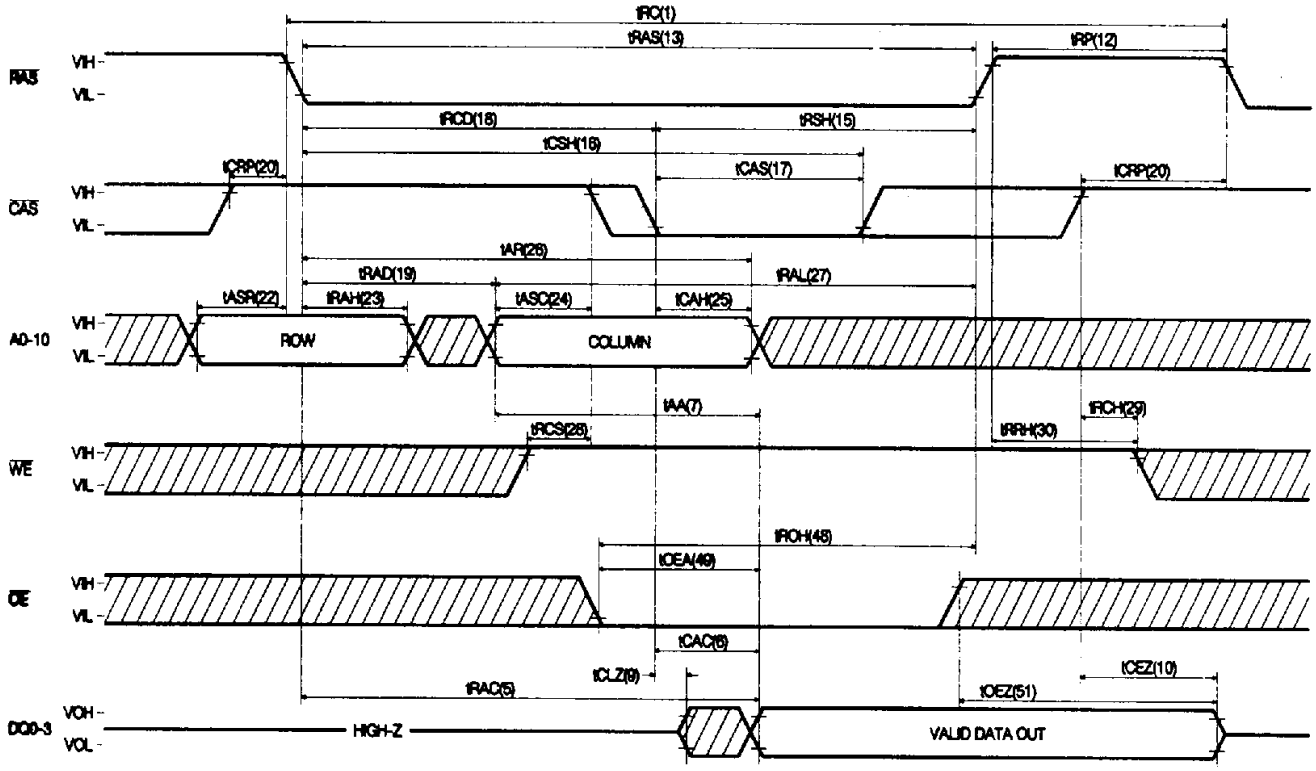
## CAPACITANCE

($T_A$=25°C, Vcc=5V±10%, Vss=0V, f=1MHz, unless otherwise noted.)

| SYMBOL | PARAMETER | TYP. | MAX. | UNIT |
|---|---|---|---|---|
| $C_{IN1}$ | Input Capacitance (A0-A10) | - | 5 | pF |
| $C_{IN2}$ | Input Capacitance ($\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$, $\overline{OE}$) | - | 7 | pF |
| $C_{DQ}$ | Data Input/Output Capacitance (DQ0-DQ3) | - | 7 | pF |

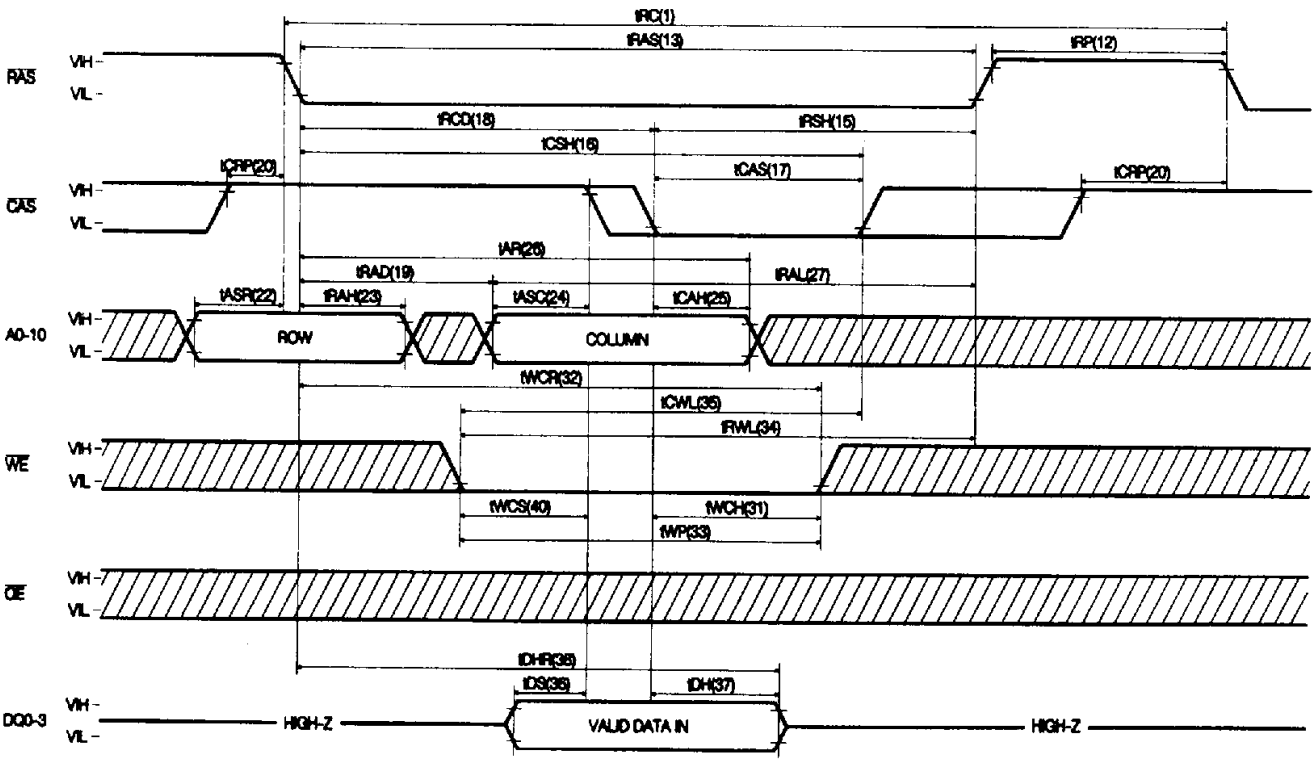
# TIMING DIAGRAM

## READ CYCLE

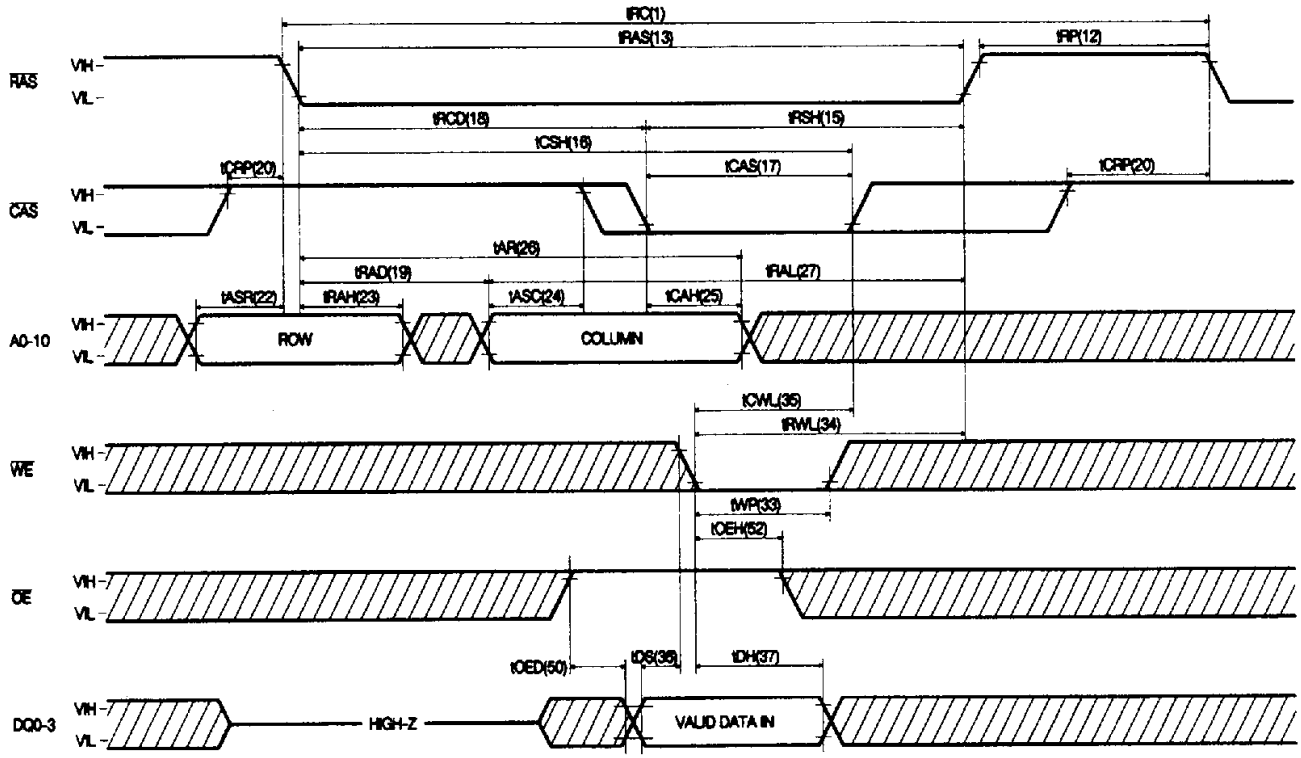




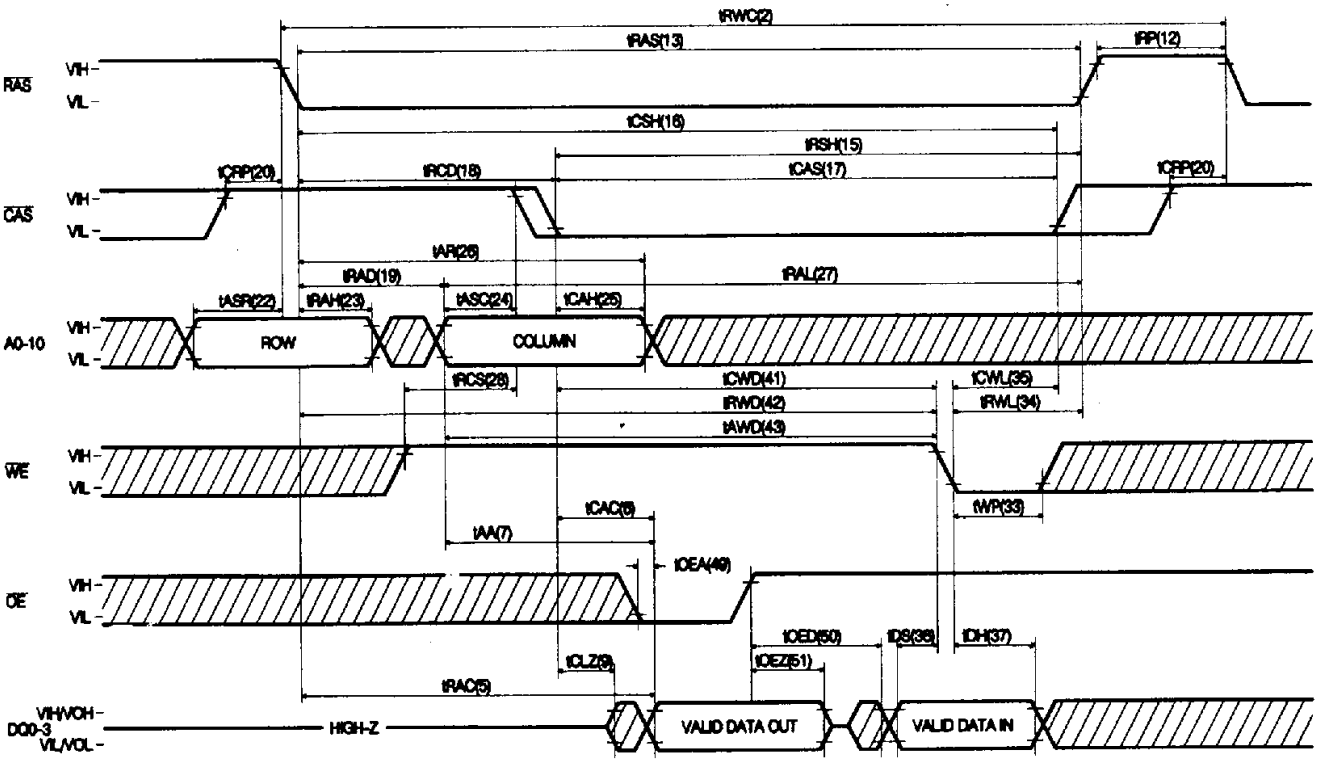

## EARLY WRITE CYCLE



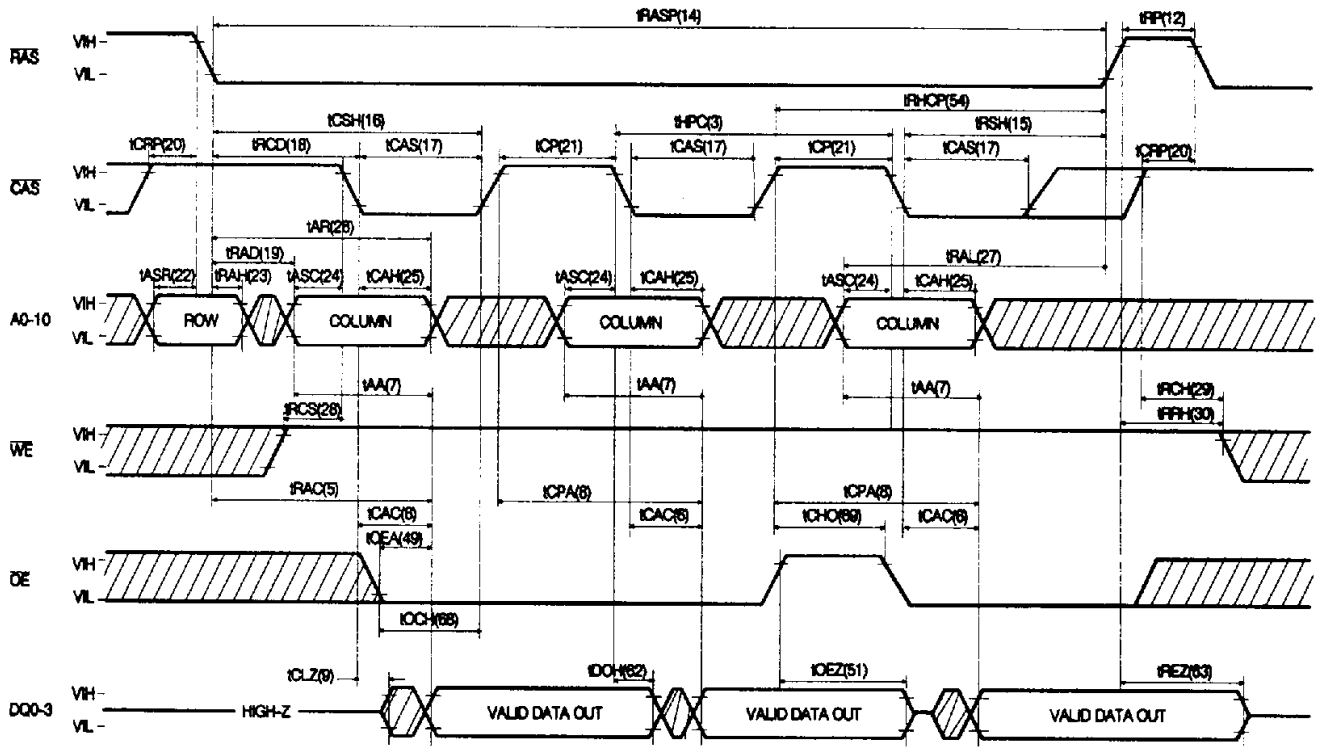
## WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)




## READ-MODIFY-WRITE CYCLE

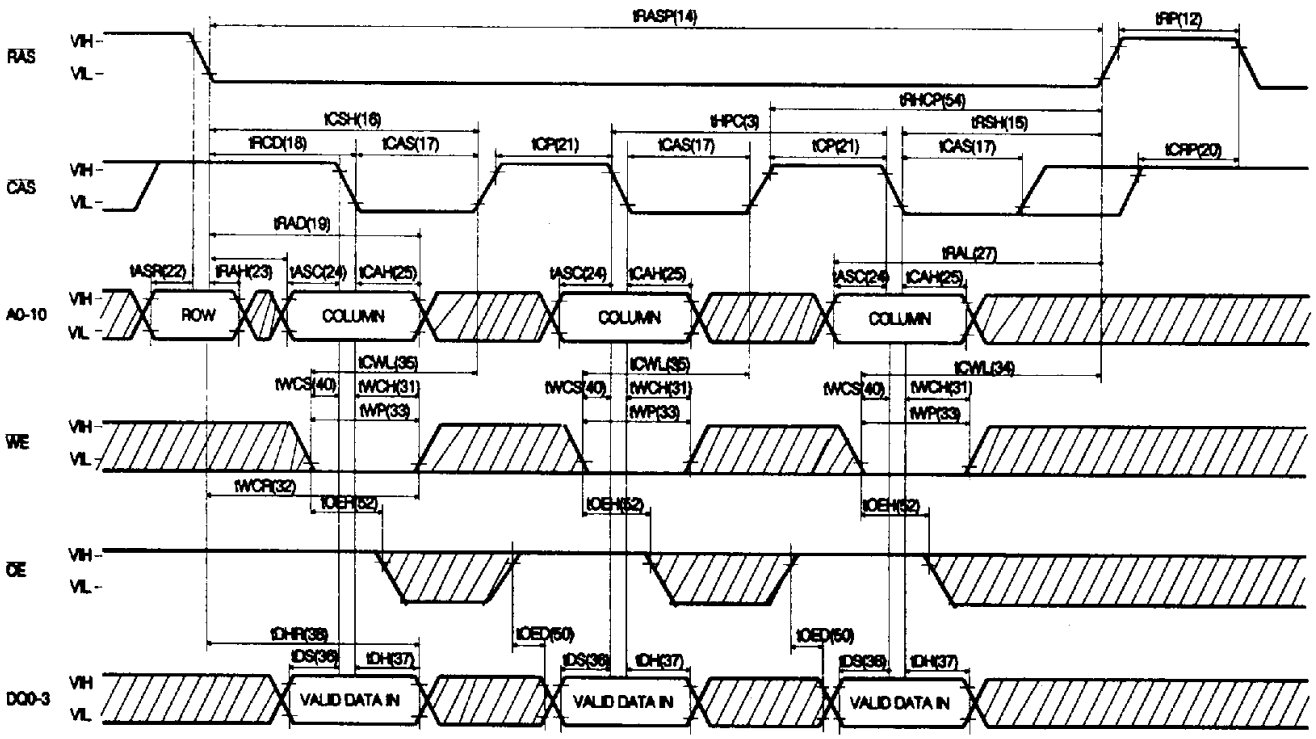


## EDO MODE READ CYCLE

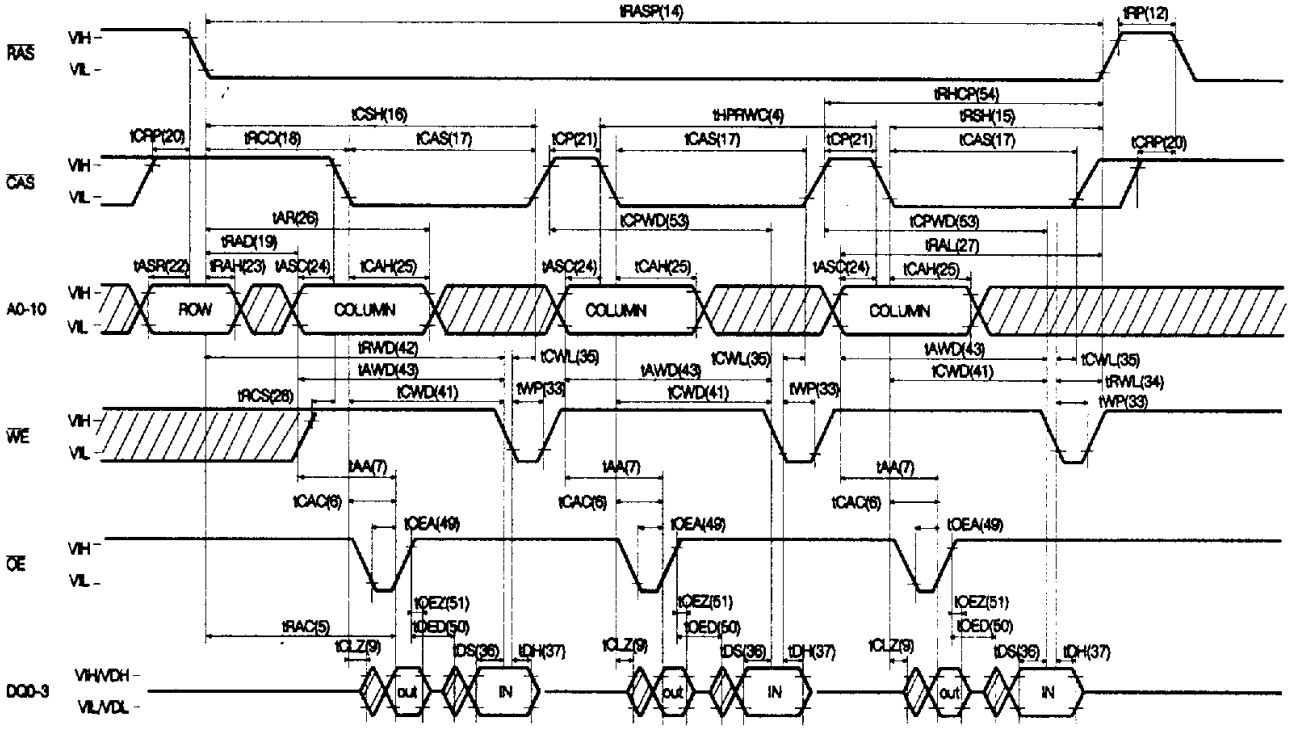




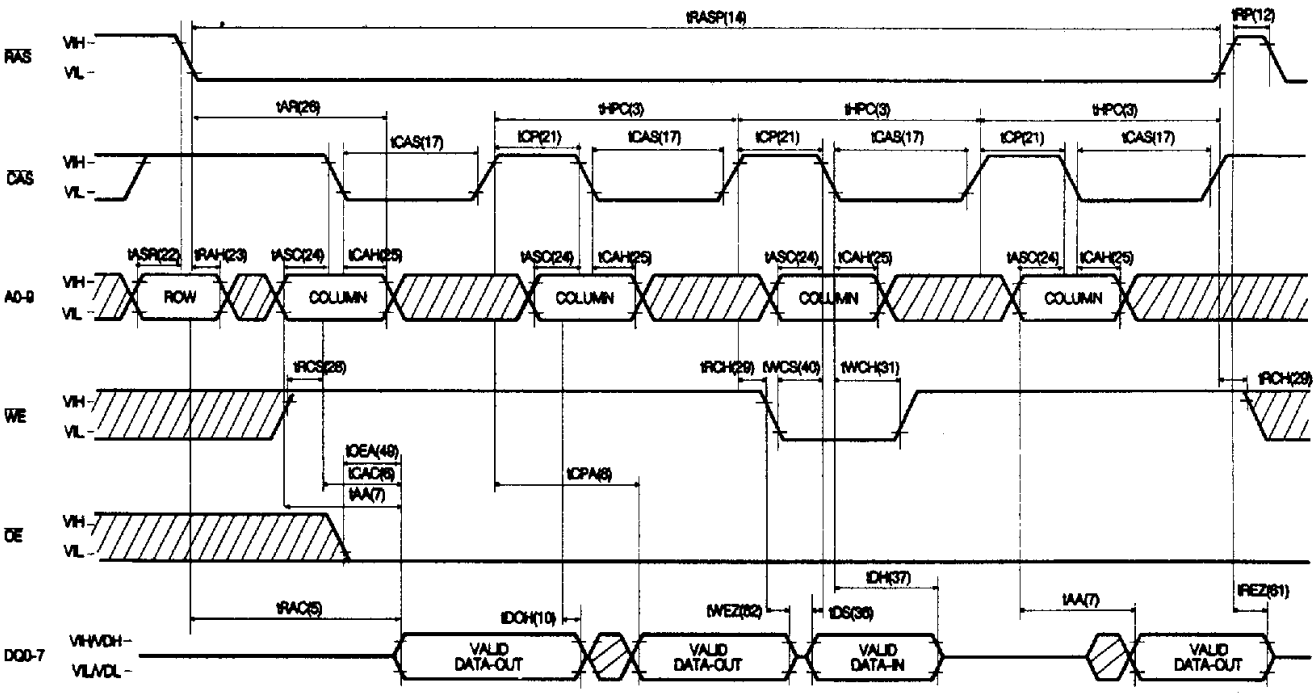

## EDO MODE EARLY WRITE CYCLE



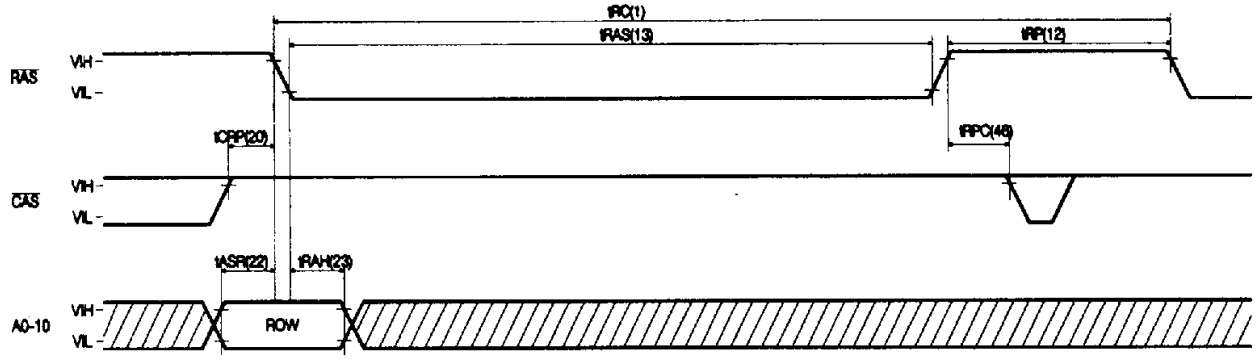
## EDO MODE READ-MODIFY-WRITE CYCLE




## EDO MODE READ AND WRITE MIXED CYCLE

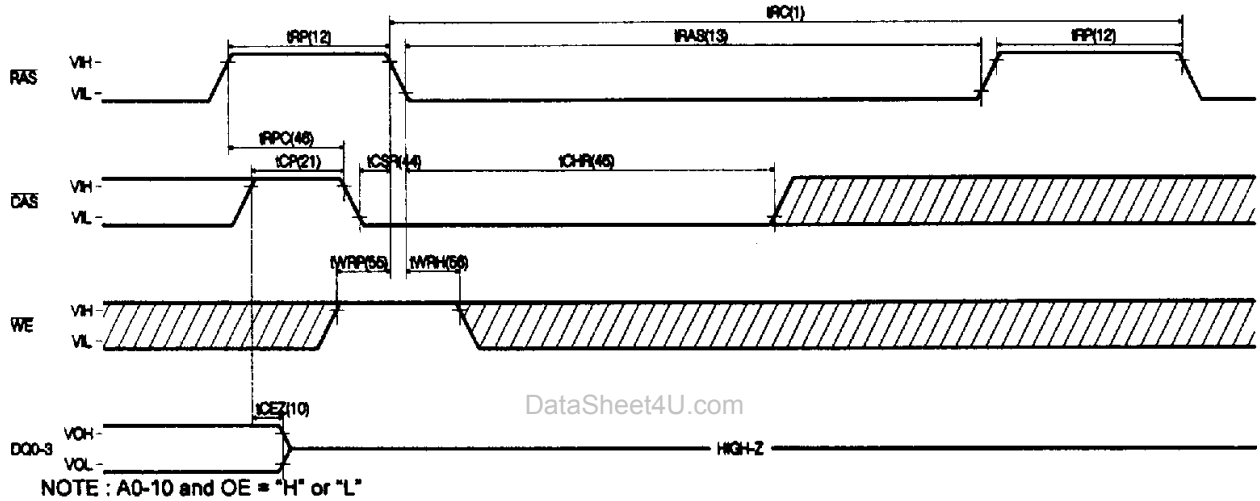


## RAS-ONLY REFRESH CYCLE



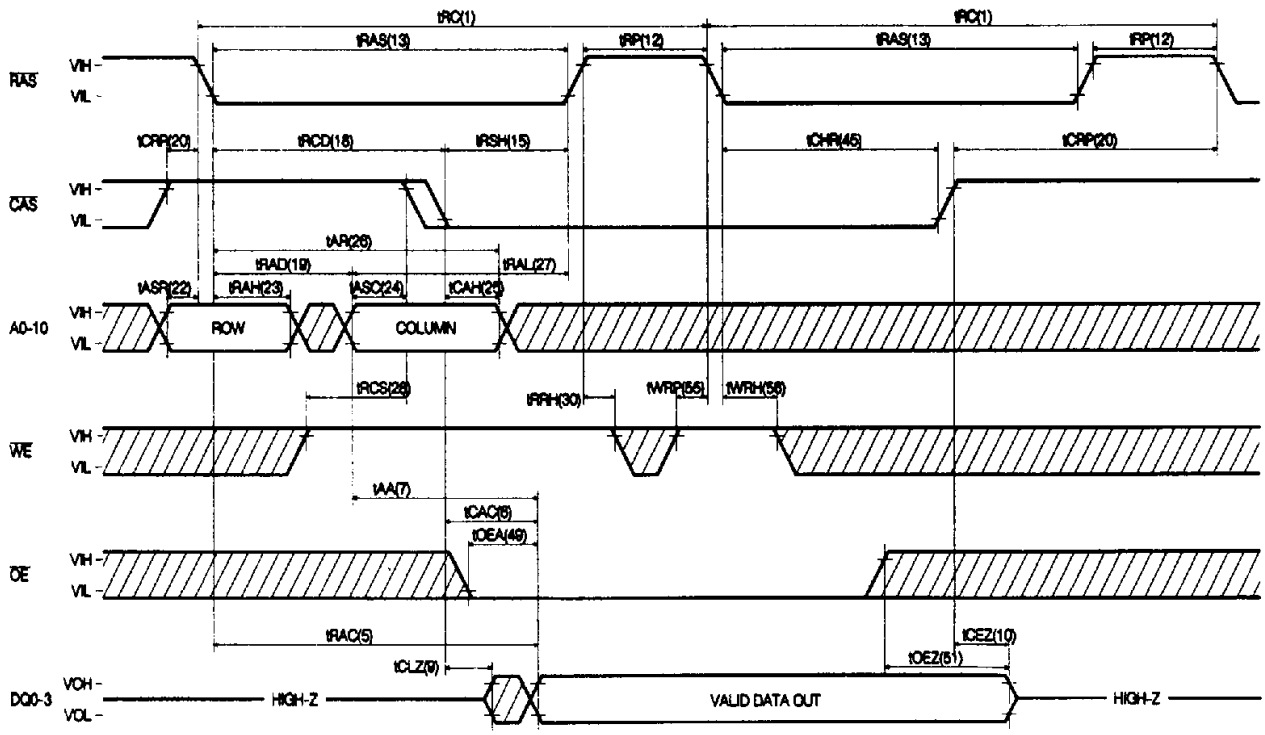

NOTE : $\overline{OE}$ and $\overline{WE}$ = "H" or "L"

## CAS-BEFORE-RAS REFRESH CYCLE

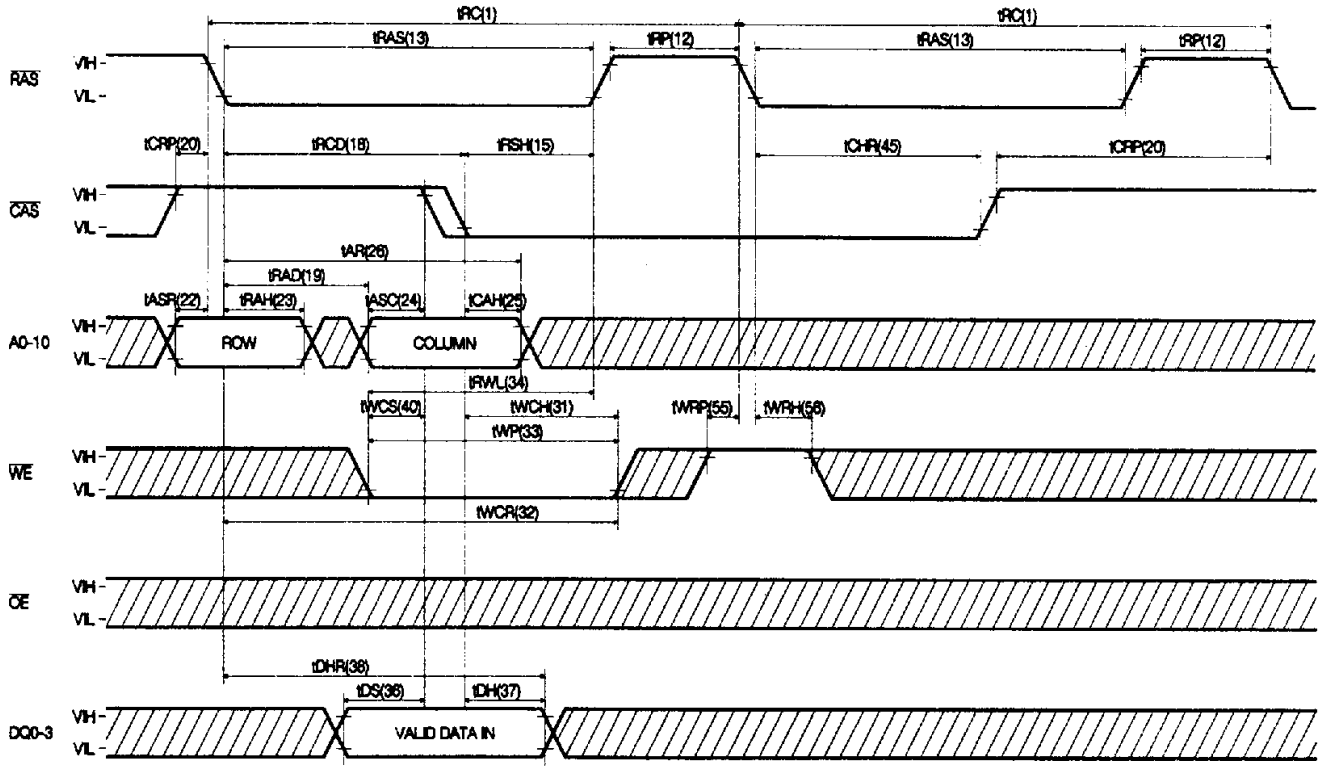



NOTE : A0-10 and OE = "H" or "L"

## HIDDEN REFRESH CYCLE (READ)

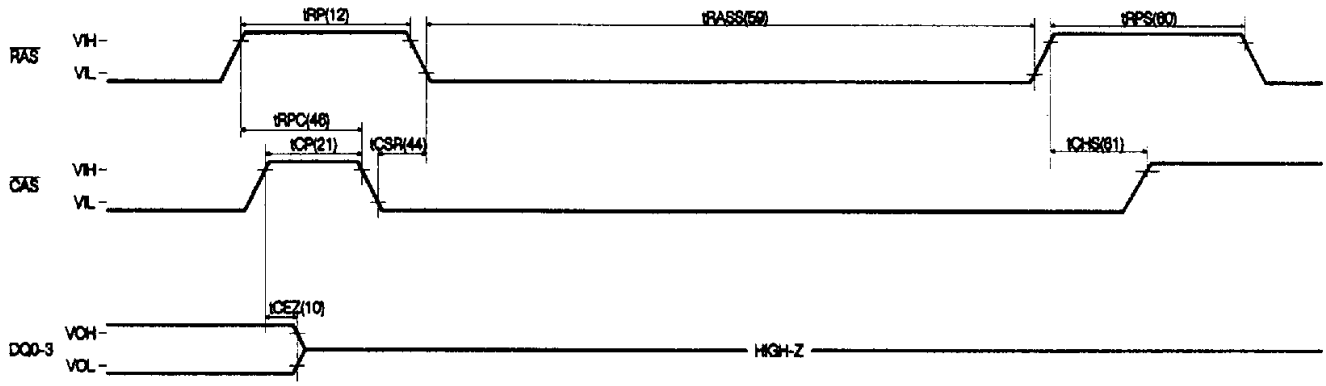


## HIDDEN REFRESH CYCLE (WRITE)



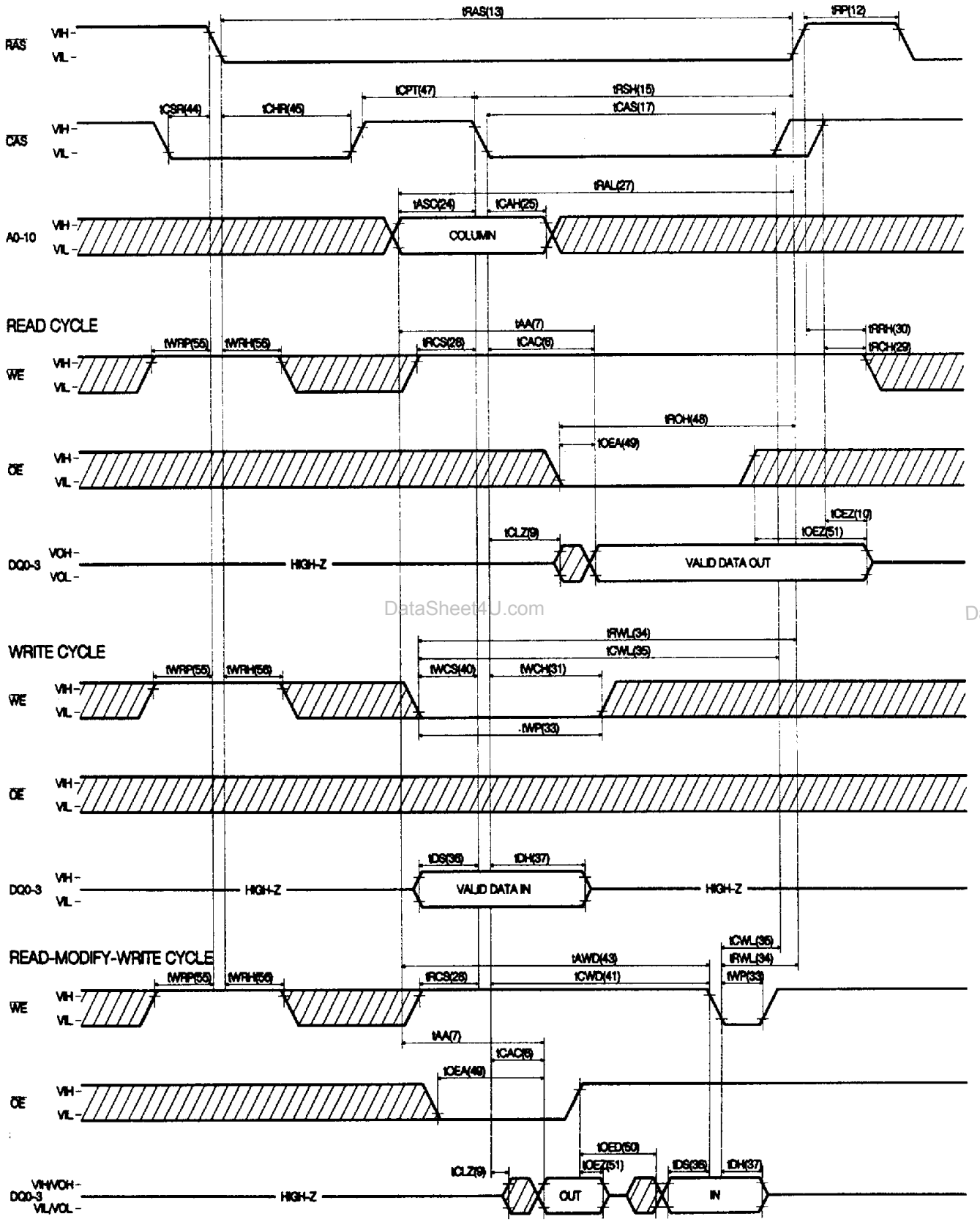



## CAS-BEFORE-RAS SELF REFRESH CYCLE




NOTE : A0-10 OE and WE ="H" or "L"

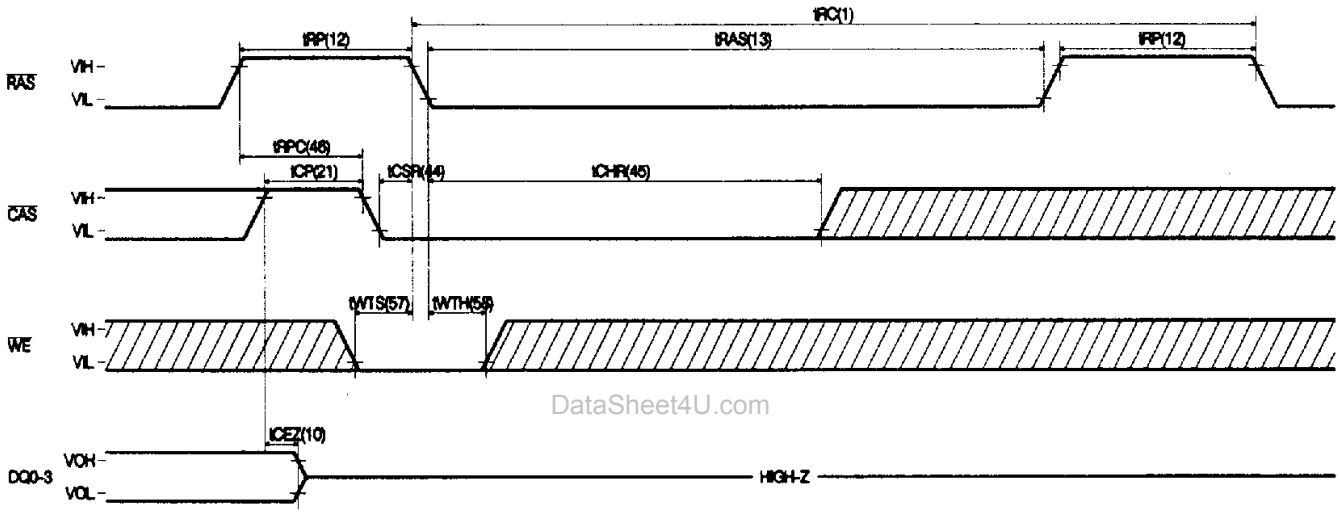
## CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



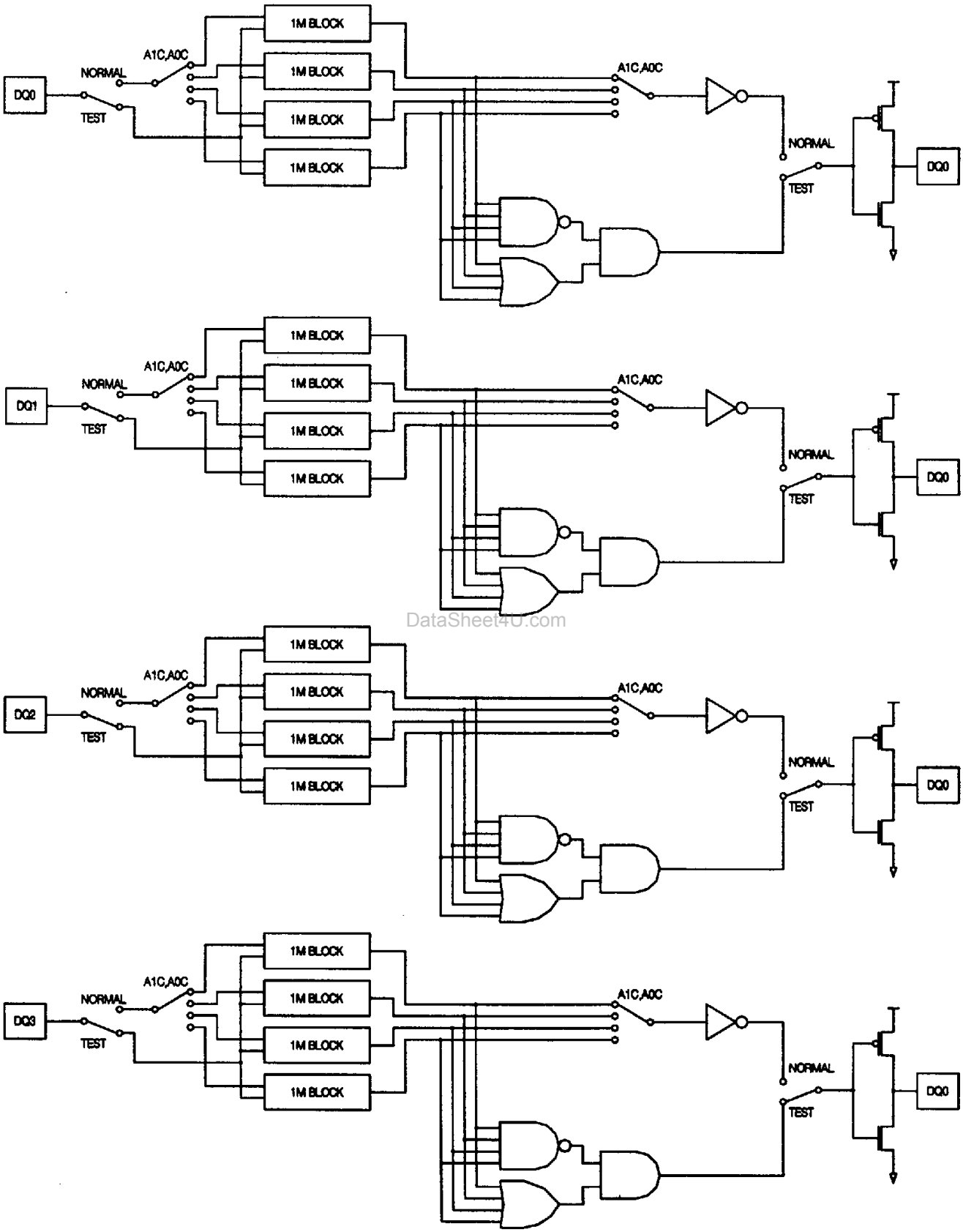
## TEST MODE

The HY5117404A is a DRAM organized 4,194,304 x 4-bit. It is internally organized 1,048,576 x 16-bit. In Test Mode, data are written into 16 sectors (Each is composed of 1M bits) in parallel and retrieved the same way. Column address A0 and A1 are not used. If upon reading, 4-bit data from 4 sectors connected to one DQ pin are equal (all "1"s or "0"s), the DQ pin indicates a "1". If they are not equal, the DQ pin indicates a "0". Belowing shows the timing diagram of the HY5117404A enter Test Mode. In Test Mode, the 4M x 4 DRAM can be tested as if it were a 1M x 4 DRAM. $\overline{WE}$, $\overline{CAS}$-before-$\overline{RAS}$ cycle (Test Mode In Cycle) puts the HY5117404A into Test Mode and $\overline{CAS}$-before-$\overline{RAS}$ or $\overline{RAS}$-only refresh cycle puts it back into Normal Model. In Test Mode, $\overline{WE}$, $\overline{CAS}$-before-$\overline{RAS}$ cycle shall be used for the refresh operation. The Test Mode function reduces test time (1/4 in case of N test pattern).

### TEST MODE IN CYCLE

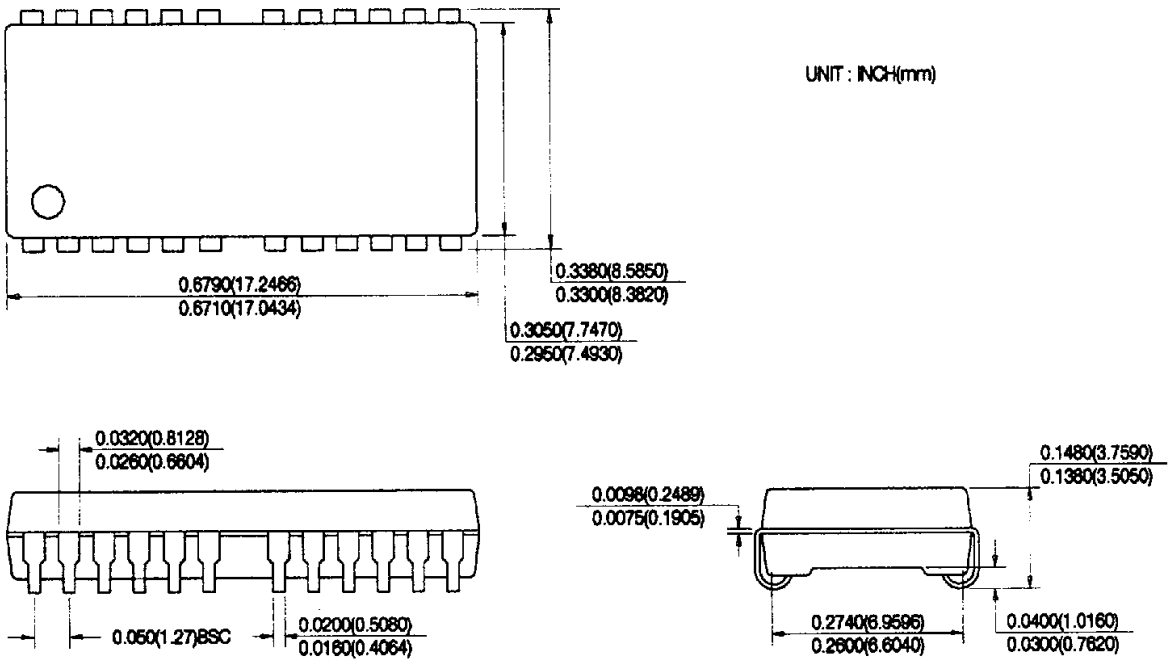


## BLOCK DIAGRAM IN TEST MODE



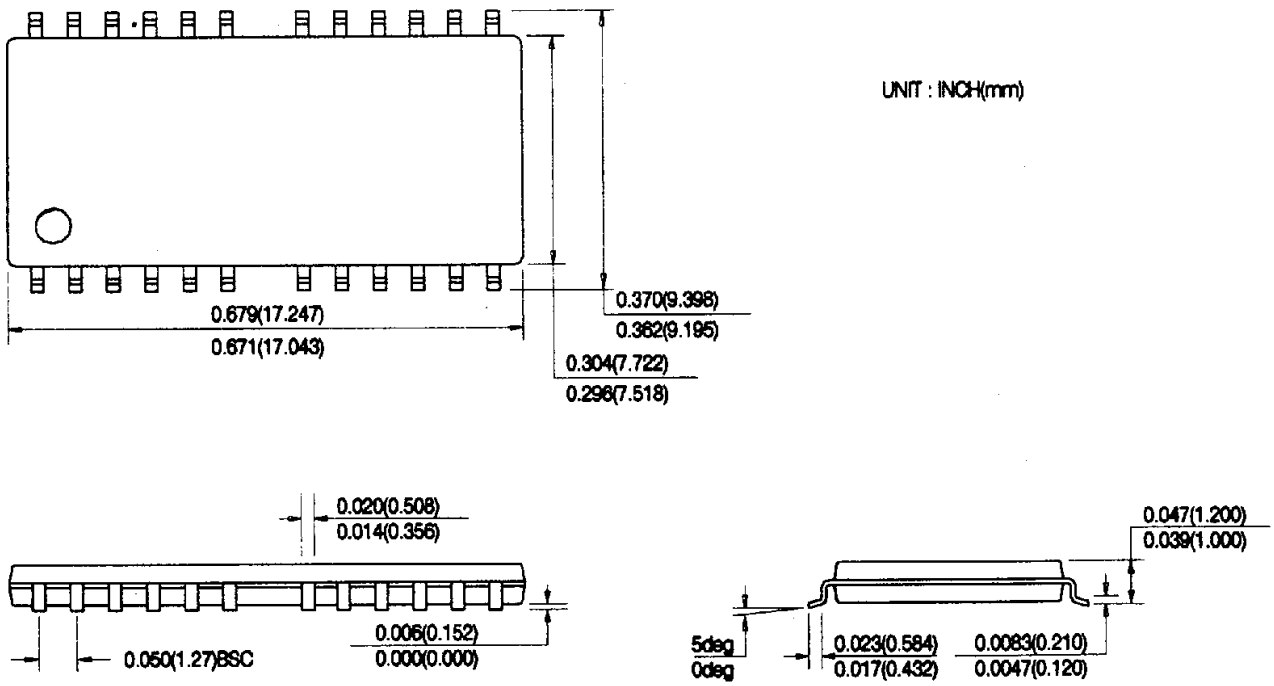
## PACKAGE INFORMATION

### 300 mil 24/26 pin Small Outline J-form Package (J)




### 300 mil 24/26 pin Thin Small Outline Package (T) (R)





## ORDERING INFORMATION

| PART NUMBER | SPEED | POWER | PACKAGE |
|---|---|---|---|
| HY5117404AJ | 60/70/80 | | SOJ |
| HY5117404ASLJ | 60/70/80 | SL-part | SOJ |
| HY5117404AT | 60/70/80 | | TSOP-II |
| HY5117404ASLT | 60/70/80 | SL-part | TSOP-II |
| HY5117404AR | 60/70/80 | | TSOP-II(R) |
| HY5117404ASLR | 60/70/80 | SL-part | TSOP-II(R) |