Serial EEPROM Series Automotive EEPROM

105℃ Operation I²C BUS EEPROM (2-Wire)

BR24Axxx-WM
(1K 2K 4K 8K 16K 32K 64K)

●General Description

BR24Axxx-WM is a serial EEPROM of I²C BUS interface method.

●Features

- Completely conforming to the world standard I²C BUS. All controls available by 2 ports of serial clock (SCL) and serial data (SDA)
- Wide temperature range -40℃ to +105℃
- Other devices than EEPROM can be connected to the same port, saving microcontroller port
- 2.5V to 5.5V single power source operation most suitable for battery use
- Page write mode useful for initial value write at factory shipment
- Auto erase and auto end function at data rewrite
- Low current consumption
  - At write operation (5V) : 1.2mA (Typ.) *1
  - At read operation (5V) : 0.2mA (Typ.)
  - At standby condition (5V) : 0.1μA (Typ.)
- Write mistake prevention function
  - Write (write protect) function added
  - Write mistake prevention function at low voltage
- Data rewrite up to 1,000,000 times(Ta≦25℃)
- Data kept for 40 years(Ta≦25℃)
- Noise filter built in SCL / SDA terminal
- Shipment data all address FFh

*1 BR24A32-WM, BR24A64-WM : 1.5mA

●Packages W(Typ.) x D(Typ.) x H(Max.)

SOP8
5.00mm x 6.20mm x 1.71mm

SOP- J8
4.90mm x 6.00mm x 1.65mm

MSOP8
2.90mm x 4.00mm x 0.90mm

●Page write

Number of Pages	8Byte	16Byte	32Byte
Product number	BR24A01A-WM BR24A02-WM	BR24A04-WM BR24A08-WM BR24A16-WM	BR24A32-WM BR24A64-WM

●BR24Axxx-WM

Capacity	Bit format	Type	Power source voltage	SOP8	SOP-J8	MSOP8
1Kbit	128×8	BR24A01A-WM	2.5V to 5.5V	●	●	
2Kbit	256×8	BR24A02-WM	2.5V to 5.5V	●	●	●
4Kbit	512×8	BR24A04-WM	2.5V to 5.5V	●	●	
8Kbit	1K×8	BR24A08-WM	2.5V to 5.5V	●	●	
16Kbit	2K×8	BR24A16-WM	2.5V to 5.5V	●	●	
32Kbit	4K×8	BR24A32-WM	2.5V to 5.5V	●		
64Kbit	8K×8	BR24A64-WM	2.5V to 5.5V	●		

○Product structure: Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

●Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Ratings	Unit	Remarks
Supply Voltage	V_{CC}	-0.3 to +6.5	V	
Power Dissipation	Pd	450 (SOP8)	mW	When using at Ta=25℃ or higher 4.5mW to be reduced per 1℃.
		450 (SOP-J8)		When using at Ta=25℃ or higher 4.5mW to be reduced per 1℃.
		310 (MSOP8)		When using at Ta=25℃ or higher 3.1mW to be reduced per 1℃.
Storage Temperature	Tstg	-65 to +125	℃	
Operating Temperature	Topr	-40 to +105	℃	
Terminal Voltage	-	-0.3 to V_{CC}+1.0	V	

●Memory cell characteristics (V_{CC}=2.5V to 5.5V)

Parameter	Limits			Unit	Conditions
	Min.	Typ.	Max		
Number of data rewrite times *1	1,000,000	-	-	Times	Ta≦25℃
	100,000	-	-		Ta≦105℃
Data hold years *1	40	-	-	Years	Ta≦25℃
	10	-	-		Ta≦105℃

○Shipment data all address FFh
*1Not 100% TESTED

●Recommended Operating Ratings

Parameter	Symbol	Ratings	Unit
Power source voltage	V_{CC}	2.5 to 5.5	V
Input voltage	V_{IN}	0 to V_{CC}	

●Electrical characteristics (Unless otherwise specified, Ta=-40℃ to +105℃, V_{CC}=2.5V to 5.5V)

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
"HIGH" input voltage	V_{IH}	0.7 V_{CC}	-	-	V	
"LOW" input voltage	V_{IL}	-	-	0.3 V_{CC}	V	
"LOW" output voltage 1	V_{OL}	-	-	0.4	V	I_{OL}=3.0mA (SDA)
Input leak current	I_{LI}	-1	-	1	μA	V_{IN}=0V to V_{CC}
Output leak current	I_{LO}	-1	-	1	μA	V_{OUT}=0V to V_{CC}, (SDA)
Current consumption	I_{CC1}	-	-	2.0 *1 3.0 *2	mA	V_{CC} =5.5V,f_{SCL}=400kHz, t_{WR}=5ms, Byte write, Page write
	I_{CC2}	-	-	0.5	mA	V_{CC} =5.5V,f_{SCL}=400kHz Random read, current read, sequential read
Standby current	I_{SB}	-	-	2.0	μA	V_{CC} =5.5V, SDA・SCL= V_{CC} A0, A1, A2=GND, WP=GND

*1 BR24A01A/02/04/08/16-WM, *2 BR24A32/64-WM

●Operating timing characteristics (Unless otherwise specified, Ta=-40℃ to +105℃, V_{CC}=2.5V to 5.5V)

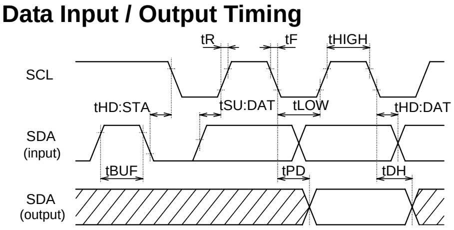
Parameter	Symbol	FAST-MODE 2.5V≦V_{CC}≦5.5V			STANDARD-MODE 2.5V≦V_{CC}≦5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL frequency	f_{SCL}	-	-	400	-	-	100	kHz
Data clock “HIGH“ time	t_{HIGH}	0.6	-	-	4.0	-	-	μs
Data clock “LOW“ time	t_{LOW}	1.2	-	-	4.7	-	-	μs
SDA, SCL rise time *1	t_R	-	-	0.3	-	-	1.0	μs
SDA, SCL fall time *1	t_F	-	-	0.3	-	-	0.3	μs
Start condition hold time	$t_{HD:STA}$	0.6	-	-	4.0	-	-	μs
Start condition setup time	$t_{SU:STA}$	0.6	-	-	4.7	-	-	μs
Input data hold time	$t_{HD:DAT}$	0	-	-	0	-	-	ns
Input data setup time	$t_{SU:DAT}$	100	-	-	250	-	-	ns
Output data delay time	t_{PD}	0.1	-	0.9	0.2	-	3.5	μs
Output data hold time	t_{DH}	0.1	-	-	0.2	-	-	μs
Stop condition setup time	$t_{SU:STO}$	0.6	-	-	4.7	-	-	μs
Bus release time before transfer start	t_{BUF}	1.2	-	-	4.7	-	-	μs
Internal write cycle time	t_{WR}	-	-	5	-	-	5	ms
Noise removal valid period (SDA, SCL terminal)	t_I	-	-	0.1	-	-	0.1	μs
WP hold time	$t_{HD:WP}$	0	-	-	0	-	-	ns
WP setup time	$t_{SU:WP}$	0.1	-	-	0.1	-	-	μs
WP valid time	$t_{HIGH:WP}$	1.0	-	-	1.0	-	-	μs

*1 Not 100% tested

●FAST-MODE and STANDARD-MODE

FAST-MODE and STANDARD-MODE are of same operations, and mode is changed. They are distinguished by operating speeds. 100kHz operation is called STANDARD-MODE, and 400kHz operation is called FAST-MODE. This operating frequency is the maximum operating frequency, so 100kHz clock may be used in FAST-MODE. At V_{CC} =2.5V to 5.5V, 400kHz, namely, operation is made in FASTMODE. (Operation is made also in STANDARD-MODE.)

●Sync Data Input / Output Timing



○Input read at the rise edge of SCL
○Data output in sync with the fall of SCL

Figure 1-(a) Sync data input / output timing

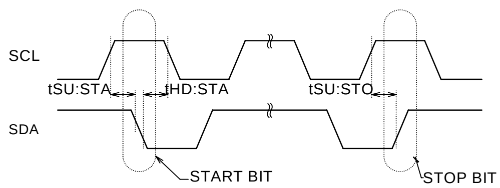


Figure 1-(b) Start-stop bit timing

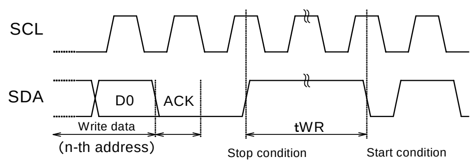


Figure 1-(c) Write cycle timing

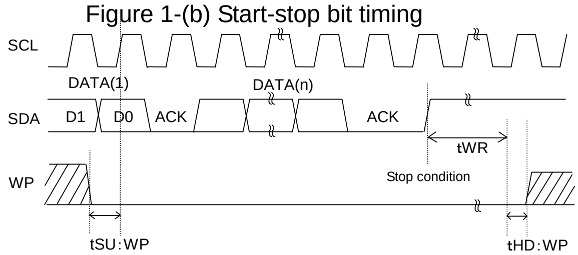
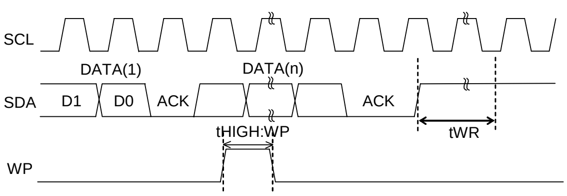


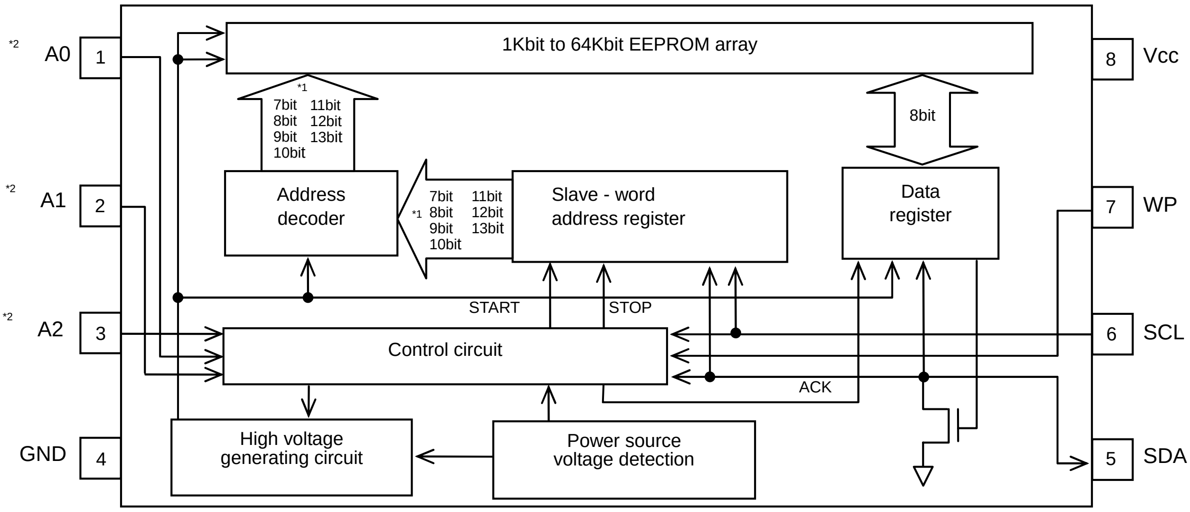
Figure 1-(d) WP timing at write execution



○At write execution, in the area from the D0 taken clock rise of the first DATA(1), to tWR, set WP=“LOW”.
○By setting WP “HIGH” in the area, write can be cancelled.
When it is set WP=“HIGH” during tWR, write is forcibly ended, and data of address under access is not guaranteed, therefore write it once again.

Figure 1-(e) WP timing at write cancel

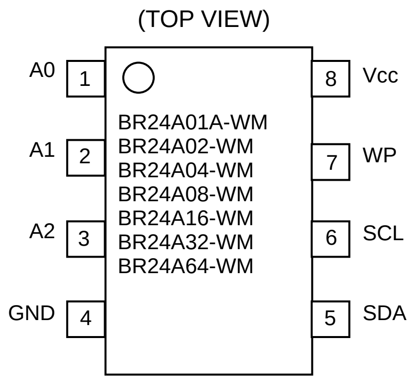
●Block Diagram



*1 7bit : BR24A01A-WM
8bit : BR24A02-WM
9bit : BR24A04-WM
10bit : BR24A08-WM
11bit : BR24A16-WM
12bit : BR24A32-WM
13bit : BR24A64-WM

*2 A0=N.C. : BR24A04-WM
A0, A1=N.C. : BR24A08-WM
A0, A1= N.C. A2=Don't Use : BR24A16-WM

●Pin Configuration



●Pin Descriptions

Terminal name	Input / output	Function						
		BR24A01A-WM	BR24A02-WM	BR24A04-WM	BR24A08-WM	BR24A16-WM	BR24A32-WM	BR24A64-WM
A0	Input	Slave address setting		Not connected			Slave address setting	
A1	Input	Slave address setting			Not connected		Slave address setting	
A2	Input	Slave address setting				Not used	Slave address setting	
GND	-	Reference voltage of all input / output, 0V						
SDA	Input / output	Slave and word address, Serial data input serial data output						
SCL	Input	Serial clock input						
WP	Input	Write protect terminal						
Vcc	-	Connect the power source.						

●**Typical Performance Curves**
(The following values are Typ. ones.)

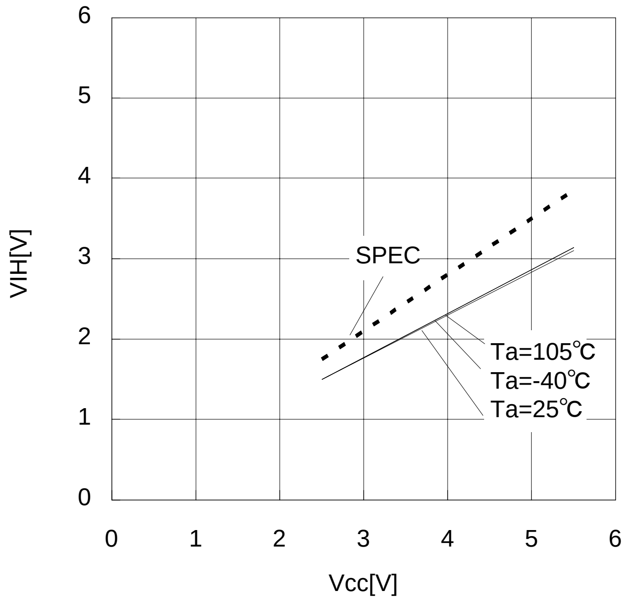


Figure 2. H input voltage VIH1,2
(SCL,SDA,WP)

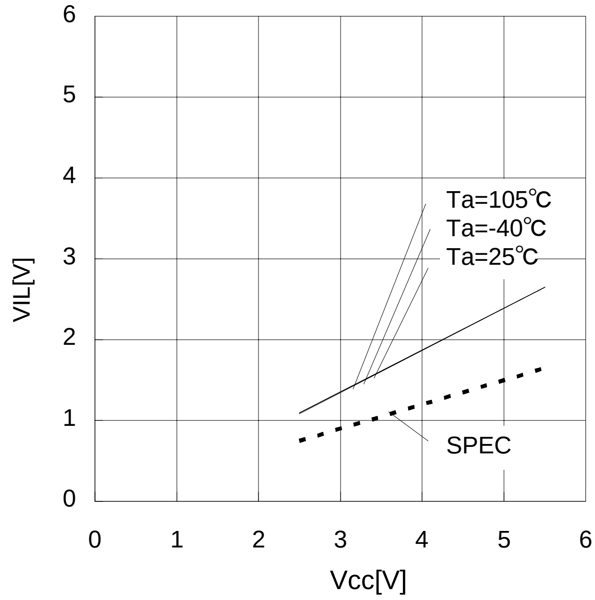


Figure 3. L input voltageVIL1,2
(SCL,SDA,WP)

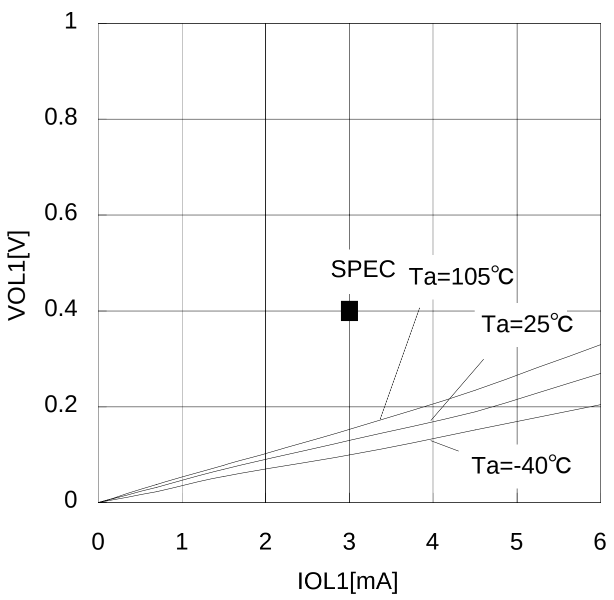


Figure 4. L output voltage VOL1-IOL1
(V_{CC} =2.5V)

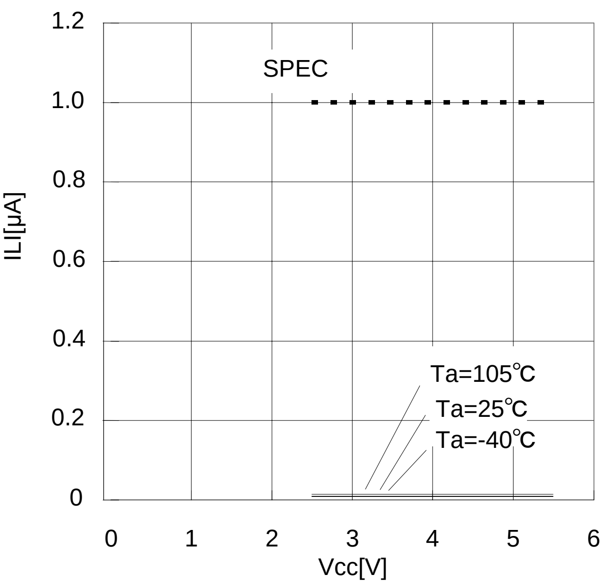


Figure 5. Input leak current ILI (SCL,WP)

●**Typical Performance Curves - Continued**

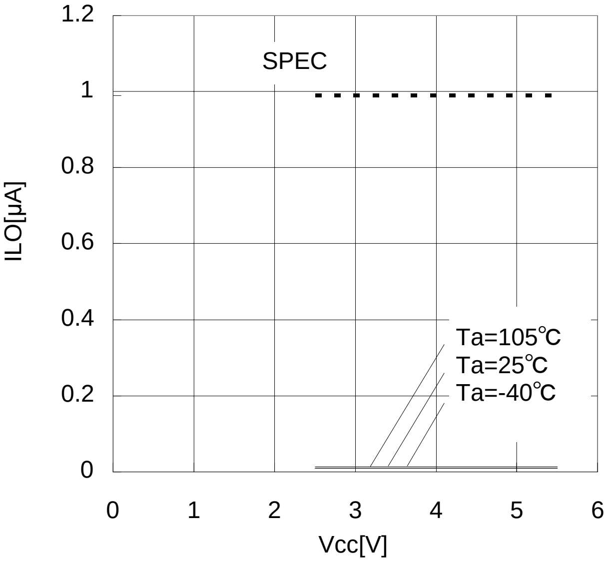


Figure 6. Output leak current ILO(SDA)

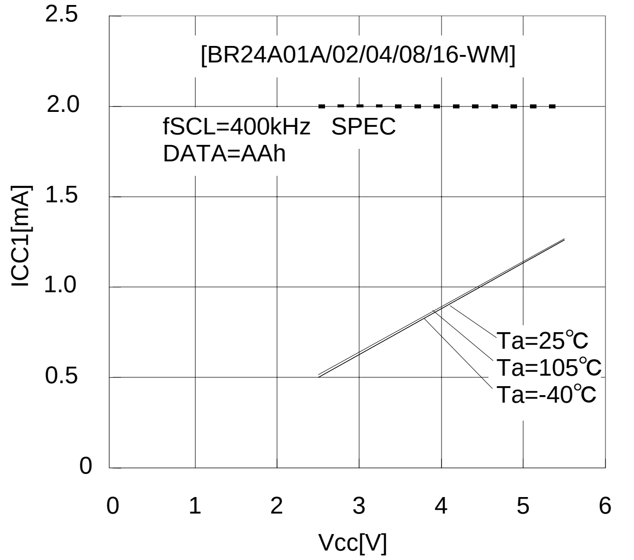


Figure 7. Current consumption at WRITE operation ICC1 (fSCL=400kHz)

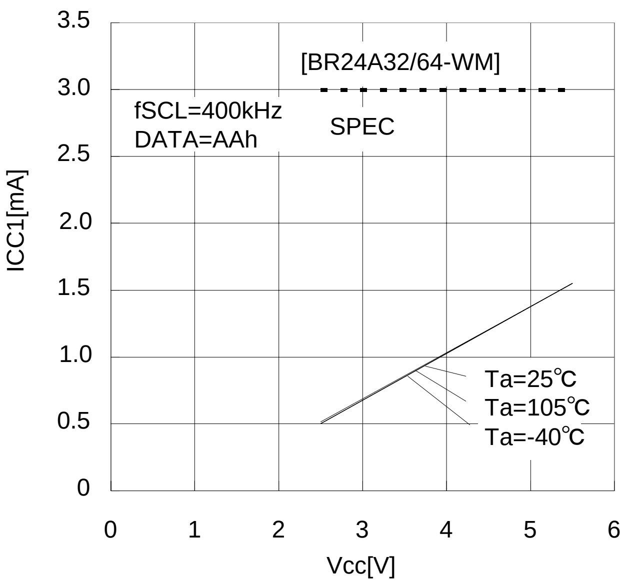


Figure 8. Current consumption at WRITE operation ICC1 (fSCL=400kHz)

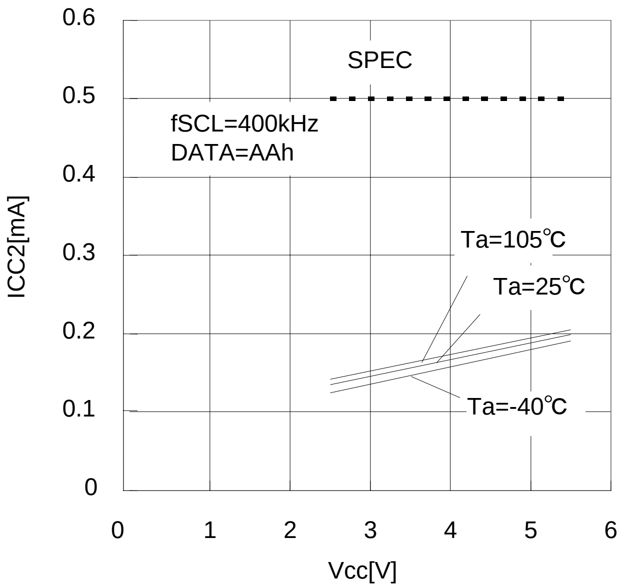


Figure 9. Current consumption at READ operation ICC2 (fSCL=400kHz)

● **Typical Performance Curves - Continued**

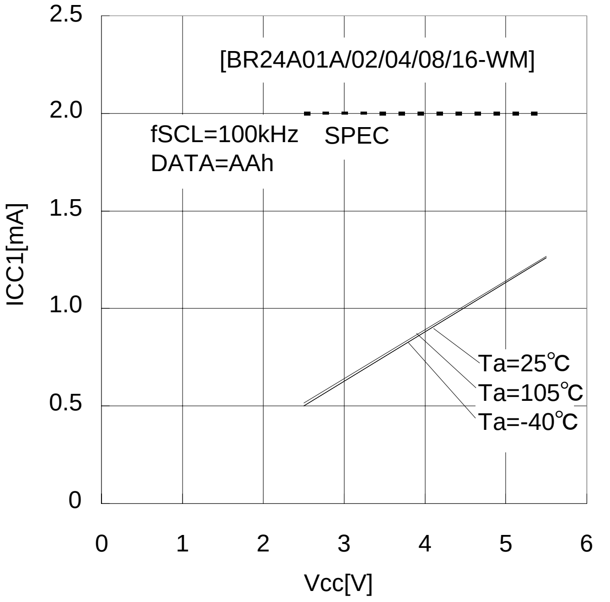


Figure 10. Current consumption at WRITE operation ICC1 (fSCL=100kHz)

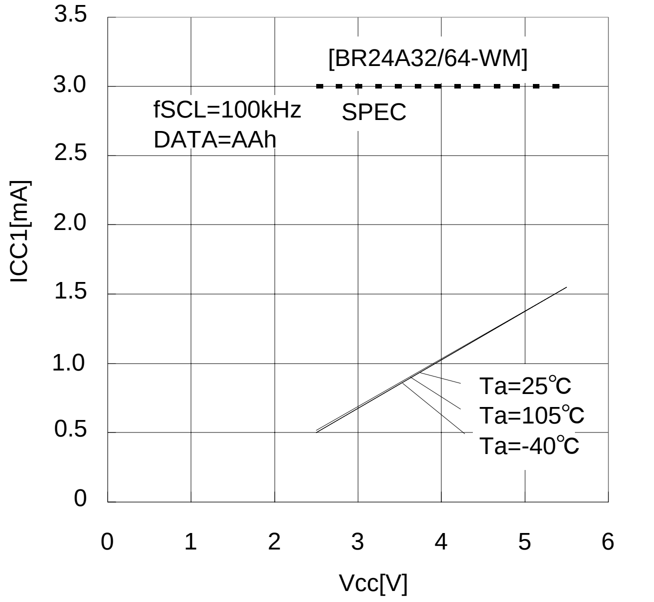


Figure 11. Current consumption at WRITE operation ICC1 (fSCL=100kHz)

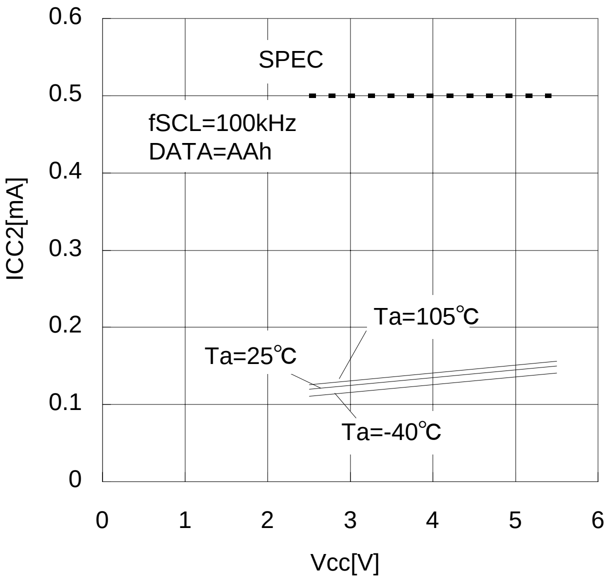


Figure 12. Current consumption at READ operation ICC2 (fSCL=100kHz)

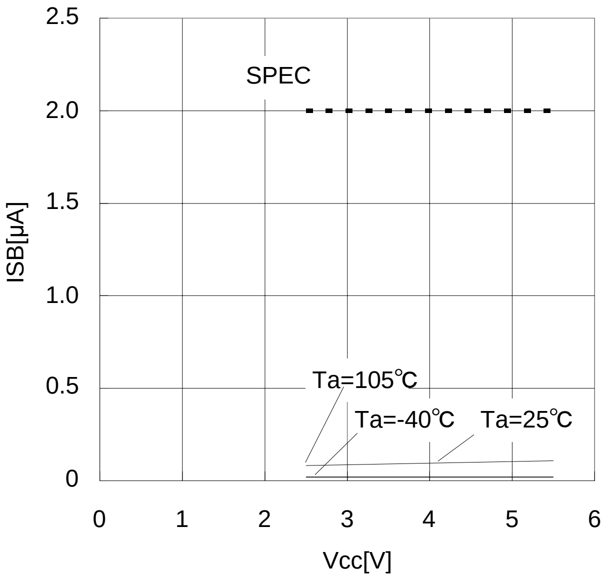


Figure 13. Standby current ISB

●**Typical Performance Curves - Continued**

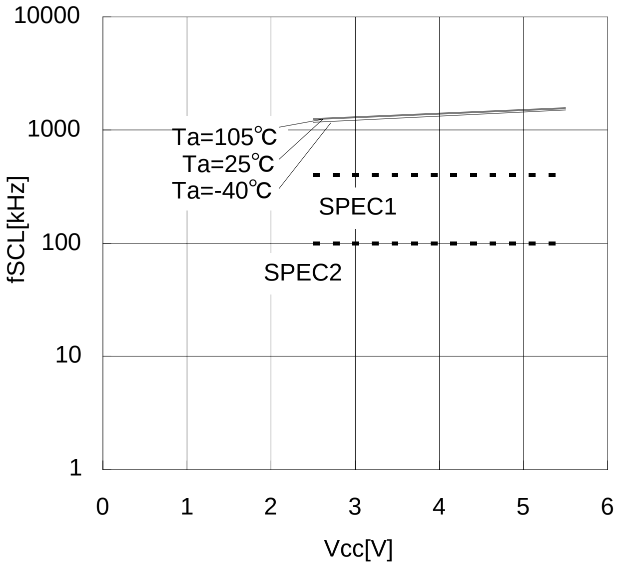


Figure 14. SCL frequency fSCL

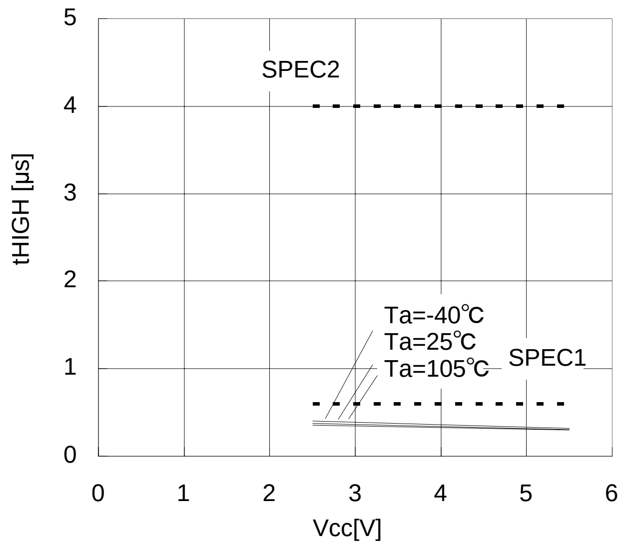


Figure 15. Data clock "H" time tHIGH

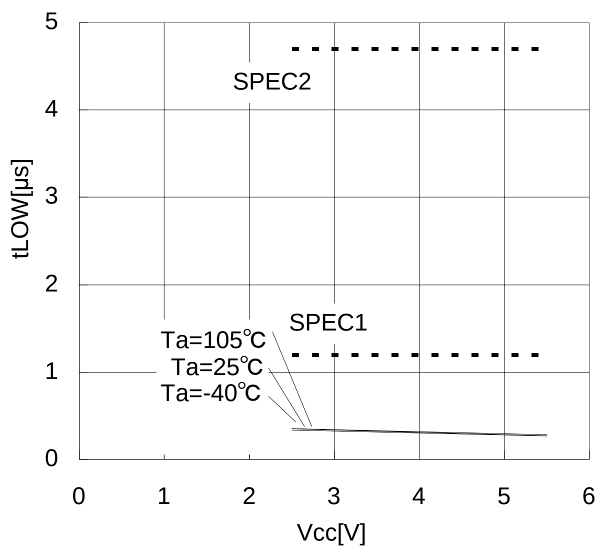


Figure 16. Data clock "L" time tLOW

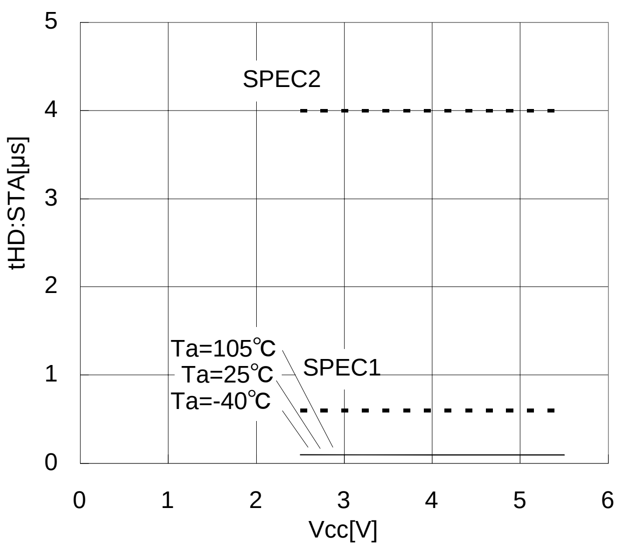


Figure 17. Start condition hold time tHD:STA

●**Typical Performance Curves - Continued**

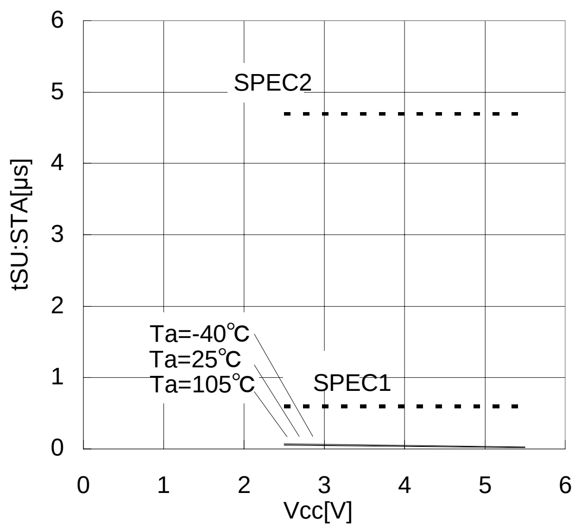


Figure 18. Start condition setup time tSU:STA

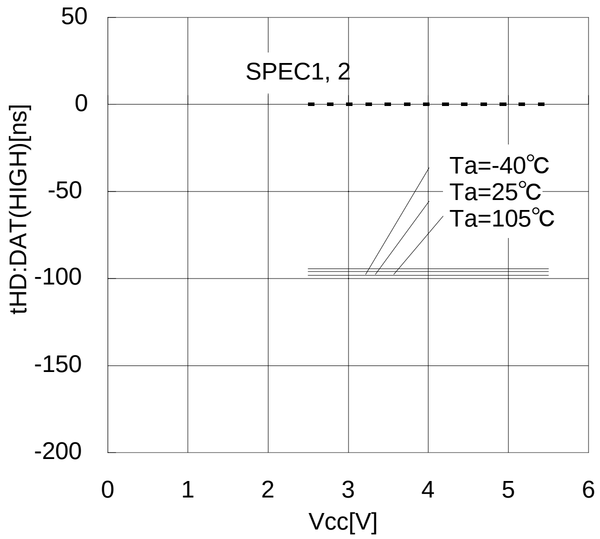


Figure 19. Input data hold time tHD:DAT(HIGH)

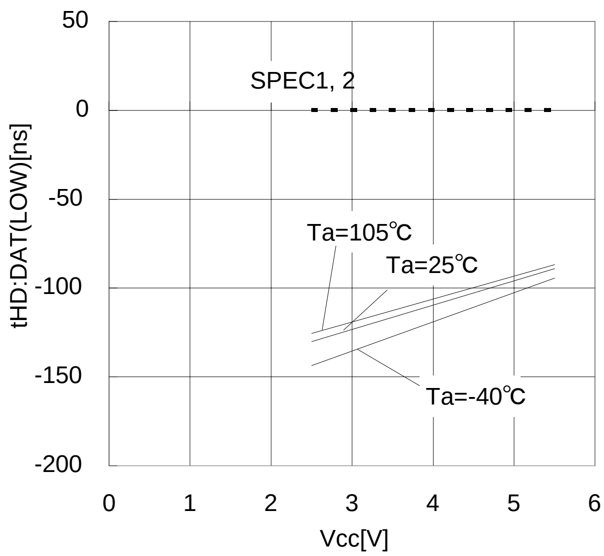


Figure 20. Input data hold time tHD:DAT(LOW)

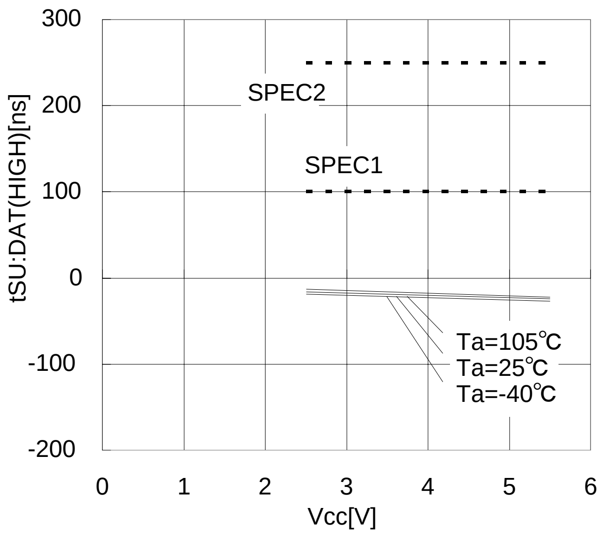


Figure 21. Input data setup time tSU:DAT(HIGH)

●**Typical Performance Curves - Continued**

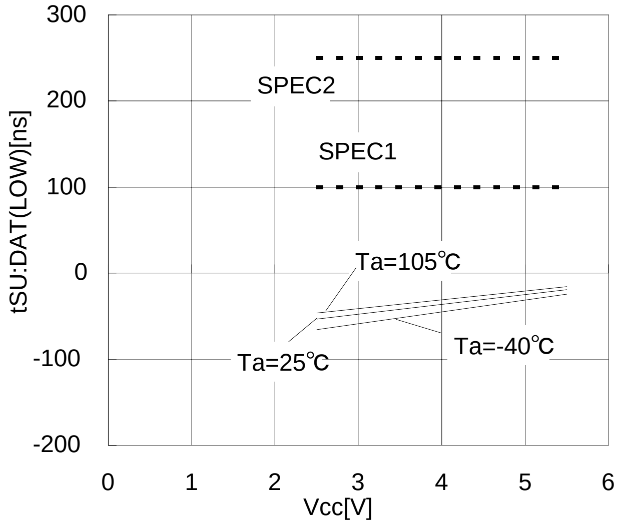


Figure 22. Input data setup time tSU:DAT(LOW)

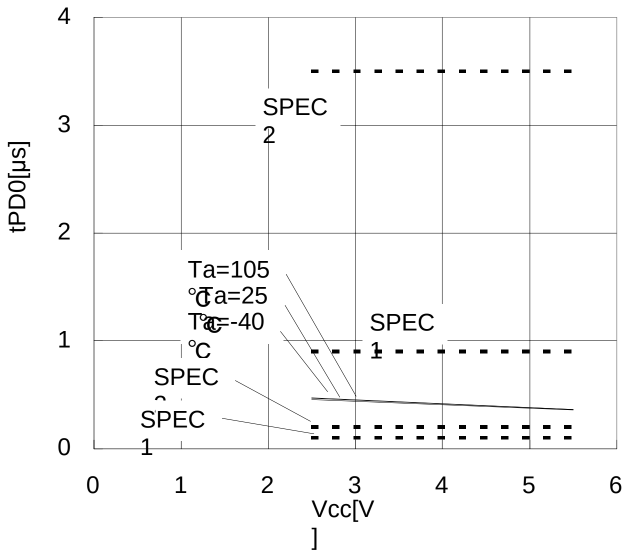


Figure 23. Output data delay time tPD0

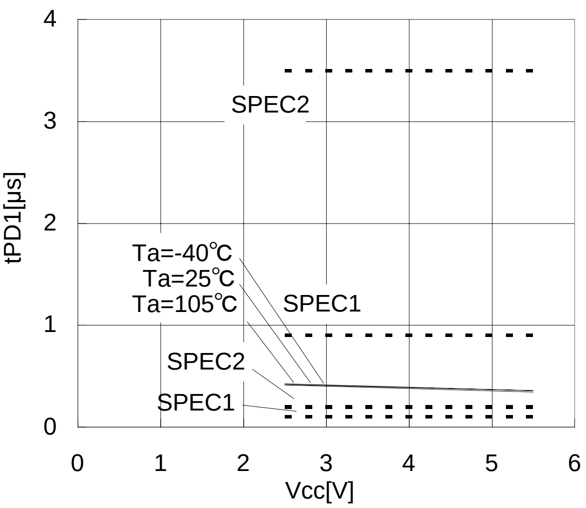


Figure 24. Output data delay time tPD1

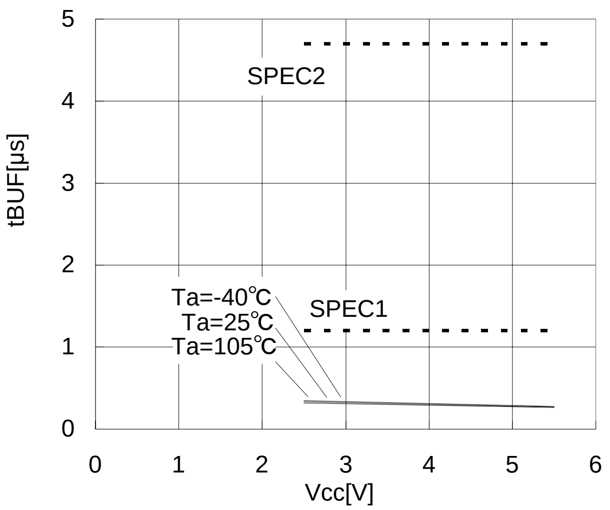


Figure 25. Bus release time before transfer start tBUF

●**Typical Performance Curves - Continued**

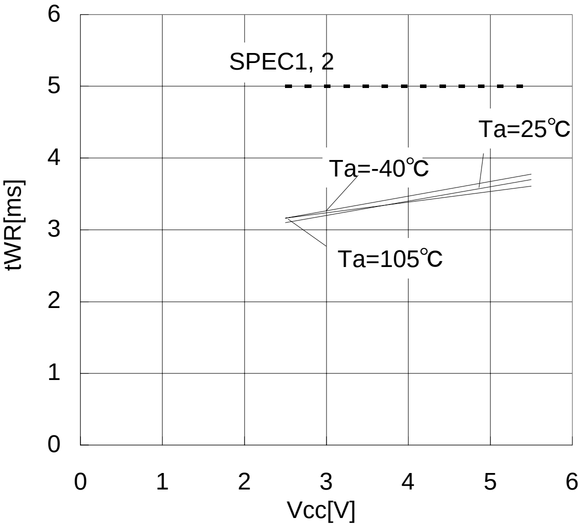


Figure 26. Internal write cycle time tWR

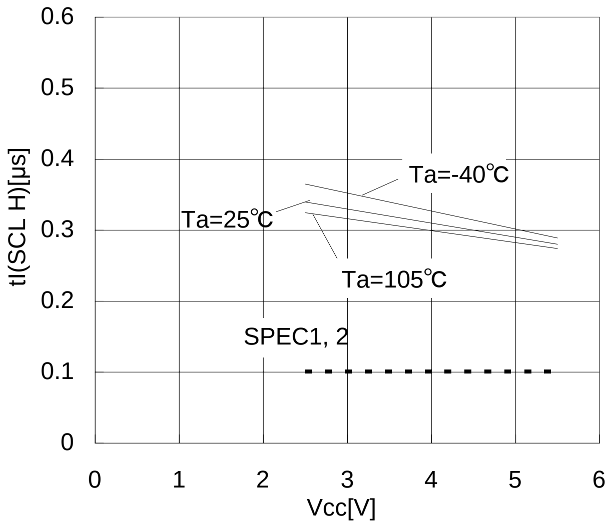


Figure 27. Noise removal valid time tI(SCL H)

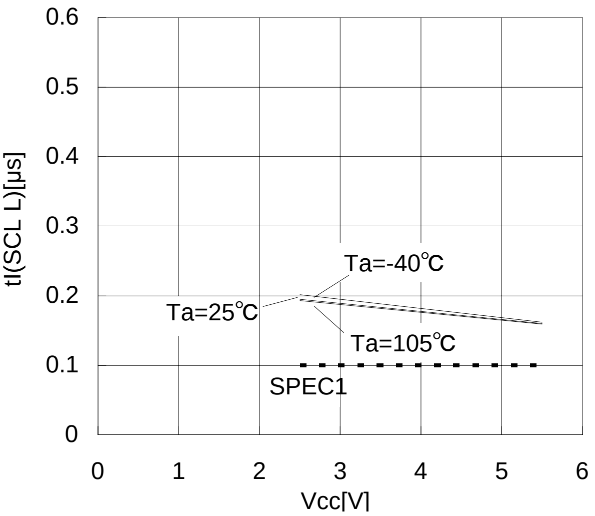


Figure 28. Noise removal valid time tI(SCL L)

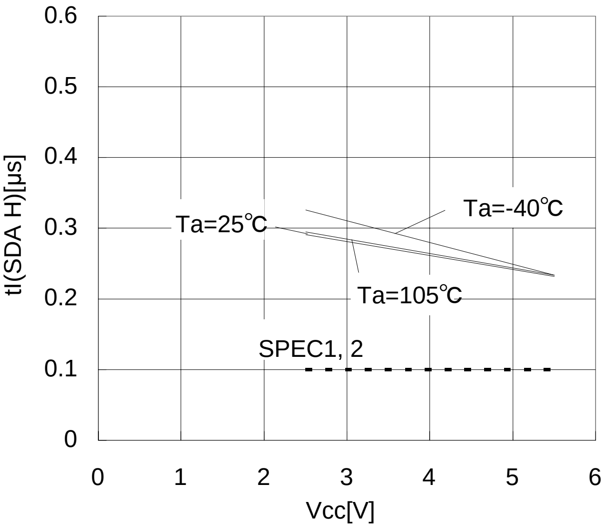


Figure 29. Noise removal valid time tI(SDA H)

●**Typical Performance Curves - Continued**

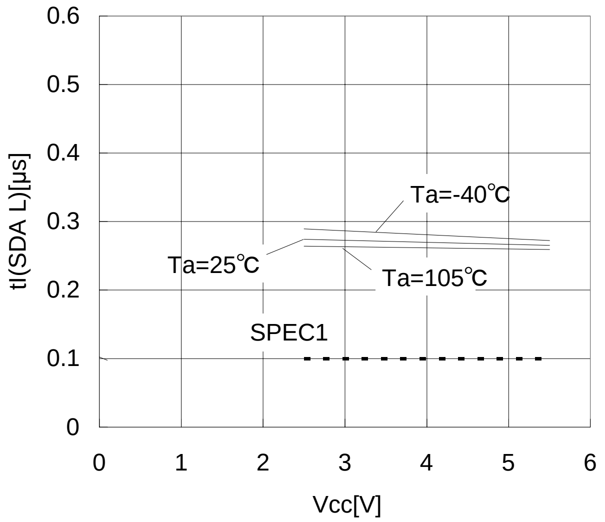


Figure 30. Noise removal valid time tI(SDA L)

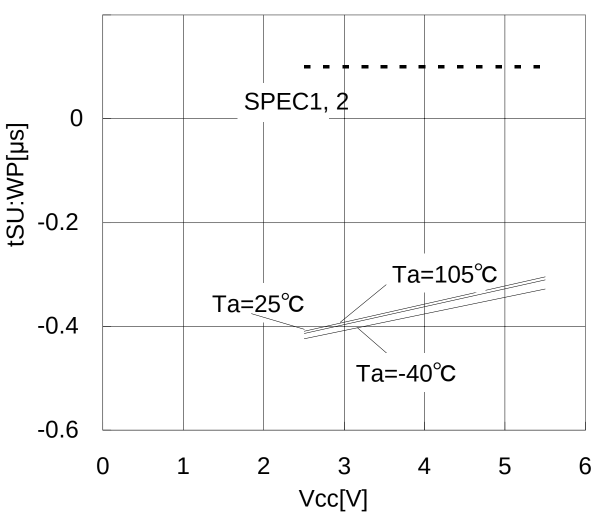


Figure 31. WP setup time　tSU:WP

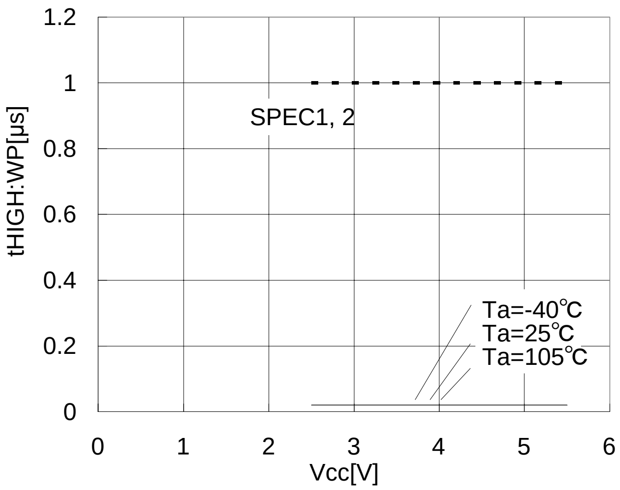


Figure 32. WP valid time　tHIGH:WP

●I²C BUS Communication

○I²C BUS data communication

I²C BUS data communication starts by start condition input, and ends by stop condition input. Data is always 8bit long, and acknowledge is always required after each byte. I²C BUS carries out data transmission with plural devices connected by 2 communication lines of serial data (SDA) and serial clock (SCL).

Among devices, there are “master” that generates clock and control communication start and end, and “slave” that is controlled by address peculiar to devices. EEPROM becomes “slave”. And the device that outputs data to bus during data communication is called “transmitter”, and the device that receives data is called “receiver”.

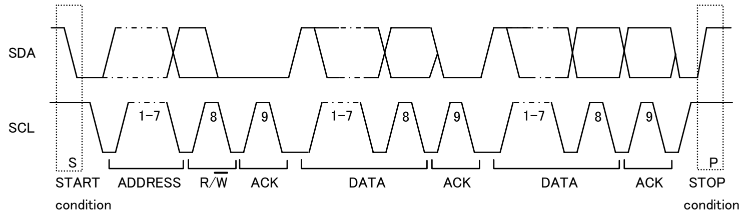


Figure 33. Data transfer timing

○Start condition (Start bit recognition)

- Before executing each command, start condition (start bit) where SDA goes from 'HIGH' down to 'LOW' when SCL is 'HIGH' is necessary.
- This IC always detects whether SDA and SCL are in start condition (start bit) or not, therefore, unless this confdition is satisfied, any command is executed.

○Stop condition (stop bit recongnition)

- Each command can be ended by SDA rising from 'LOW' to 'HIGH' when stop condition (stop bit), namely, SCL is 'HIGH'

○Acknowledge (ACK) signal

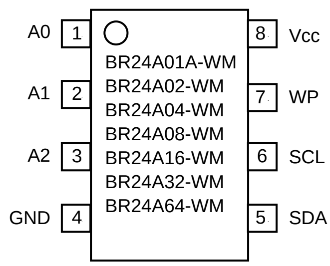
- This acknowledge (ACK) signal is a software rule to show whether data transfer has been made normally or not. In master and slave, the device (μ-COM at slave address input of write command, read command, and this IC at data output of readcommand) at the transmitter (sending) side releases the bus after output of 8bit data.
- The device (this IC at slave address input of write command, read command, and μ-COM at data output of read command) at the receiver (receiving) side sets SDA 'LOW' during 9 clock cycles, and outputs acknowledge signal (ACK signal) showing that it has received the 8bit data.
- This IC, after recognizing start condition and slave address (8bit), outputs acknowledge signal (ACK signal) 'LOW'.
- Each write operation outputs acknowledge signal (ACK signal) 'LOW', at receiving 8bit data (word address and write data).
- Each read operation outputs 8bit data (read data), and detects acknowledge signal (ACK signal) 'LOW'.
- When acknowledge signal (ACK signal) is detected, and stop condition is not sent from the master (μ-COM) side, this IC continues data output. When acknowledge signal (ACK signal) is not detected, this IC stops data transfer, and recognizes stop condition (stop bit), and ends read operation. And this IC gets in status.

○Device addressing

- Output slave address after start condition from master.
- The significant 4 bits of slave address are used for recognizing a device type. The device code of this IC is fixed to '1010'.
- Next slave addresses (A2 A1 A0 --- device address) are for selecting devices, and plural ones can be used on a same bus according to the number of device addresses.
- The most insignificant bit (R/$\overline{W}$ --- READ / $\overline{WRITE}$) of slave address is used for designating write or read operation, and is as shown below.

  Setting R / $\overline{W}$ to 0 ------- write (setting 0 to word address setting of random read)
  Setting R / $\overline{W}$ to 1 ------- read

Type	Slave address								Maximum number of connected buses
BR24A01A-WM	1	0	1	0	A2	A1	A0	R/$\overline{W}$	8
BR24A02-WM	1	0	1	0	A2	A1	A0	R/$\overline{W}$	8
BR24A04-WM	1	0	1	0	A2	A1	PS	R/$\overline{W}$	4
BR24A08-WM	1	0	1	0	A2	P1	P0	R/$\overline{W}$	2
BR24A16-WM	1	0	1	0	P2	P1	P0	R/$\overline{W}$	1
BR24A32-WM	1	0	1	0	A2	A1	A0	R/$\overline{W}$	8
BR24A64-WM	1	0	1	0	A2	A1	A0	R/$\overline{W}$	8



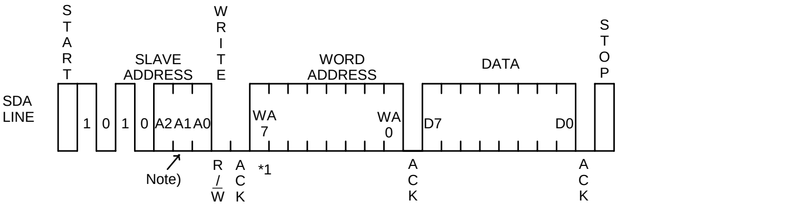
PS, P0 to P2 are page select bits.

Note) Up to 4 units BR24A04-WM, up to 2 units of BR24A08-WM, and one unit of BR24A16-WM can be connected.
Device address is set by 'H' and 'L' of each pin of A0, A1, and A2.

●Write Command

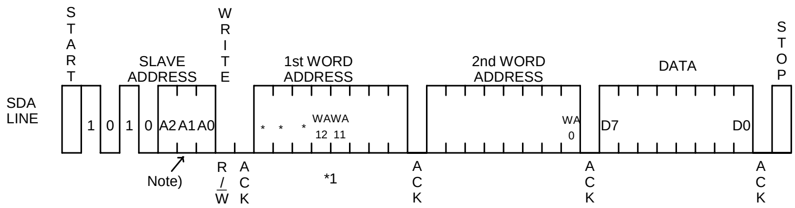
○Write cycle

・Arbitrary data is written to EEPROM. When to write only 1 byte, byte write is normally used, and when to write continuous data of 2 bytes or more, simultaneous write is possible by page write cycle. The maximum number of write bytes is specified per device of each capacity. Up to 32 arbitrary bytes can be written. (In the case of BR24A32 / A64-WM)



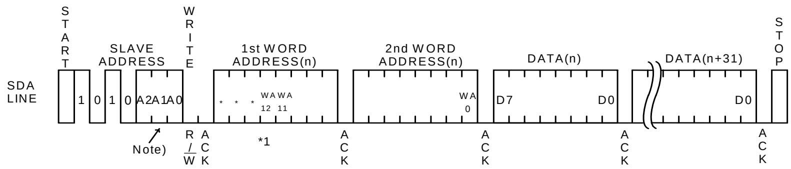
*1 As for WA7, BR24A01A-WM becomes Don’t care.

Figure 34. Byte write cycle (BR24A01A/02/04/08/16-WM)



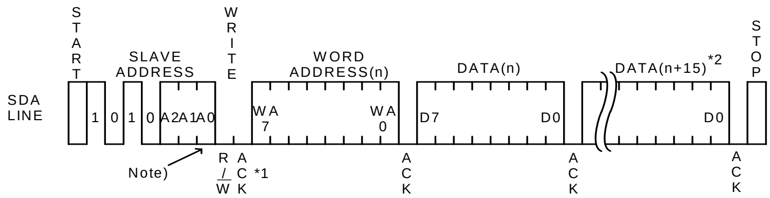
*1 As for WA12, BR24A32-WM becomes Don’t care.

Figure 35. Byte write cycle (BR24A32/64-WM)



*1 As for WA7, BR24A01A-WM becomes Don’t care.
*2 As for BR24A01A/02-WM become (n+7).

Figure 36. Page write cycle (BR24A01A/02/04/08/16-WM)



*1 As for WA12, BR24A32-WM becomes Don’t care.

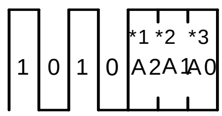
Figure 37. Page write cycle (BR24A32/64-WM)

・Data is written to the address designated by word address (n-th address)
・By issuing stop bit after 8bit data input, write to memory cell inside starts.
・When internal write is started, command is not accepted for tWR (5ms at maximum).
・By page write cycle, the following can be written in bulk : Up to 8 bytes (BR24A01A-WM, BR24A02-WM)
: Up to 16bytes (BR24A04-WM, BR24A08-WM,BR24A16-WM)
: Up to 32bytes (BR24A32-WM, BR24A64-WM

And when data of the maximum bytes or higher is sent, data from the first byte is overwritten.
(Refer to "Internal address increment" in Page 15.)

・As for page write cycle of BR24A01A-WM and BR24A02-WM, after the significant 5 bits (4 significant bits in BR24A01A-WM) of word address are designated arbitrarily, and as for page write command of BR24A04-WM, BR24A08-WM, and BR24A16-WM, after page select bit (PS) of slave address is designated arbitrarily, by continuing data input of 2 bytes or more, the address of insignificant 4 bits (insignificant 3 bit in BR24A01A-WM, and BR24A02-WM) is incremented internally, and data up to 16 bytes (up to 8 bytes in BR24A01A-WM and BR24A02-WM) can be written.
・As for page write cycle of BR24A32-WM and BR24A64-WM, after the significant 7 bits (in the case of BR24A32-WM) of word address, or the significant 8 bits (in the case of BR24A64-WM) of word address are designated arbitrarily, by continuing data input of 2 byte or more, the address of insignificant 5 bits is incremented internally, and data up to 32 bytes can be written.

Note)



*1 In BR24A16-WM, A2 becomes P2.
*2 In BR24A08-WM, BR24A16-WM, A1 become P1.
*3 In BR24A04-WM, A0 becomes PS, and in BR24A08-WM and

Figure 38. Difference of slave address of each

○Notes on write cycle continuous input

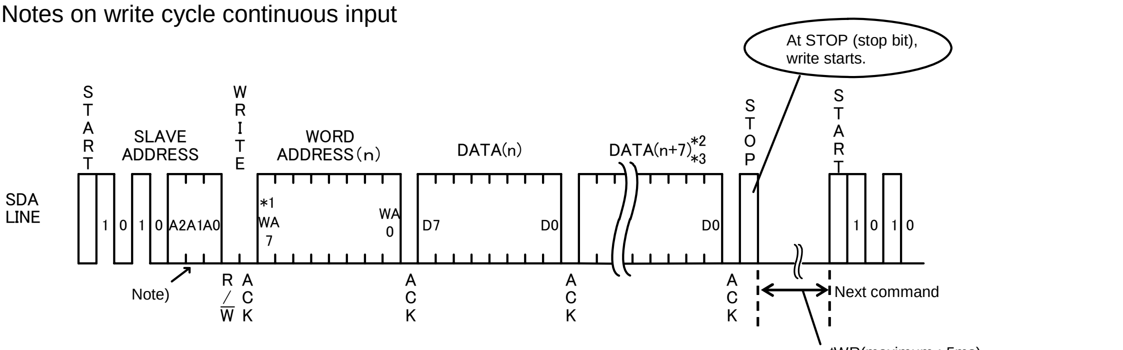


Figure 39. Page write cycle

*1 BR24A01A-WM becomes Don't care.
*2 BR24A04-WM, BR24A08-W, and BR24A16-WM become (n+15).
*3 BR24A32-WM and BR24A64-WM become (n+31).

Note)

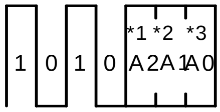


Figure 40. Difference of each type of slave address

*1 In BR24A16-WM, A2 becomes P2.
*2 In BR24A08-WM, BR24A16-WM, A1 become P1.
*3 In BR24A04-WM, A0 becomes PS, and in BR24A08-WM and in BR24A16-WM, A0 becomes P0.

○Notes on page write cycle

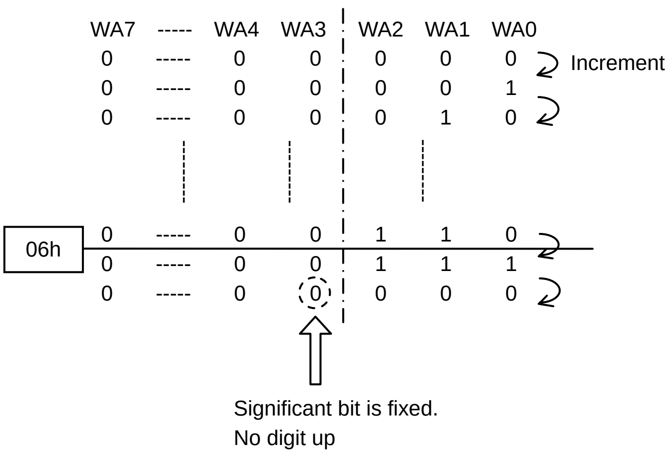
List of numbers of page write

Number of Pages	8Byte	16Byte	32Byte
Product number	BR24A01A-WM BR24A02-WM	BR24A04-WM BR24A08-WM BR24A16-WM	BR24A32-WM BR24A64-WM

The above numbers are maximum bytes for respective types.
Any bytes below these can be written.
In the case BR24A02-WM, 1 page=8bytes, but the page write cycle write time is 5ms at maximum for 8byte bulk write.
It does not stand 5ms at maximum × 8byte=40ms(Max.).

○Internal address increment

Page write mode (in the case of BR24A02-WM)



For example, when it is started from address 06h, therefore, increment is made as below,
06h → 07h → 00h → 01h ---, which please note.

*06h･･･06 in hexadecimal, therefore, 00000110 becomes a binary number.

○Write protect (WP) terminal

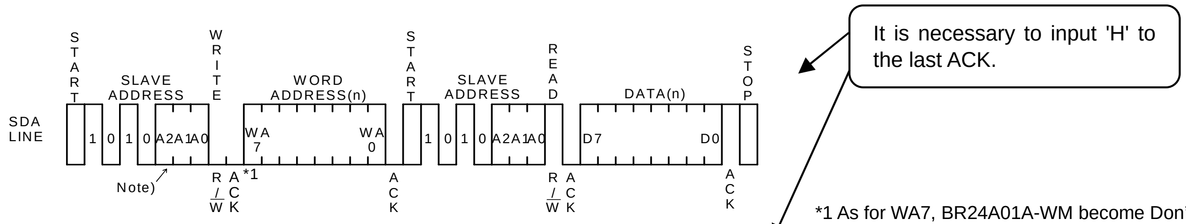
・Write protect (WP) function

When WP terminal is set V_{CC} (H level), data rewrite of all addresses is prohibited. When it is set GND (L level), data rewrite of all address is enabled. Be sure to connect this terminal to V_{CC} or GND, or control it to H level or L level. Do not use it open.
At extremely low voltage at power ON / OFF, by setting the WP terminal 'H', mistake write can be prevented.
During tWR, set the WP terminal always to 'L'. If it is set 'H', write is forcibly terminated.

●**Read Command**

○Read cycle

Data of EEPROM is read. In read cycle, there are random read cycle and current read cycle.
Random read cycle is a command to read data by designating address, and is used generally.
Current read cycle is a command to read data of internal address register without designating address, and is used when to verify just after write cycle. In both the read cycles, sequential read cycle is available, and the next address data can be read in succession.



*1 As for WA7, BR24A01A-WM become Don't care.

Figure 41. Random read cycle (BR24A01A/02/04/08/16-WM)

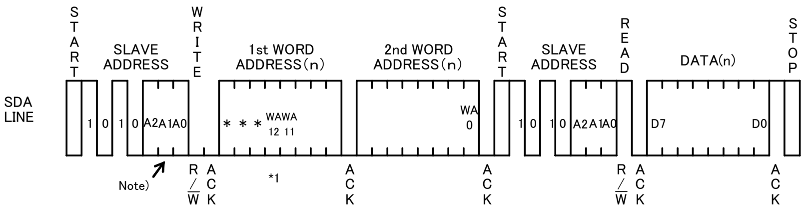


Figure 42. Random read cycle (BR24A32/64 -WM)

*1 As for WA12, BR24A32-WM become Don't care.

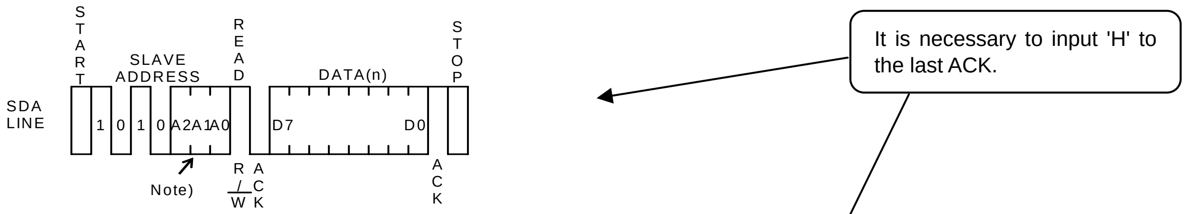


Figure 43. Current read cycle

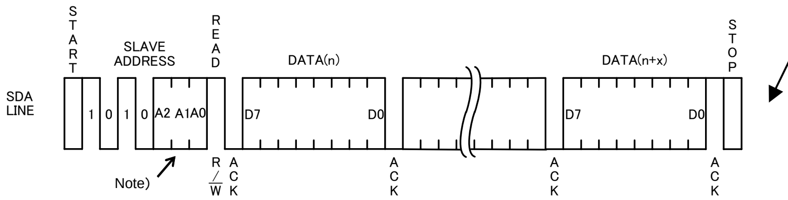


Figure 44. Sequential read cycle (in the case of current read cycle)

- In random read cycle, data of designated word address can be read.
- When the command just before current read cycle is random read cycle, current read cycle (each including sequential read cycle), data of incremented last read address (n)-th address, i.e., data of the (n+1)-th address is output.
- When ACK signal 'LOW' after D0 is detected, and stop condition is not sent from master (μ-COM) side, the next address data can be read in succession.
- Read cycle is ended by stop condition where 'H' is input to ACK signal after D0 and SDA signal is started at SCL signal 'H' .
- When 'H' is not input to ACK signal after D0, sequential read gets in, and the next data is output.
  Therefore, read command cycle cannot be ended. When to end read command cycle, be sure input stop condition to input 'H' to ACK signal after D0, and to start SDA at SCL signal 'H'.
- Sequential read is ended by stop condition where 'H' is input to ACK signal after arbitrary D0 and SDA is started at SCL signal 'H'.

Note)

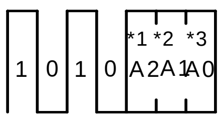


Figure 45. Difference of slave address of each type

*1 In BR24A16-WM, A2 becomes P2.
*2 In BR24A08-WM, BR24A16-WM, A1 become P1.
*3 In BR24A04-WM, A0 becomes PS, and in BR24A08-WM and BR24A16-WM, A0 becomes P0.

●Software reset

Software reset is executed when to avoid malfunction after power on, and to reset during command input. Software reset has several kinds, and 3 kinds of them are shown in the figure below. (Refer to Figure 46(a), Figure 46(b), and Figure 46(c).) In dummy clock input area, release the SDA bus ('H' by pull up). In dummy clock area, ACK output and read data '0' (both 'L' level) may be output from EEPROM, therefore, if 'H' is input forcibly, output may conflict and over current may flow, leading to instantaneous power failure of system power source or influence upon devices.

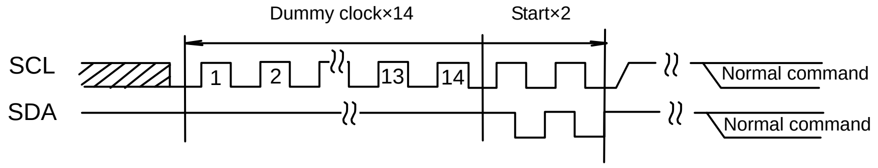


Figure 46-(a) The case of dummy clock +START+START+ command input

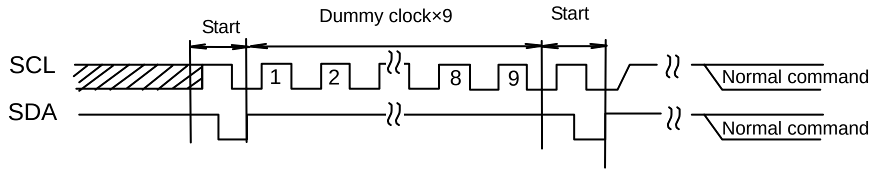


Figure 46-(b) The case of START +9 dummy clocks +START+ command input

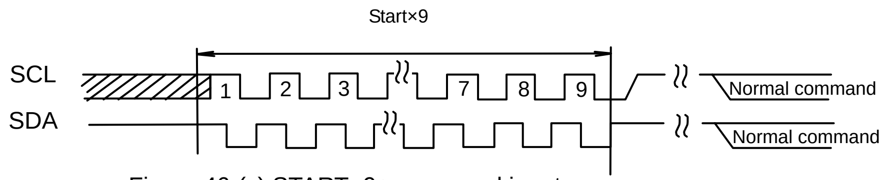


Figure 46-(c) START×9+ command input

※ Start command from START input.

●Acknowledge polling

During internal write execution, all input commands are ignored, therefore ACK is not sent back. During internal automatic write execution after write cycle input, next command (slave address) is sent, and if the first ACK signal sends back 'L', then it means end of write operation, while if it sends back 'H', it means now in writing. By use of acknowledge polling, next command can be executed without waiting for tWR = 5ms.
When to write continuously, $R/\overline{W}$ = 0, when to carry out current read cycle after write, slave address $R/\overline{W}$ = 1 is sent, and if ACK signal sends back 'L', then execute word address input and data output and so forth.

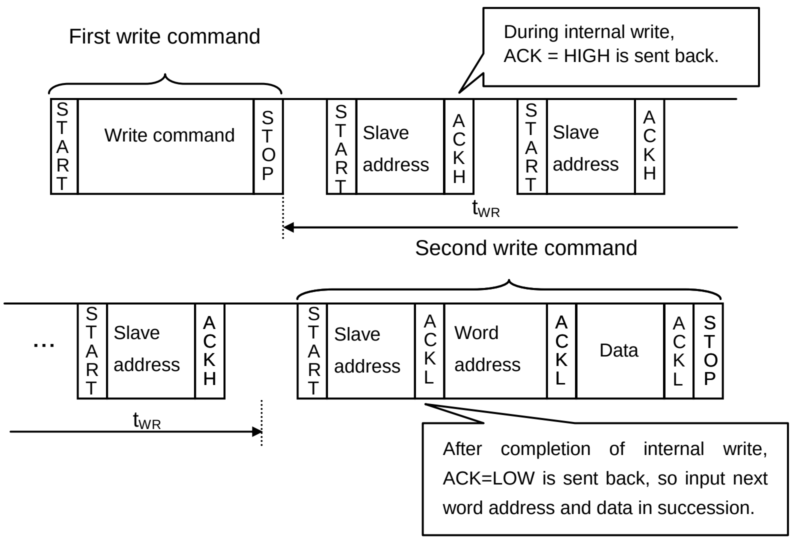


Figure 47. Case to continuously write by acknowledge polling

●**WP valid timing (write cancel)**

WP is usually fixed to 'H' or 'L', but when WP is used to cancel write cycle and so forth, pay attention to the following WP valid timing. During write cycle execution, in cancel valid area, by setting WP='H', write cycle can be cancelled. In both byte write cycle and page write cycle, the area from the first start condition of command to the rise of clock to taken in D0 of data(in page write cycle, the first byte data) is cancel invalid area.

WP input in this area becomes Don't care. Set the setup time to rise of D0 taken SCL 100ns or more. The area from the rise of SCL to take in D0 to the end of internal automatic write (tWR) is cancel valid area. And, when it is set WP='H' during tWR, write is ended forcibly, data of address under access is not guaranteed, therefore, write it once again. (Refer to Figure 48.)

After execution of forced end by WP, standby status gets in, so there is no need to wait for tWR (5ms at maximum).

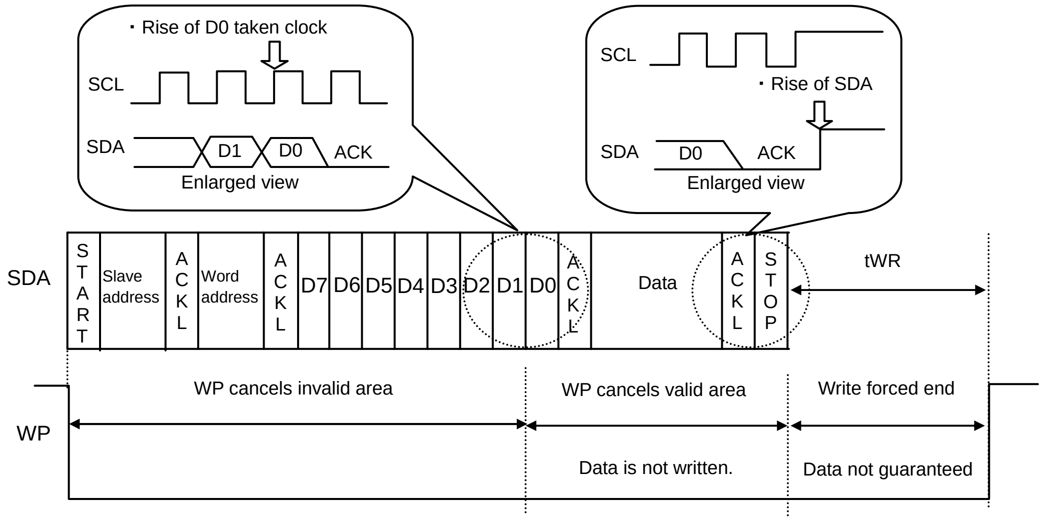


Figure 48. WP valid timing

●**Command cancel by start condition and stop condition**

During command input, by continuously inputting start condition and stop condition, command can be cancelled. (Refer to Figure 49.)

However, in ACK output area and during data read, SDA bus may output 'L', and in this case, start condition and stop condition cannot be input, so reset is not available. Therefore, execute software reset. And when command is cancelled by start, stop condition, during random read cycle, sequential read cycle, or current read cycle, internal setting address is not determined, therefore, it is not possible to carry out current read cycle in succession. When to carry out read cycle in succession, carry out random read cycle.

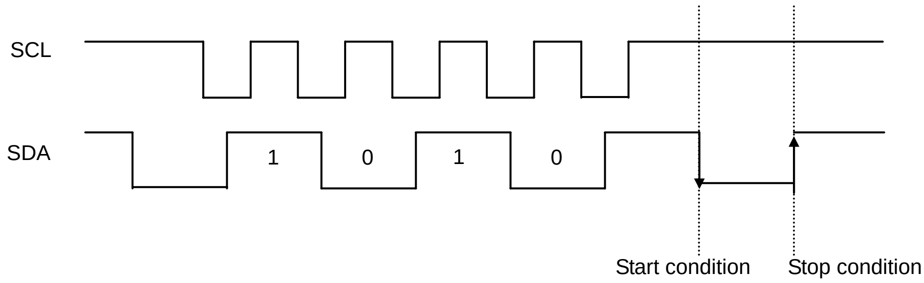


Figure 49. Case of cancel by start, stop condition during slave address input

●I/O peripheral circuit

○Pull up resistance of SDA terminal

SDA is NMOS open drain, so requires pull up resistance. As for this resistance value (R_{PU}), select an appropriate value to this resistance value from microcontroller V_{IL}, I_L, and V_{OL}-I_{OL} characteristics of this IC. If R_{PU} is large, operating frequency is limited. The smaller the R_{PU}, the larger the consumption current at operation.

○Maximum value of R_{PU}

The maximum value of R_{PU} is determined by the following factors.

(1)SDA rise time to be determined by the capacitance (CBUS) of bus line of R_{PU} and SDA should be tR or below. And AC timing should be satisfied even when SDA rise time is late.

(2)The bus electric potential A to be determined by input leak total (I_L) of device connected to bus at output of 'H' to SDA bus and RPU should sufficiently secure the input 'H' level (VIH) of microcontroller and EEPROM including recommended noise margin 0.2 V_{CC}.

$$V_{cc} - I_L R_{PU} - 0.2V_{cc} \geqq V_{IH}$$

$$\therefore \quad R_{PU} = \frac{0.8V_{cc} - V_{IH}}{I_L}$$

Ex.) When V_{CC} =3V, I_L=10µA, V_{IH}=0.7 V_{CC},
from (2)

$$R_{PU} \leqq \frac{0.8\times3 - 0.7\times3}{10\times10^{-6}}$$

$$\leqq 300\ [\mathrm{k}\Omega]$$

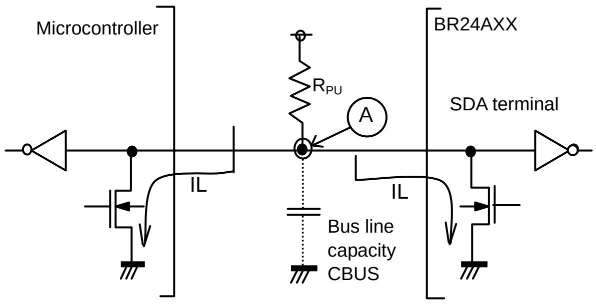


Figure 50. I/O circuit diagram

○Minimum value of R_{PU}

The minimum value of R_{PU} is determined by the following factors.

(1)When IC outputs LOW, it should be satisfied that V_{OLMAX}=0.4V and I_{OLMAX}=3mA.

$$\frac{V_{CC}-V_{OL}}{R_{PU}} \leqq I_{OL} \qquad \therefore \quad R_{PU} \leqq \frac{V_C - V_{OL}}{I_{OL}}$$

(2)V_{OLMAX}=0.4V should secure the input 'L' level (V_{IL}) of microcontroller and EEPROM including recommended noise margin 0.1 V_{CC}.

$V_{OLMAX} \leqq V_{IL} - 0.1\ V_{CC}$

Ex.) When V_{CC} =3V, VOL=0.4V, IOL=3mA, microcontroller, EEPROM VIL=0.3 V_{CC}
from (1)

$$R_{PU} \geqq \frac{3-0.4}{3\times10^{-3}}$$

$$\geqq 867\ [\Omega]$$

And

$$V_{OL} = 0.4\ [V]$$

$$V_{IL} = 0.3\times3 = 0.9\ [V]$$

Therefore, the condition (2) is satisfied.

○Pull up resistance of SCL terminal

When SCL control is made at CMOS output port, there is no need, but in the case there is timing where SCL becomes 'Hi-Z', add a pull up resistance. As for the pull up resistance, one of several kΩ to several ten kΩ is recommended in consideration of drive performance of output port of microcontroller.

●A0, A1, A2, WP process

○Process of device address terminals (A0,A1,A2)

Check whether the set device address coincides with device address input sent from the master side or not, and select one among plural devices connected to a same bus. Connect this terminal to pull up or pull down, or V_{CC} or GND. And, pins (N, C, PIN) not used as device address may be set to any of 'H', 'L', and 'Hi-Z'.

Types with N.C.PIN	BR24A16/F/FJ -WM	A0, A1, A2
	BR24A08/F/FJ-WM	A0, A1
	BR24A04/F/FJ -WM	A0

○Process of WP terminal

WP terminal is the terminal that prohibits and permits write in hardware manner. In 'H' status, only READ is available and WRITE of all address is prohibited. In the case of 'L', both are available. In the case of use it as an ROM, it is recommended to connect it to pull up or V_{CC}. In the case to use both READ and WRITE, control WP terminal or connect it to pull down or GND.

●Cautions on microcontroller connection

○Rs

In I²C BUS, it is recommended that SDA port is of open drain input/output. However, when to use CMOS input / output of tri state to SDA port, insert a series resistance Rs between the pull up resistance Rpu and the SDA terminal of EEPROM. This is controls over current that occurs when PMOS of the microcontroller and NMOS of EEPROM are turned ON simultaneously. Rs also plays the role of protection of SDA terminal against surge. Therefore, even when SDA port is open drain input/output, Rs can be used.

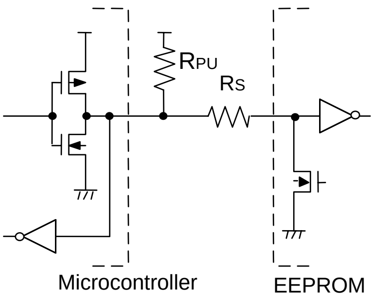


Figure 51. I/O circuit diagram

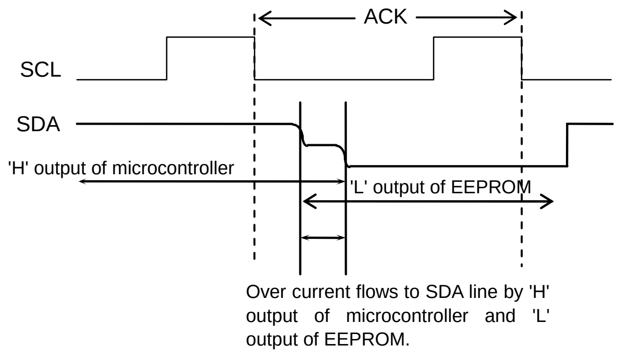


Figure 52. Input / output collision timing

○Maximum value of Rs

The maximum value of Rs is determined by the following relations.

(1)SDA rise time to be determined by the capacity (CBUS) of bus line of Rpu and SDA should be tR or below. And AC timing should be satisfied even when SDA rise time is late.

(2)The bus electric potential Ⓐ to be determined by Rpu and Rs the moment when EEPROM outputs 'L' to SDA bus should sufficiently secure the input 'L' level (V_{IL}) of microcontroller including recommended noise margin 0.1 V_{CC}.

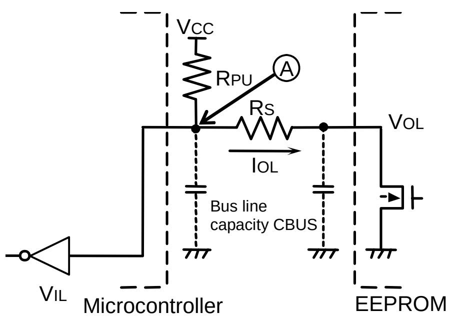


Figure 53. I/O circuit diagram

$$\frac{(V_{CC}-V_{OL})\times R_S}{R_{PU}+R_S} + V_{OL}+0.1V_{CC} \leqq V_{IL}$$

$$\therefore \quad R_S \leqq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

Example) When V_{CC}=3V, V_{IL}=0.3V_{CC}, V_{OL}=0.4V, R_{PU}=20kΩ,

$$\text{from(2),} \quad R_S \leqq \frac{0.3\times 3-0.4-0.1\times 3}{1.1\times 3-0.3\times 3} \times 20\times 10^3$$

$$\leqq 1.67[k\Omega]$$

○Minimum value of Rs

The minimum value of Rs is determined by over current at bus collision. When over current flows, noises in power source line, and instantaneous power failure of power source may occur. When allowable over current is defined as I, the following relation must be satisfied. Determine the allowable current in consideration of impedance of power source line in set and so forth. Set the over current to EEPROM 10mA or below.

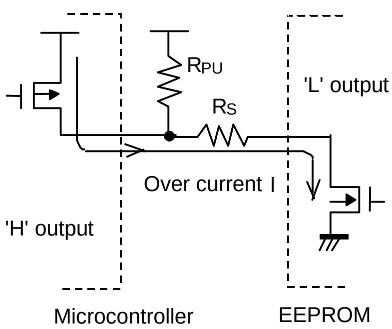


Figure 54. I/O circuit diagram

$$\frac{V_{CC}}{R_S} \leqq I$$

$$\therefore \quad R_S \geqq \frac{V_{CC}}{I}$$

Example) When V_{CC}=3V, I=10mA

$$R_S \geqq \frac{3}{10\times 10^{-3}}$$

$$\geqq 300[\Omega]$$

● I^2C BUS input / output circuit

○Input (A0,A2,SCL)

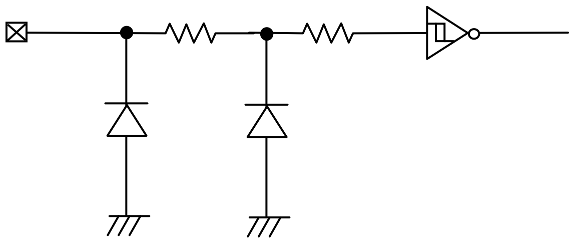


Figure 55. Input pin circuit diagram

○Input / output (SDA)

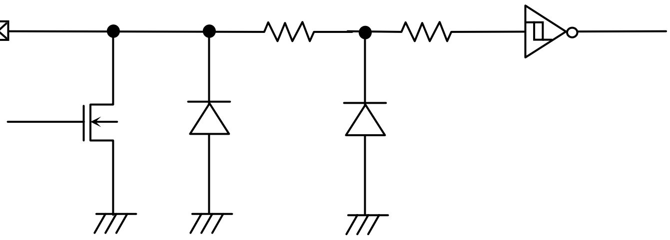


Figure 56. Input / output pin circuit diagram

○Input (A1, WP)

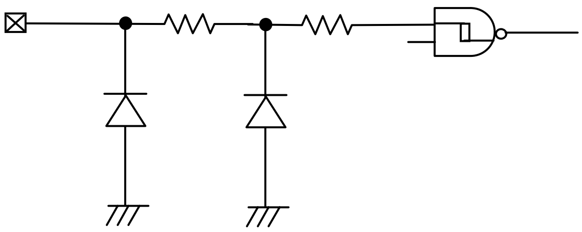


Figure 57. Input pin circuit diagram

● **Notes on power ON**

At power on, in IC internal circuit and set, V_{CC} rises through unstable low voltage area, and IC inside is not completely reset, and malfunction may occur. To prevent this, functions of POR circuit and LVCC circuit are equipped. To assure the operation, observe the following conditions at power on.

1. Set SDA = 'H' and SCL ='L' or 'H'
2. Start power source so as to satisfy the recommended conditions of t_R, t_{OFF}, and Vbot for operating POR circuit.

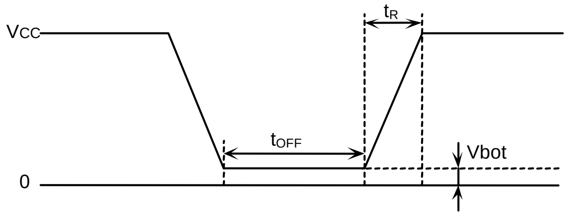


Figure 58. Rise waveform diagram

Recommended conditions of t_R, t_{OFF},Vbot

t_R	t_{OFF}	Vbot
10ms or below	10ms or longer	0.3V or below
100ms or below	10ms or longer	0.2V or below

3. Set SDA and SCL so as not to become 'Hi-Z'.
When the above conditions 1 and 2 cannot be observed, take the following countermeasures.
a) In the case when the above condition 1 cannot be observed. When SDA becomes 'L' at power on.
→Control SCL and SDA as shown below, to make SCL and SDA, 'H' and 'H'.

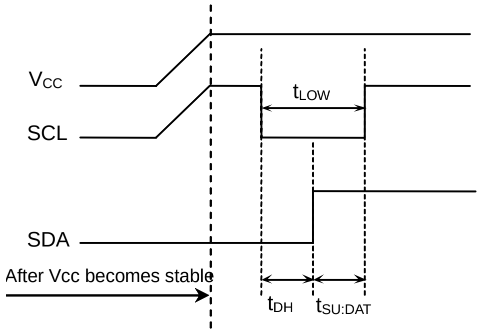


Figure 59. When SCL= 'H' and SDA= 'L'

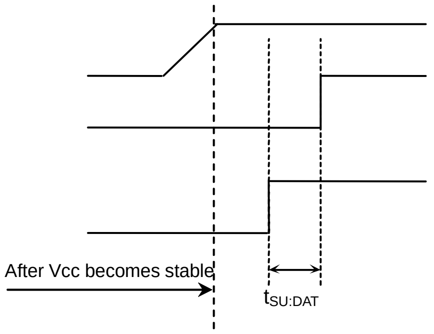


Figure 60. When SCL='L' and SDA='L'

b) In the case when the above condition 2 cannot be observed.
→After power source becomes stable, execute software reset(Page 17).

c) In the case when the above conditions 1 and 2 cannot be observed.
→Carry out a), and then carry out b).

●**Low voltage malfunction prevention function**

LVCC circuit prevents data rewrite operation at low power, and prevents wrong write. At LVCC voltage (Typ. =1.2V) or below, it prevent data rewrite.

●**V_{CC} noise countermeasures**

○Bypass capacitor

When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a by pass capacitor (0.1µF) between IC V_{CC} and GND. At that moment, attach it as close to IC as possible. And, it is also recommended to attach a bypass capacitor between board V_{CC} and GND.

●**Note of use**

(1) Described numeric values and data are design representative values, and the values are not guaranteed.

(2) We believe that application circuit examples are recommendable, however, in actual use, confirm characteristics further sufficiently. In the case of use by changing the fixed number of external parts, make your decision with sufficient margin in consideration of static characteristics and transition characteristics and fluctuations of external parts and our LSI.

(3) Absolute maximum ratings
If the absolute maximum ratings such as impressed voltage and operation temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(4)GND electric potential
Set the voltage of GND terminal lowest at any operating condition. Make sure that each terminal voltage is lower than that of GND terminal.

(5)Terminal design
In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.

(6)Terminal to terminal shortcircuit and wrong packaging
When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(7) Use in a strong electromagnetic field may cause malfunction, therefore, evaluate design sufficiently.

●Ordering Information

Product Code Description

B R 2 4 A x x x x x - WM x x

BUS type
24: I^2C

Operating temperature
-40℃ to +105℃

Capacity

01A=1K 08=8K 64=64K
02=2K 16=16K
04=4K 32=32K

Package

F : SOP8
FJ : SOP-J8
FVM : MSOP8

Double Cell

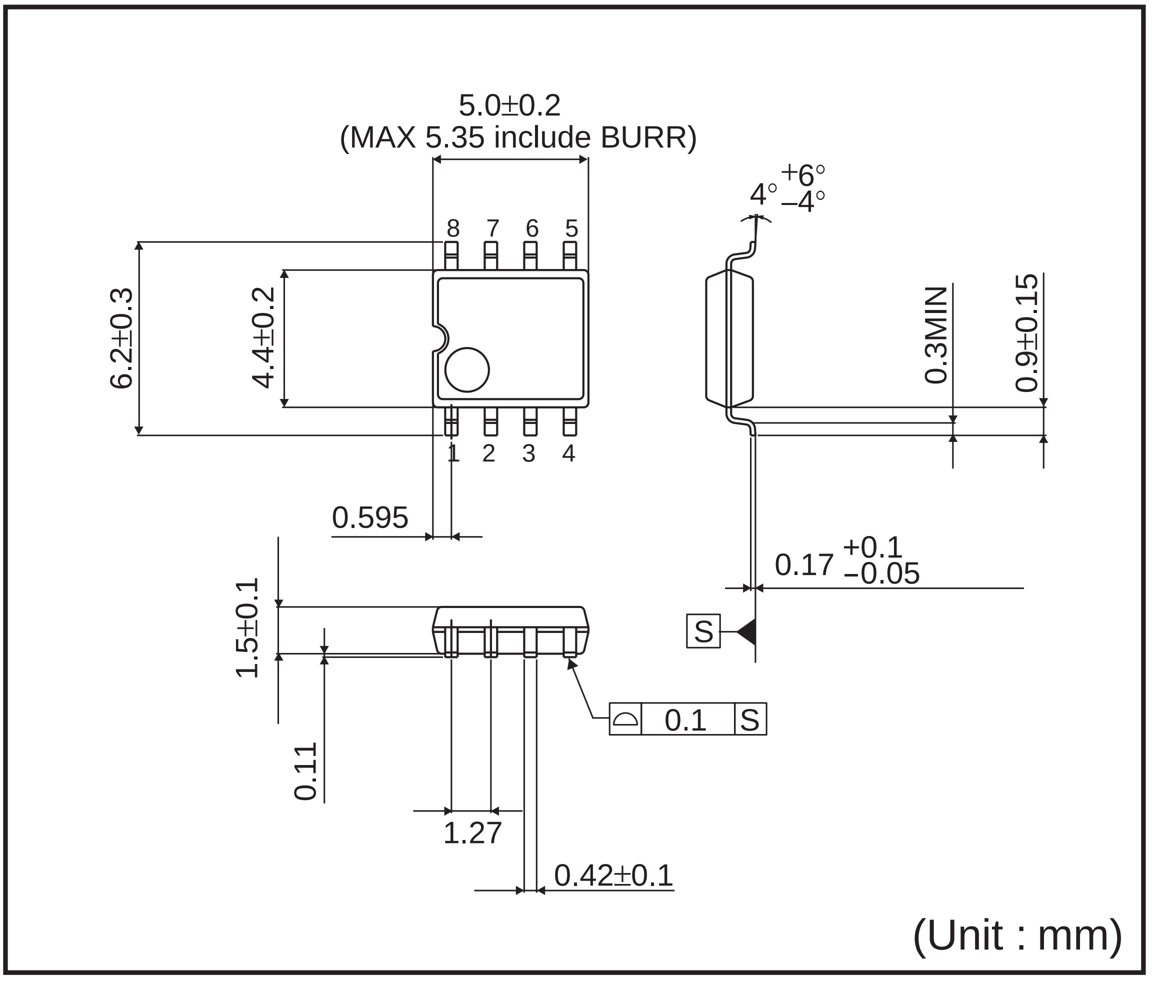
Packaging and forming specification
E2 : Embossed tape and reel (SOP8,SOP-J8)
TR : Embossed tape and reel (MSOP8)

●Lineup

Capacity	Package	
	Type	Quantity
1K	SOP8	Reel of 2500
	SOP-J8	Reel of 2500
2K	SOP8	Reel of 2500
	SOP-J8	Reel of 2500
	MSOP8	Reel of 3000
4K	SOP8	Reel of 2500
	SOP-J8	Reel of 2500
8K	SOP8	Reel of 2500
	SOP-J8	Reel of 2500
16K	SOP8	Reel of 2500
	SOP-J8	Reel of 2500
32K	SOP8	Reel of 2500
64K	SOP8	Reel of 2500

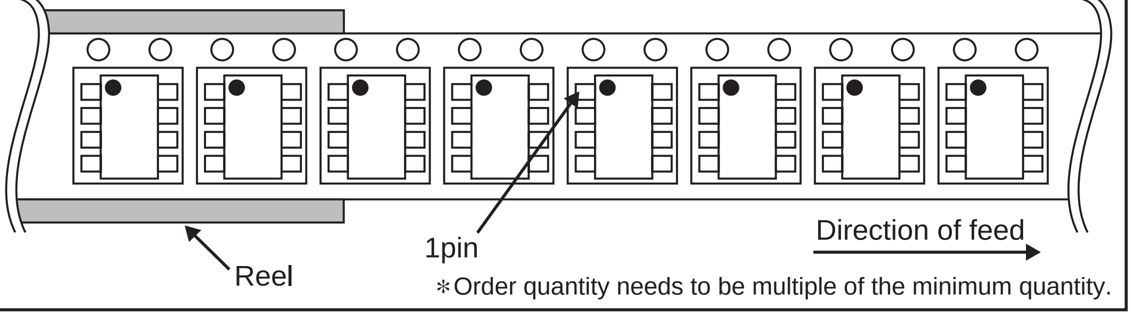
●**Physical Dimension Tape and Reel Information**

SOP8



<Tape and Reel information>

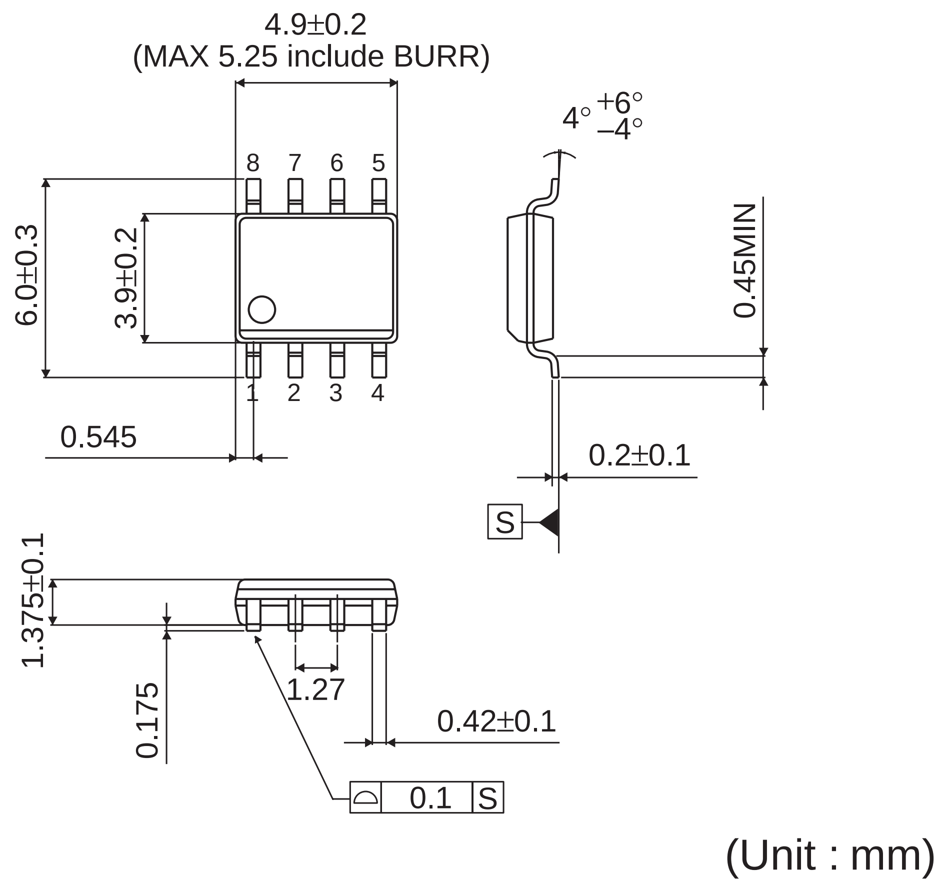
Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



*Order quantity needs to be multiple of the minimum quantity.

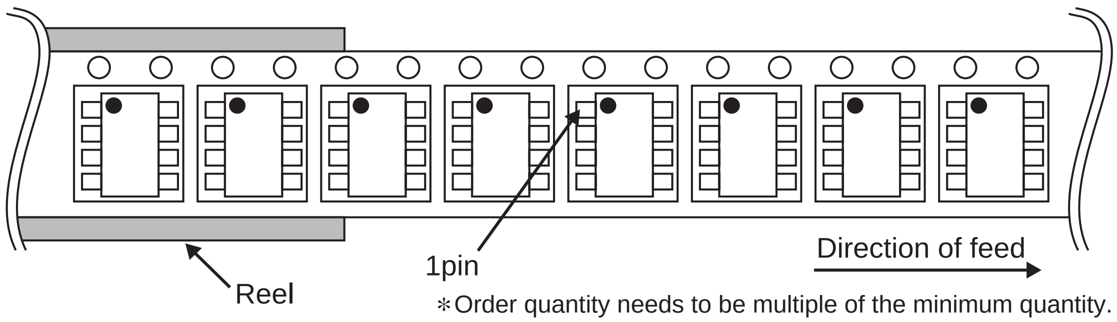
●Physical Dimension Tape and Reel Information - Continued

SOP-J8



<Tape and Reel information>

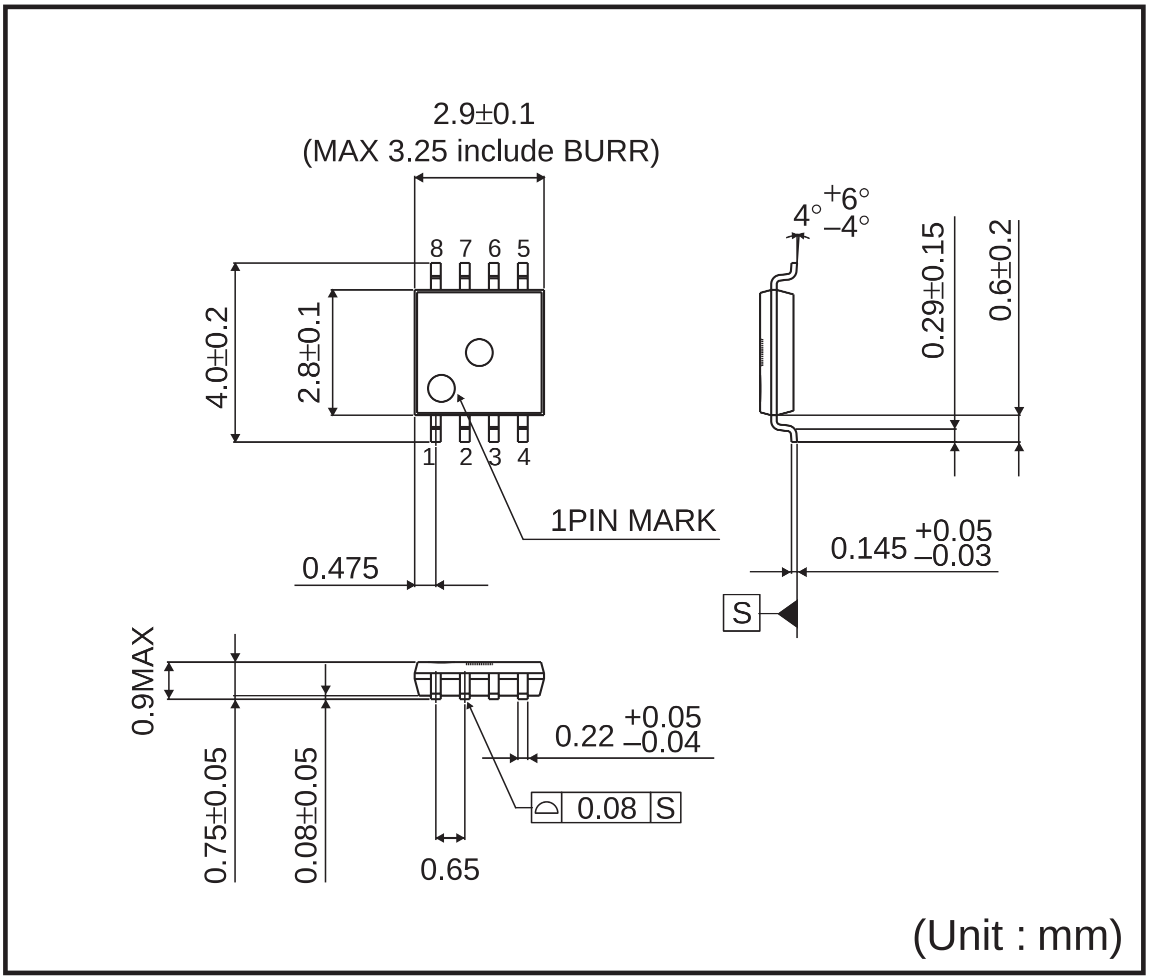
Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

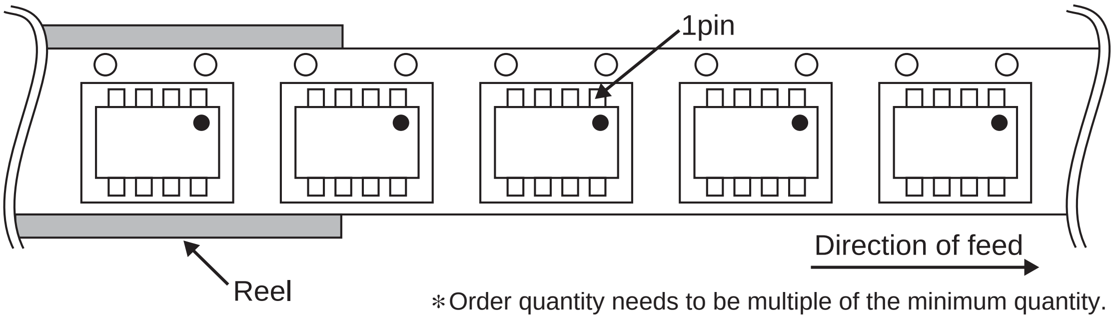
●Physical Dimension Tape and Reel Information - Continued

MSOP8



<Tape and Reel information>

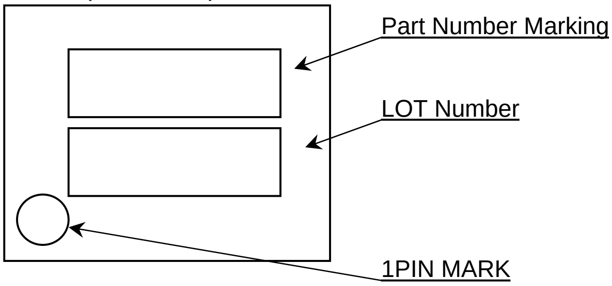
Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



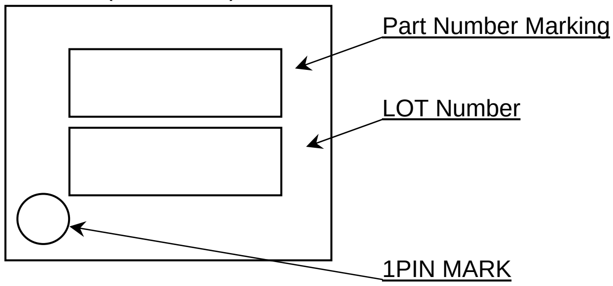
∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagrams

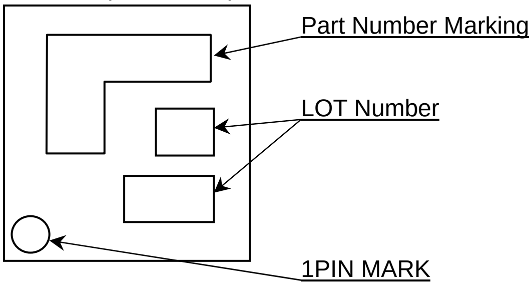
SOP8(TOP VIEW)



SOP-J8(TOP VIEW)



MSOP8(TOP VIEW)



●Marking Information

Capacity	Product Name Marking	Package Type
1K	A01A	SOP8
		SOP-J8
2K	A02	SOP8
		SOP-J8
		MSOP8
4K	A04	SOP8
		SOP-J8
8K	A08	SOP8
		SOP-J8
16K	A16	SOP8
		SOP-J8
32K	A32	SOP8
64K	A64	SOP8

●**Revision History**

Date	Revision	Changes
31.Aug.2012	001	New Release

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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