



**Frequency Generator & Integrated Buffers for Celeron & PII/III™**

**Recommended Application:**

BX, Appollo Pro 133 type of chip set.

**Output Features:**

- 3 - CPUs @2.5V, up to 150MHz.
- 17 - SDRAM @ 3.3V, up to 150MHz.
- 7 - PCI @3.3V
- 2 - IOAPIC @ 2.5V
- 1 - 48MHz, @3.3V fixed.
- 1 - 24MHz @ 3.3V
- 2 - REF @3.3V, 14.318MHz.

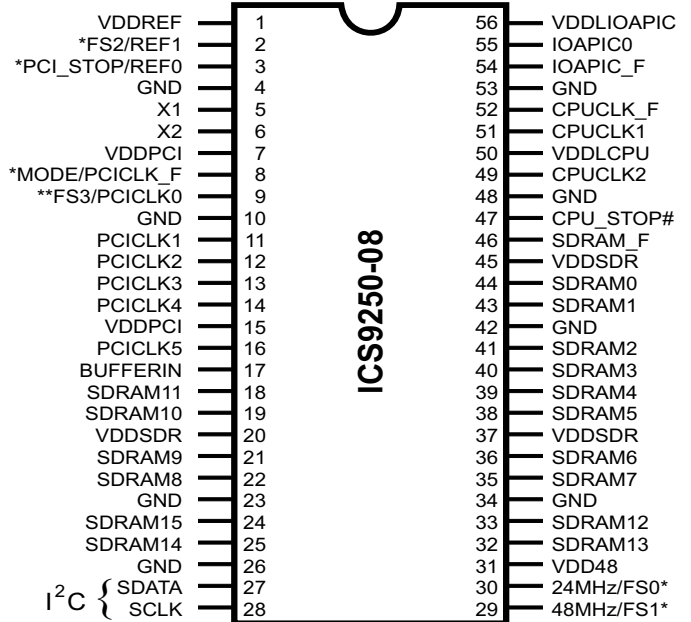
**Features:**

- Up to 150MHz frequency support
- Support power management: CPU, PCI, stop and Power down Mode form I<sup>2</sup>C programming.
- Spread spectrum for EMI control (0 to -0.5%, ± 0.25%).
- Uses external 14.318MHz crystal

**Key Specifications:**

- CPU – CPU: <175ps
- CPU – PCI: min = 1ns max = 4ns
- PCI – PCI: <250ps
- SDRAM - SDRAM: <500ps

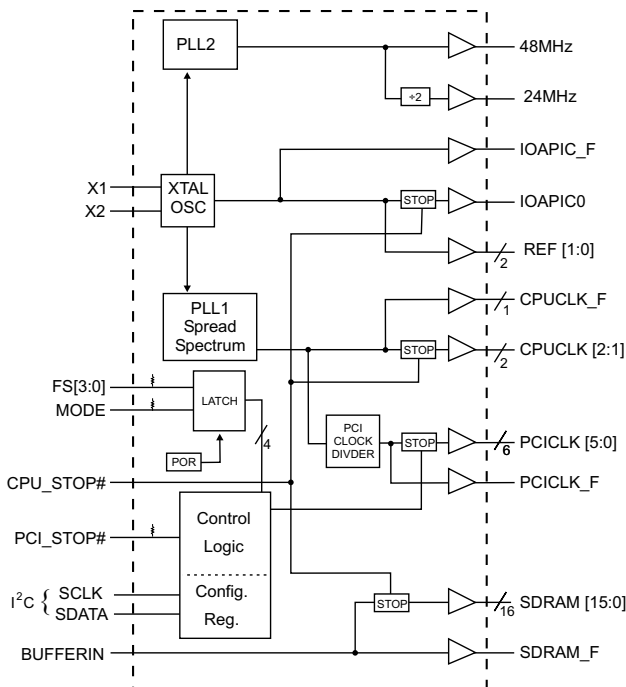
**Pin Configuration**



**56-Pin SSOP**

\* Internal Pull-up Resistor of 240K to 3.3V on indicated inputs  
 \*\* Internal Pull-down resistor of 240K to GND on indicated inputs.

**Block Diagram**



**Functionality**

FS3	FS2	FS1	FS0	CPU (MHz)	PCICLK (MHz)
1	1	1	1	133	33.3 (CPU/4)
1	1	1	0	124	31 (CPU/4)
1	1	0	1	150	37.5 (CPU/4)
1	1	0	0	140	35 (CPU/4)
1	0	1	1	105	35 (CPU/3)
1	0	1	0	110	36.67 (CPU/3)
1	0	0	1	115	38.33 (CPU/3)
1	0	0	0	120	40.00 (CPU/3)
0	1	1	1	100.3	33.43 (CPU/3)
0	1	1	0	133	44.33 (CPU/3)
0	1	0	1	112	37.33 (CPU/3)
0	1	0	0	103	34.33 (CPU/2)
0	0	1	1	66.8	33.40 (CPU/2)
0	0	1	0	83.3	41.65 (CPU/2)
0	0	0	1	75	37.5 (CPU/2)
0	0	0	0	124	41.33 (CPU/2)



**Pin Configuration**

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2	REF1	OUT	14.318 MHz reference clock output
	FS2 <sup>1</sup>	IN	Latched frequency select input. Has pull-up to VDDPCI
3	REF0	OUT	14.318MHz reference clock output
	PCI_STOP# <sup>1</sup>	IN	Halts PCICLK [5:0] at logic "0" level when low. (in mobile, MODE=0)
4, 10, 23, 26, 34, 42, 48, 53	GND	PWR	Ground.
5	X1	IN	14.318MHz input. Has internal load cap, (nominal 33pF).
6	X2	OUT	Crystal output. Has internal load cap (33pF) and feedback resistor to X1
8	PCICLK_F	OUT	Free running BUS clock not affected by PCI_STOP#
	MODE <sup>1</sup>	IN	Latched input for MODE select. Converts pin 3 to PCI_STOP# when low for power management.
9	FS3 <sup>1</sup>	IN	Latched frequency select input, pull-down
	PCICLK0	OUT	Free running BUS clock not affected by PCI_STOP#
16, 14, 13, 12, 11	PCICLK [5:1]	OUT	PCI Clock Outputs.
17	BUFFERIN	IN	Input for Buffers
27	SDATA	IN	Serial data in for serial config port. (I <sup>2</sup> C)
28	SCLK	IN	Clock input for serial config port. (I <sup>2</sup> C)
30	24MHz	OUT	24MHz clock output for Super I/O or FD.
	FS0 <sup>1</sup>	IN	Latched frequency select input. Has pull-up to VDD4.
29	48MHz	OUT	48MHz clock output for USB.
	FS1 <sup>1</sup>	IN	Latched frequency select input. Has pull-up to VDD2.
1, 7, 15, 20, 31, 37, 45	VDDPCI, VDDREF, VDDSDR, VDD48	PWR	Nominal 3.3V power supply, see power groups for function.
24, 25, 32, 33, 18, 19, 21, 22, 35, 36, 38, 39, 40, 41, 43, 44	SDRAM [15:0]	OUT	SDRAM clocks
46	SDRAM_F	OUT	Free running SDRAM clock Not affected by CPU_STOP#
47	CPU_STOP#	IN	Halts CPUCLK [2:1], IOAPIC0, SDRAM [15:0] clocks at logic "0" level when low.
50, 56	VDDLCPU, VDDLIOAPIC	PWR	CPU and IOAPIC clock buffer power supply, 2.5V nominal.
55	IOAPIC0	OUT	IOAPIC clock output. (14.318 MHz) Poweredby VDDLIOAPIC
51, 49	CPUCLK [2:1]	OUT	CPU Output clocks. Powered by VDDL2 (60 or 66.6MHz)
52	CPUCLK_F	OUT	Free running CPU output clock. Not affected ty the CPU_STOP#.
54	IOAPIC_F	OUT	Freerunning IOAPIC clock output. Not affected by the CPU_STOP# (14.31818 MHz) Powered by VDDLIOAPIC

**Notes:**

- 1: Bidirectional input/output pins, input logic levels are latched at internal power-on-reset. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low.



## General Description

The **ICS9250-08** is the single chip clock solution for Desktop/ designs using BX, Appollo Pro 133 type of chip sets. It provides all necessary clock signals for such a system.

Spread spectrum may be enabled through I<sup>2</sup>C programming. Spread spectrum typically reduces system EMI by 8dB to 10dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9250-08 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Serial programming I<sup>2</sup>C interface allows changing functions, stop clock programming and frequency selection.

## Power Groups

VDDREF = REF [1:0], X1, X2  
VDDPCI = PCICLK\_F, PCICLK [5:0]  
VDDSDR = SDRAM [15:0], supply for PLL core,  
VDD48 = 48MHz, 24MHz  
VDDLIOAPIC = IOAPIC\_F  
VDDLCPU = CPUCLK\_F [2:1]

## Mode Pin - Power Management Input Control

MODE (Latched Input)	
0	PCI_STOP# (Input)
1	REF0 (Output)



## General I<sup>2</sup>C serial interface information

The information in this section assumes familiarity with I<sup>2</sup>C programming. For more information, contact ICS for an I<sup>2</sup>C programming application note.

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2<sub>(H)</sub>
- ICS clock will *acknowledge*
- Controller (host) sends a dummy command code
- ICS clock will *acknowledge*
- Controller (host) sends a dummy byte count
- ICS clock will *acknowledge*
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will *acknowledge* each byte *one at a time*.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D2 <sub>(H)</sub>	
	<b>ACK</b>
Dummy Command Code	
	<b>ACK</b>
Dummy Byte Count	
	<b>ACK</b>
Byte 0	
	<b>ACK</b>
Byte 1	
	<b>ACK</b>
Byte 2	
	<b>ACK</b>
Byte 3	
	<b>ACK</b>
Byte 4	
	<b>ACK</b>
Byte 5	
	<b>ACK</b>
Stop Bit	

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3<sub>(H)</sub>
- ICS clock will *acknowledge*
- ICS clock will send the *byte count*
- Controller (host) acknowledges
- ICS clock sends first byte (*Byte 0*) through *byte 5*
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	ICS (Slave/Receiver)
Start Bit	
Address D3 <sub>(H)</sub>	
	<b>ACK</b>
	<b>Byte Count</b>
ACK	
	<b>Byte 0</b>
ACK	
	<b>Byte 1</b>
ACK	
	<b>Byte 2</b>
ACK	
	<b>Byte 3</b>
ACK	
	<b>Byte 4</b>
ACK	
	<b>Byte 5</b>
ACK	
Stop Bit	

### Notes:

1. The ICS clock generator is a slave/receiver, I<sup>2</sup>C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol.**
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I<sup>2</sup>C interface, the protocol is set to use only "Block-Writes" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



## Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Description	PWD
Bit 7	0 - $\pm 0.25\%$ Spread Spectrum Modulation 1 - $\pm 0.5\%$ Spread Spectrum Modulation	0
	Bit2 Bit6 Bit5 Bit4      CPU clock      PCI	
Bit 2, Bit 6:4	0111      100.3      33.43 (CPU/3)	Note1
	0110      133      44.33 (CPU/3)	
	0101      112      37.33 (CPU/3)	
	0100      103      34.3 (CPU/3)	
	0011      66.8      33.4 (CPU/2)	
	0010      83.3      41.65(CPU/2)	
	0001      75      37.5 (CPU/2)	
	0000      124      41.33 (CPU/3)	
	1111      133      33.25 (CPU/4)	
	1110      124      31.00 (CPU/4)	
	1101      150      37.50 (CPU/4)	
	1100      140      35.00 (CPU/4)	
	1011      105      35.00 (CPU/3)	
	1010      110      36.67 (CPU/3)	
1001      115      38.33 (CPU/3)		
1000      120      40.00 (CPU/3)		
Bit 3	0 - Frequency is selected by hardware select, Latched Inputs 1 - Frequency is selected by Bit 2, 6:4 (above)	0
Bit 1	0 - Normal 1 - Spread Spectrum Enabled (Center Spread)	0
Bit 0	0 - Running 1 - Tristate all outputs	0

**Note 1.** Default at Power-up will be for latched logic inputs to define frequency. Bits 2, 4, 5, 6 are default to 0000, and if bit 3 is written to a 1 to use Bits 2, 6:4, then these should be defined to desired frequency at same write cycle.

**Note:** PWD = Power-Up Default



**Byte 1: CPU, Active/Inactive Register**  
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	1	Reserved
Bit 3	46	1	SDRAM_F (Act/Inact)
Bit 2	49	1	CPUCLK2 (Act/Inact)
Bit 1	51	1	CPUCLK1 (Act/Inact)
Bit 0	52	1	CPUCLK_F (Act/Inact)

**Byte 2: PCI, Active/Inactive Register**  
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	8	1	PCICLK_F (Act/Inact)
Bit 5	16	1	PCICLK5 (Act/Inact)
Bit 4	14	1	PCICLK4 (Act/Inact)
Bit 3	13	1	PCICLK3 (Act/Inact)
Bit 2	12	1	PCICLK2 (Act/Inact)
Bit 1	11	1	PCICLK1 (Act/Inact)
Bit 0	9	1	PCICLK0 (Act/Inact)

**Byte 3: SDRAM, Active/Inactive Register**  
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	1	Reserved
Bit 5	30	1	24MHz (Act/Inact)
Bit 4	29	1	48MHz (Act/Inact)
Bit 3	33, 32, 25, 24	1	SDRAM(12:15) (Act/Inact)
Bit 2	22, 21, 19, 18	1	SDRAM (8:11) (Act/Inact)
Bit 1	39, 38, 36, 35	1	SDRAM (4:7) (Act/Inact)
Bit 0	44, 43, 41, 40	1	SDRAM0 (0:3) (Act/Inact)

**Byte 4: Reserved , Active/Inactive Register**  
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	Latched FS0#
Bit 6	-	1	Reserved
Bit 5	-	1	Reserved
Bit 4	-	X	Latched FS1#
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	-	X	Latched FS3#
Bit 0	-	1	Reserved

**Byte 5: Peripheral , Active/Inactive Register**  
(1= enable, 0 = disable)

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	1	Reserved
Bit 6	-	X	Latched FS2#
Bit 5	54	1	IOAPIC_F (Act/Inact)
Bit 4	55	1	IOAPIC0 (Act/Inact)
Bit 3	-	1	Reserved
Bit 2	-	1	Reserved
Bit 1	2	1	REF1 (Act/Inact)
Bit 0	3	1	REF0 (Act/Inact)

**Notes:**

1. Inactive means outputs are held LOW and are disabled from switching.
2. Latched Frequency Selects (FS#) will be inferred logic load of the input frequency select pin conditions.



## Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) on the **ICS9250-08** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 4-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kiloohm(10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figs. 1 and 2 show the recommended means of implementing this function. In Fig. 1 either one of the resistors is loaded onto the board (selective stuffing) to configure the device's internal logic. Figs. 2a and b provide a single resistor loading option where either solder spot tabs or a physical jumper header may be used.

These figures illustrate the optimal PCB physical layout options. These configuration resistors are of such a large ohmic value that they do not effect the low impedance clock signals. The layouts have been optimized to provide as little impedance transition to the clock signal as possible, as it passes through the programming resistor pad(s).

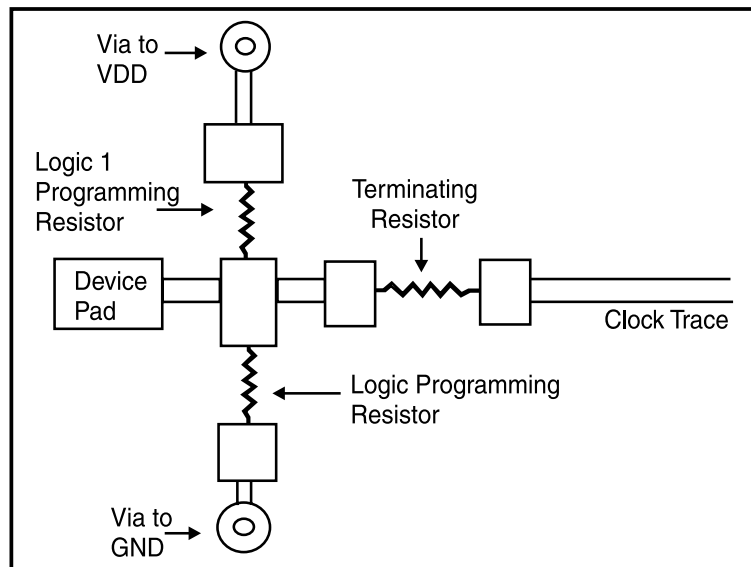


Fig. 1

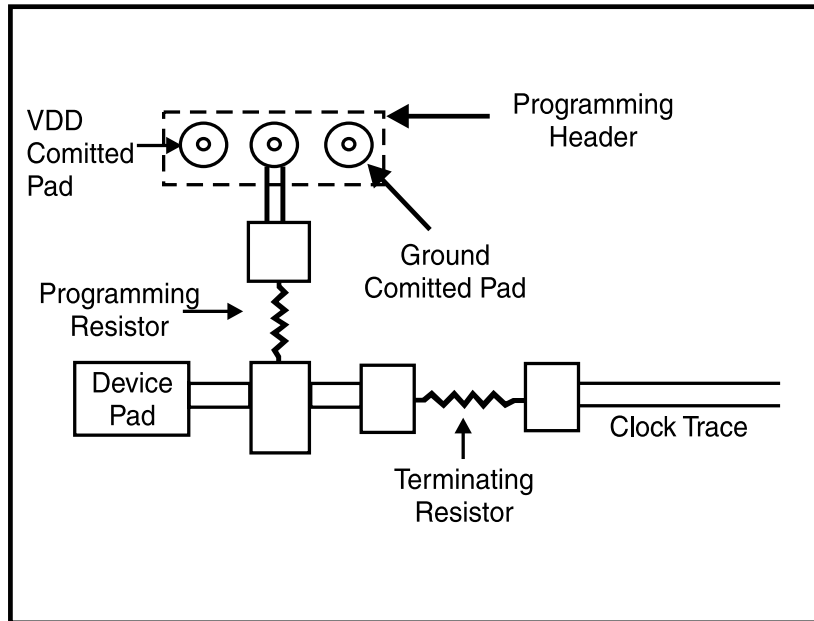


Fig. 2a

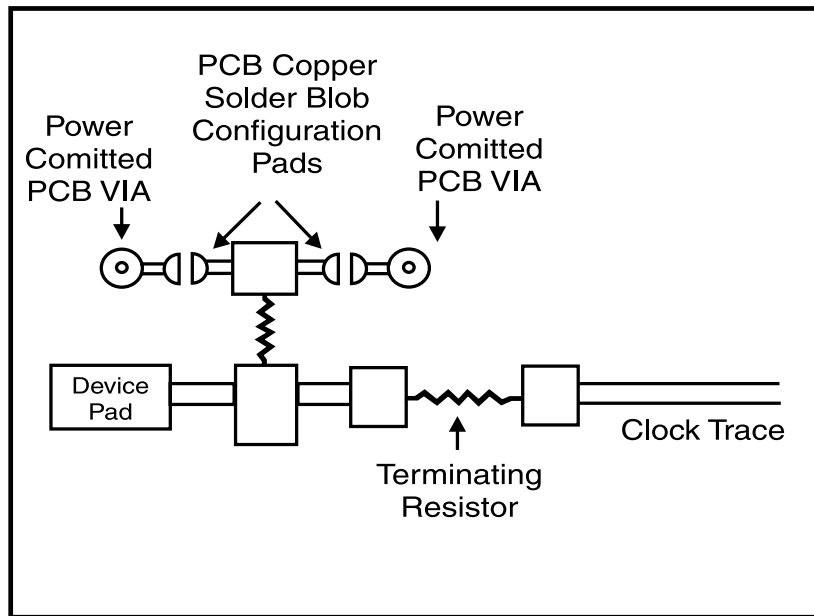


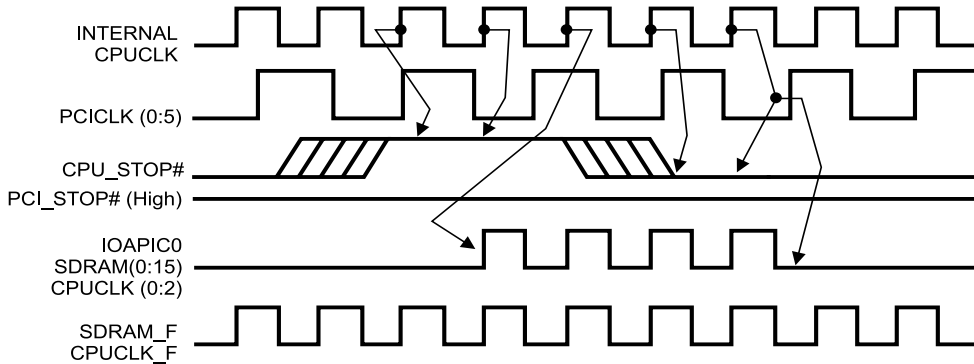
Fig. 2b





### CPU\_STOP# Timing Diagram

CPUSTOP# is an asynchronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU\_STOP# is synchronized by the ICS9250-08. All other clocks will continue to run while the CPUCLKs are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.

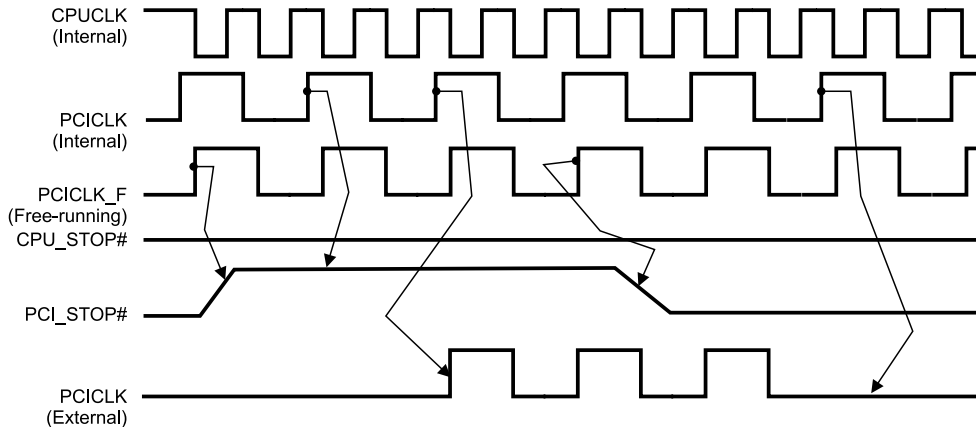


**Notes:**

1. All timing is referenced to the internal CPUCLK.
2. CPU\_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the ICS9250-08.
3. IOAPIC output is stopped Glitch Free by CPUSTOP# going low.
4. PCI\_STOP# is shown in a high (true) state.
5. All other clocks continue to run undisturbed.

### PCI\_STOP# Timing Diagram

PCI\_STOP# is an asynchronous input to the ICS9250-08. It is used to turn off the PCI\_CLK (0:5) clocks for low power operation. PCI\_STOP# is synchronized by the ICS9250-08 internally. PCI\_CLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCI\_CLK (0:5) clock on latency cycles are only one rising PCI\_CLK clock off latency is one PCI\_CLK clock.



**Notes:**

1. All timing is referenced to the Internal CPUCLK (defined as inside the device.)
2. PCI\_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the device.
3. All other clocks continue to run undisturbed.
4. CPU\_STOP# is shown in a high (true) state.



### Absolute Maximum Ratings

- Supply Voltage ..... 7.0 V
- Logic Inputs ..... GND -0.5 V to  $V_{DD} + 0.5 V$
- Ambient Operating Temperature ..... 0°C to +70°C
- Case Temperature ..... 115°C
- Storage Temperature ..... -65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

### Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ C$ ; Supply Voltage  $V_{DD} = 3.3 V \pm 5\%$ ,  $V_{DDL} = 2.5 V \pm 5\%$  (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	$V_{IH}$		2		$V_{DD} + 0.3$	V
Input Low Voltage	$V_{IL}$		$V_{SS} - 0.3$		0.8	V
Input High Current	$I_{IH}$	$V_{IN} = V_{DD}$		0.1	5	$\mu A$
Input Low Current	$I_{IL1}$	$V_{IN} = 0 V$ ; Inputs with no pull-up resistors	-5	2.0		$\mu A$
Input Low Current	$I_{IL2}$	$V_{IN} = 0 V$ ; Inputs with pull-up resistors	-200	-100		$\mu A$
Operating Supply Current	$I_{DD3.30P66}$	Select @ 66MHz; Sdram running, unloaded		112	140	mA
	$I_{DD3.30P100}$	Select @ 100MHz; Sdram running, unloaded		150	180	
	$I_{DD3.30P133}$	Select @ 133MHz; Sdram running, unloaded		200	250	
Input frequency	$F_i$	$V_{DD} = 3.3 V$	12	14.318	16	MHz
Input Capacitance <sup>1</sup>	$C_{IN}$	Logic Inputs			5	pF
	$C_{INX}$	X1 & X2 pins	27	36	45	pF
Transition Time <sup>1</sup>	$T_{Trans}$	To 1st crossing of target Freq.			3	ms
Settling Time <sup>1</sup>	$T_S$	From 1st crossing to 1% target Freq.		1	3	ms
Clk Stabilization <sup>1</sup>	$T_{Stab}$	From $V_{DD} = 3.3 V$ to 1% target Freq.			3	ms

<sup>1</sup>Guaranteed by design, not 100% tested in production.

### Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A = 0 - 70^\circ C$ ; Supply Voltage  $V_{DD} = 3.3 V \pm 5\%$ ,  $V_{DDL} = 2.5 V \pm 5\%$  (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating	$I_{DD2.50P66}$	Select @ 66MHz; Max discrete cap loads		10	25	mA
Operating Supply Current	$I_{DD2.50P100}$	Select @ 100MHz; Max discrete cap loads		13	25	
	$I_{DD2.50P133}$	Select @ 133MHz; Max discrete cap loads		18	25	

<sup>1</sup>Guaranteed by design, not 100% tested in production.



### Electrical Characteristics - CPUCLK

T<sub>A</sub> = 0 - 70° C; V<sub>DD</sub> = 3.3 V +/-5%, V<sub>DDL</sub> = 2.5 V +/-5%; C<sub>L</sub> = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V <sub>OH2B</sub>	I <sub>OH</sub> = -12.0 mA	2	2.3		V
Output Low Voltage	V <sub>OL2B</sub>	I <sub>OL</sub> = 12 mA		0.3	0.4	V
Output High Current	I <sub>OH2B</sub>	V <sub>OH</sub> = 1.7 V		-35	-19	mA
Output Low Current	I <sub>OL2B</sub>	V <sub>OL</sub> = 0.7 V	19	26		mA
Rise Time	t <sub>r2B</sub> <sup>1</sup>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.0 V	0.4	1.4	1.8	ns
Fall Time	t <sub>f2B</sub> <sup>1</sup>	V <sub>OH</sub> = 2.0 V, V <sub>OL</sub> = 0.4 V	0.4	1.35	1.8	ns
Duty Cycle	d <sub>t1B</sub> <sup>1</sup>	V <sub>T</sub> = 1.25 V; CPU < 120MHz	45	45	55	%
	d <sub>t2B</sub> <sup>1</sup>	V <sub>T</sub> = 1.25 V; CPU >= 124MHz	35	43	50	
Skew	t <sub>sk2B</sub> <sup>1</sup>	V <sub>T</sub> = 1.25 V; CPU >= 100 MHz		150	175	ps
	t <sub>sk2B</sub> <sup>1</sup>	V <sub>T</sub> = 1.25 V; CPU < 100 MHz		170	240	
Jitter, One Sigma	t <sub>j1σ2B</sub> <sup>1</sup>	V <sub>T</sub> = 1.25 V		35	150	ps
Jitter, Absolute	t <sub>jabs2B</sub> <sup>1</sup>	V <sub>T</sub> = 1.25 V	-250	99	+250	
Jitter, Cycle-to-cycle	t <sub>jycyc-cyc2B</sub> <sup>1</sup>	V <sub>T</sub> = 1.25 V		210	250	

<sup>1</sup>Guaranteed by design, not 100% tested in production.

### Electrical Characteristics - PCICLK

T<sub>A</sub> = 0 - 70° C; V<sub>DD</sub> = 3.3 V +/-5%, V<sub>DDL</sub> = 2.5 V +/-5%; C<sub>L</sub> = 60 pF for PCI0 & PCI1, CL = 30 pF for other PCIs

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V <sub>OH1</sub>	I <sub>OH</sub> = -18 mA	2.4	2.9		V
Output Low Voltage	V <sub>OL1</sub>	I <sub>OL</sub> = 9.4 mA		0.2	0.4	V
Output High Current	I <sub>OH1</sub>	V <sub>OH</sub> = 2.0 V		-52	-22	mA
Output Low Current	I <sub>OL1</sub>	V <sub>OL</sub> = 0.8 V	25	41		mA
Rise Time <sup>1</sup>	t <sub>r1</sub>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V	0.5	2.2	2.6	ns
Fall Time <sup>1</sup>	t <sub>f1</sub>	V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V	0.5	1.8	2.2	ns
Duty Cycle <sup>1</sup>	d <sub>t1</sub>	V <sub>T</sub> = 1.5 V	46	50	56	%
Skew <sup>1</sup> window	t <sub>sk1</sub>	V <sub>T</sub> = 1.5 V; All PCI clocks including PCI0		400	850	ps
	t <sub>sk1</sub>	V <sub>T</sub> = 1.5 V; All PCI clocks except PCI0		250	500	
Jitter, One Sigma <sup>1</sup>	t <sub>j1σ1</sub>	V <sub>T</sub> = 1.5 V		15	150	ps
Jitter, Absolute <sup>1</sup>	t <sub>jabs1</sub>	V <sub>T</sub> = 1.5 V	-250	60	250	

<sup>1</sup>Guaranteed by design, not 100% tested in production.



### Electrical Characteristics - SDRAM

T<sub>A</sub> = 0 - 70° C; V<sub>DD</sub> = 3.3 V +/-5%, V<sub>DDL</sub> = 2.5 V +/-5%; C<sub>L</sub> = 30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V <sub>OH1</sub>	I <sub>OH</sub> = -28 mA	2.4	2.8		V
Output Low Voltage	V <sub>OL1</sub>	I <sub>OL</sub> = 19 mA		0.34	0.4	V
Output High Current	I <sub>OH1</sub>	V <sub>OH</sub> = 2.0 V		-100	-42	mA
Output Low Current	I <sub>OL1</sub>	V <sub>OL</sub> = 0.8 V	33	42		mA
Rise Time <sup>1</sup>	t <sub>rl</sub>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V; 66, 75, 83 MHz	0.5	1.6	2.2	ns
	t <sub>rl</sub>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V; >= 100 MHz	0.5	1.3	1.6	
Fall Time <sup>1</sup>	t <sub>fl</sub>	V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V; 66, 75, 83 MHz	0.5	1.5	2.3	
	t <sub>fl</sub>	V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V; >= 100 MHz	0.5	1.5	1.8	
Duty Cycle <sup>1</sup>	d <sub>t1</sub>	V <sub>T</sub> = 1.5 V; Input Duty Cycle at 50%	47	52	57	%
Skew <sup>1</sup> Window	t <sub>sk1</sub>	V <sub>T</sub> = 1.5 V; SD_F to 0:6, 8:10		150	250	ps
	t <sub>sk1</sub>	V <sub>T</sub> = 1.5 VSD_F to 7, 12:15		210	400	
Jitter, One Sigma <sup>1</sup>	t <sub>j1σ1</sub>	V <sub>T</sub> = 1.5 V		50	150	
Jitter, Absolute <sup>1</sup>	t <sub>jabs1</sub>	V <sub>T</sub> = 1.5 V	-250	130	250	

<sup>1</sup>Guaranteed by design, not 100% tested in production.

### Electrical Characteristics - IOAPIC

T<sub>A</sub> = 0 - 70° C; V<sub>DD</sub> = 3.3 V +/-5%, V<sub>DDL</sub> = 2.5 V +/-5%; C<sub>L</sub> = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V <sub>OH4B</sub>	I <sub>OH</sub> = -8 mA	2	2.2		V
Output Low Voltage	V <sub>OL4B</sub>	I <sub>OL</sub> = 12 mA		0.3	0.4	V
Output High Current	I <sub>OH4B</sub>	V <sub>OH</sub> = 1.7 V		-24	-15	mA
Output Low Current	I <sub>OL4B</sub>	V <sub>OL</sub> = 0.7 V	19	26		mA
Rise Time <sup>1</sup>	T <sub>r4B</sub>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.0 V	0.4	1.3	1.6	ns
Fall Time <sup>1</sup>	T <sub>f4B</sub>	V <sub>OH</sub> = 2.0 V, V <sub>OL</sub> = 0.4 V	0.4	2	2.6	ns
Duty Cycle <sup>1</sup>	D <sub>t4B</sub>	V <sub>T</sub> = 1.25 V	45	51	55	%
Jitter, One Sigma <sup>1</sup>	T <sub>j1σ4B</sub>	V <sub>T</sub> = 1.25 V		240	300	ps
Jitter, Absolute <sup>1</sup>	T <sub>jabs4B</sub>	V <sub>T</sub> = 1.25 V		625	650	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.



### Electrical Characteristics - 48MHz, 24MHz, REF0

T<sub>A</sub> = 0 - 70° C; V<sub>DD</sub> = 3.3 V +/-5%, V<sub>DDL</sub> = 2.5 V +/-5%; C<sub>L</sub> = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V <sub>OH5</sub>	I <sub>OH</sub> = -12 mA	2.4	2.8		V
Output Low Voltage	V <sub>OL5</sub>	I <sub>OL</sub> = 12 mA		0.2	0.4	V
Output High Current	I <sub>OH5</sub>	V <sub>OH</sub> = 2.0 V		-33	-20	mA
Output Low Current	I <sub>OL5</sub>	V <sub>OL</sub> = 0.8 V	10	32		mA
Rise Time <sup>1</sup>	t <sub>r5</sub>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V, 48MHz		2	4	ns
Fall Time <sup>1</sup>	t <sub>f5</sub>	V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V, 48MHz		1.8	4	ns
Duty Cycle <sup>1</sup>	d <sub>t5</sub>	V <sub>T</sub> = 1.5 V, 48MHz	45	50	55	%
Rise Time <sup>1</sup>	t <sub>r5</sub>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V, REF0		2.2	4	ns
Fall Time <sup>1</sup>	t <sub>f5</sub>	V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V, REF0		1.8	4	ns
Duty Cycle <sup>1</sup>	d <sub>t5</sub>	V <sub>T</sub> = 1.5 V, REF	45	52	55	%
Jitter, Cycle-to-cycle <sup>1</sup>	t <sub>jeyc-cyc5</sub>	V <sub>T</sub> = 1.5 V, 24, 48MHz		700	1100	ps
Jitter, Cycle-to-cycle <sup>1</sup>	t <sub>jeyc-cyc5</sub>	V <sub>T</sub> = 1.5 V, REF0		500	800	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.

### Electrical Characteristics - REF1

T<sub>A</sub> = 0 - 70° C; V<sub>DD</sub> = 3.3 V +/-5%, V<sub>DDL</sub> = 2.5 V +/-5%; C<sub>L</sub> = 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V <sub>OH5</sub>	I <sub>OH</sub> = -14 mA	2.4	2.8		V
Output Low Voltage	V <sub>OL5</sub>	I <sub>OL</sub> = 6 mA		0.2	0.4	V
Output High Current	I <sub>OH5</sub>	V <sub>OH</sub> = 2.0 V		-28	-20	mA
Output Low Current	I <sub>OL5</sub>	V <sub>OL</sub> = 0.8 V	10	22		mA
Rise Time <sup>1</sup>	t <sub>r5</sub>	V <sub>OL</sub> = 0.4 V, V <sub>OH</sub> = 2.4 V, REF1		2.5	4	ns
Fall Time <sup>1</sup>	t <sub>f5</sub>	V <sub>OH</sub> = 2.4 V, V <sub>OL</sub> = 0.4 V, REF1		2.2	4	ns
Duty Cycle <sup>1</sup>	d <sub>t5</sub>	V <sub>T</sub> = 1.5 V, REF1	45	50	55	%
Jitter, Cycle-to-cycle <sup>1</sup>	t <sub>jeyc-cyc5</sub>	V <sub>T</sub> = 1.5 V, REF1		600	800	ps

<sup>1</sup>Guaranteed by design, not 100% tested in production.



**General Layout Precautions:**

- 1) Use a ground plane on the top layer of the PCB in all areas not used by traces.
- 2) Make all power traces and ground traces as wide as the via pad for lower inductance.

**Notes:**

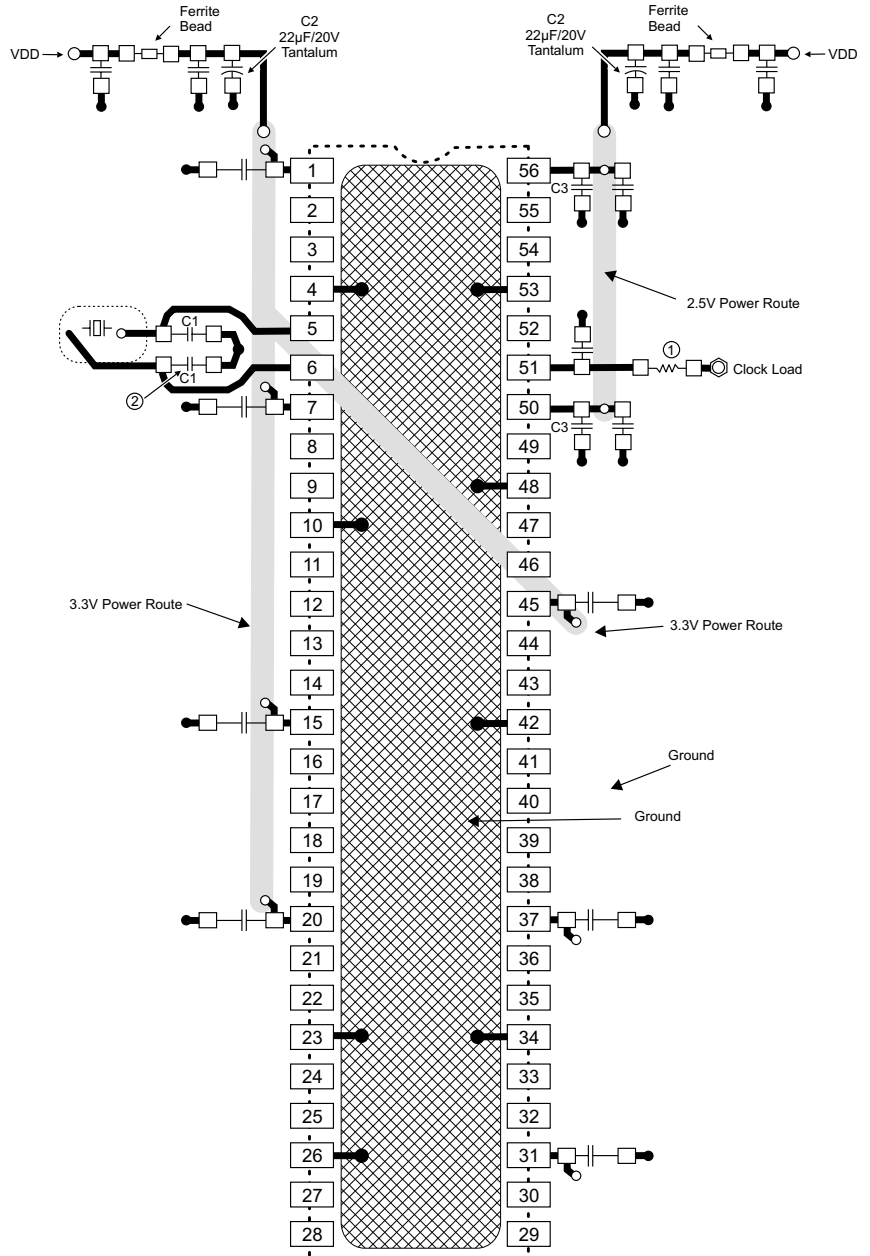
- 1) All clock outputs should have a series terminating resistor, and a 20pF capacitor to ground between the resistor and clock pin. Not shown in all places to improve readability of diagram.
- 2) Optional crystal load capacitors are recommended. They should be included in the layout but not inserted unless needed.

**Component Values:**

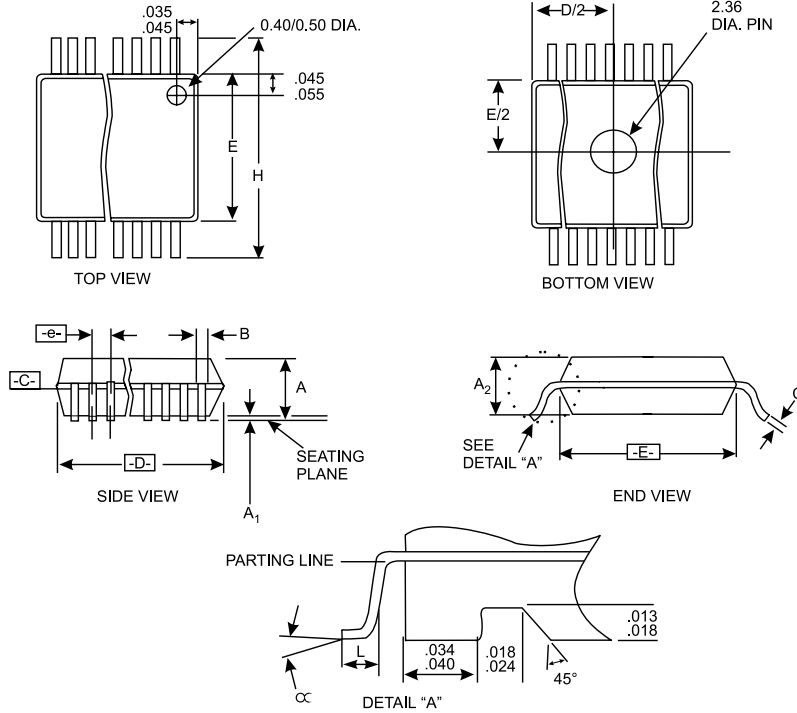
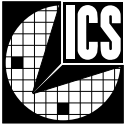
- C1 : Crystal load values determined by user
- C2 : 22µF/20V/D case/Tantalum  
AVX TAJD226M020R
- C3 : 100pF ceramic capacitor
- C4 : 20pF capacitor
- FB = Fair-Rite products 2512066017X1
- All unmarked capacitors are 0.01µF ceramic

**Connections to VDD:**

- Best
- Okay
- Avoid
- Avoid



- = Routed Power
- = Ground Connection (component side copper)
- = Ground Plane Connection
- = Power Route Connection
- = Solder Pads
- = Clock Load



SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AD	.720	.725	.730	56
A1	.008	.012	.016	<b>SSOP Package</b>				
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	-	.010					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∞	0°	5°	8°					
X	.085	.093	.100					

### Ordering Information

ICS9250yF-08

Example:

ICS XXXX y F - PPP

