Winbond

8K × 8 CMOS STATIC RAM

Slow Speed CMOS SRAMs

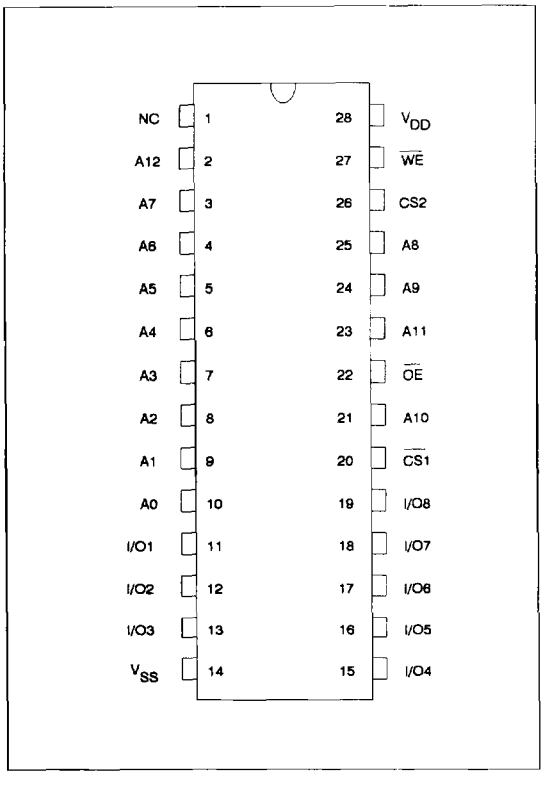
GENERAL DESCRIPTION

The W2465 is a slow speed, low power CMOS static RAM organized as 8192×8 bits that operates on a single 5-volt power supply. This device is manufactured using Winbond's high performance CMOS technology.

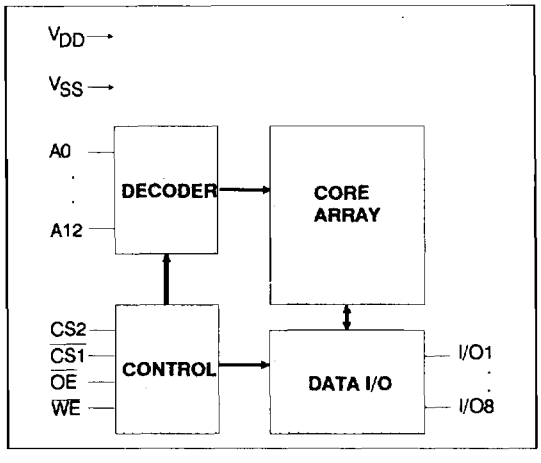
FEATURES

- **Low power consumption:**
  - Active: 200mW (typ.)
  - Standby: 5μW (typ.) (LL-version)
    10μW (typ.) (L-version)
- **Access time: 70/100 nS (max.)**
- **Single +5V power supply**
- **Fully static operation**
- **All inputs and outputs directly TTL compatible**
- **Three-state outputs**
- **Battery back-up operation capability**
- **Data retention voltage: 2V (min.)**
- **Available packages: 28-pin 600mil DIP, 330mil SOP, and 300mil skinny DIP**

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A12	Address Inputs
I/O1-I/O8	Data Inputs/Outputs
$\overline{CS1}$, CS2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power Supply
V_{SS}	Ground
NC	No Connection

Publication Release Date: September 1993
Revision A4

DC CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply Voltage to V_{SS} Potential	-0.5 to +7.0	V
Inputs/Outputs to V_{SS} Potential	-0.5 to V_{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	°C
Operating Temperature	0 to +70	°C

TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	MODE	I/O1-I/O8	V_{DD} CURRENT
H	X	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
X	L	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
L	H	H	H	Output Disable	High Z	I_{DD}
L	H	L	H	Read	Data Out	I_{DD}
L	H	X	L	Write	Data In	I_{DD}

OPERATING CHARACTERISTICS

(V_{DD} = 5V±10%, V_{SS} = 0V, Ta = 0 to 70 °C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V_{IL}	-		-0.5	-	+0.8	V
Input High Voltage	V_{IH}	-		+2.2	-	V_{DD} +0.5	V
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}		-2	-	+2	μA
Output Leakage Current	I_{LO}	$V_{I/O}$ = V_{SS} to V_{DD} $\overline{CS1}$ = V_{IH} or CS2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		-2	-	+2	μA
Output Low Voltage	V_{OL}	I_{OL} = +4.0mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -1.0mA		2.4	-	-	V
Operating Power Supply Current	I_{DD}	$\overline{CS1}$ = V_{IL}, CS2 = V_{IH} I/O = 0mA, Cycle = MIN Duty = 100%	70	-	-	70	mA
			100	-	-	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1}$ = V_{IH} or CS2 = V_{IL}		-	-	3	mA
	I_{SB1}	$\overline{CS1}$ ≥ V_{DD} -0.2V or CS2 ≤ 0.2V	LL	-	-	50	μA
			L	-	-	100	μA

Note: Typical characteristics are at V_{DD} = 5V, Ta = 25 °C.

CAPACITANCE

(V_{DD} = 5V, Ta = 25 °C, f = 1MHz)

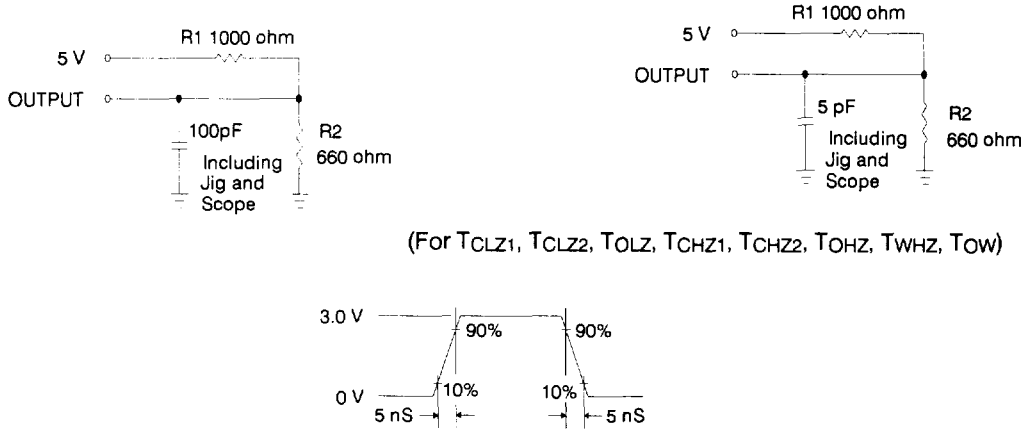
PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	8	pF

Note: These parameters are sampled but not 100% tested.

AC TEST CONDITIONS

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	5nS
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 100pF, I_{OH}/I_{OL} = -1mA/4mA

AC TEST LOADS AND WAVEFORM



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AC CHARACTERISTICS

(V_{DD} = 5V±10%, V_{SS} = 0V, Ta = 0 to 70 °C)

(1) READ CYCLE

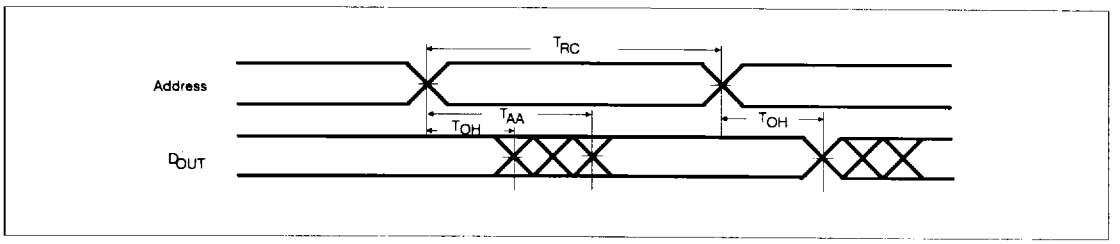
PARAMETER		SYM.	W2465-70		W2465-10		UNIT
			MIN.	MAX.	MIN.	MAX.	
Read Cycle Time		T_{RC}	70	-	100	-	nS
Address Access Time		T_{AA}	-	70	-	100	nS
Chip Select Access Time	$\overline{CS1}$	T_{ACS1}	-	70	-	100	nS
	CS2	T_{ACS2}	-	70	-	100	nS
Output Enable to Output Valid		T_{AOE}	-	35	-	50	nS
Chip Selection to Output in Low Z	$\overline{CS1}$	T_{CLZ1}	5	-	10	-	nS
	CS2	T_{CLZ2}	5	-	10	-	nS
Output Enable to Output in Low Z		T_{OLZ}	5	-	5	-	nS
Chip Deselection to Output in High Z	$\overline{CS1}$	T_{CHZ1}	-	30	-	35	nS
	CS2	T_{CHZ2}	-	30	-	35	nS
Output Disable to Output in High Z		T_{OHZ}	-	30	-	35	nS
Output Hold from Address Change		T_{OH}	5	-	10	-	nS

(2) WRITE CYCLE

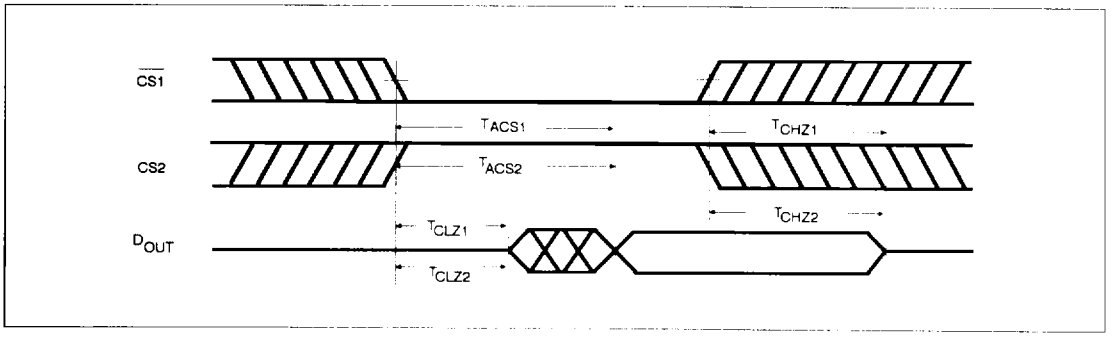
PARAMETER		SYM.	W2465-70		W2465-10		UNIT
			MIN.	MAX.	MIN.	MAX.	
Write Cycle Time		T_{WC}	70	-	100	-	nS
Chip Selection to End of Write		T_{CW}	60	-	80	-	nS
Address Valid to End of Write		T_{AW}	60	-	80	-	nS
Address Setup Time		T_{AS}	0	-	0	-	nS
Write Pulse Width		T_{WP}	40	-	60	-	nS
Write Recovery Time	$\overline{CS1}$, $\overline{WE}$	T_{WR1}	0	-	0	-	nS
	CS2	T_{WR2}	0	-	0	-	nS
Data Valid to End of Write		T_{DW}	30	-	40	-	nS
Data Hold from End of Write		T_{DH}	0	-	0	-	nS
Write to Output in High Z		T_{WHZ}	-	30	-	30	nS
Output Disable to Output in High Z		T_{OHZ}	-	30	-	30	nS
Output Active from End of Write		T_{OW}	0	-	0	-	nS

TIMING WAVEFORMS

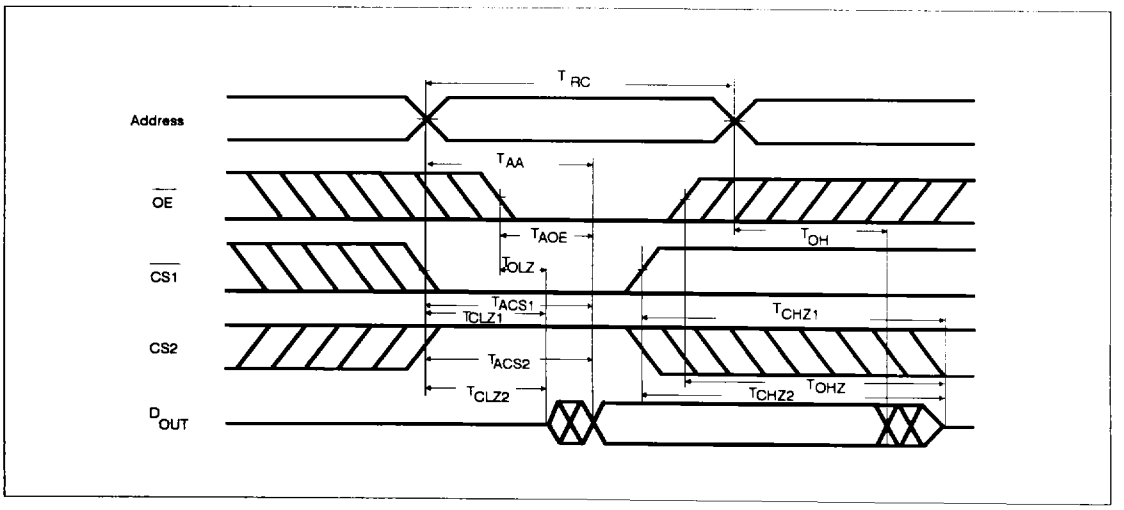
READ CYCLE 1
(Address Controlled)



READ CYCLE 2
(Chip Select Controlled)



READ CYCLE 3
(Output Enable Controlled)



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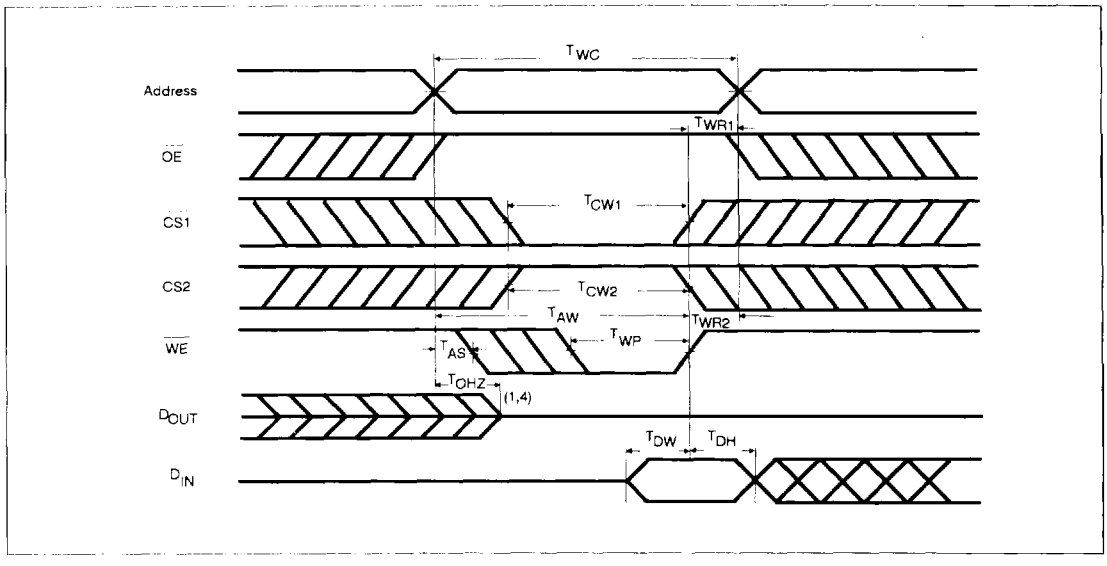
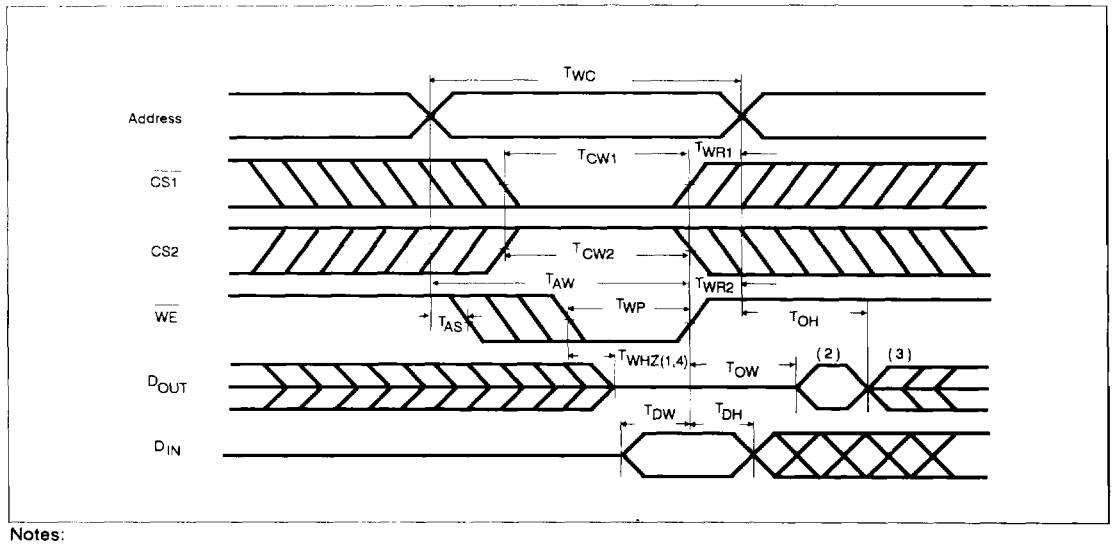
WRITE CYCLE 1



WRITE CYCLE 2
($\overline{OE}$ = V_{IL} Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from D_{OUT} are the same as the data written to D_{IN} during the write cycle.
3. D_{OUT} provides the read data for the next address.
4. Transition is measured ±500mV from steady state with C_L = 5pF. This parameter is guaranteed but not 100% tested.

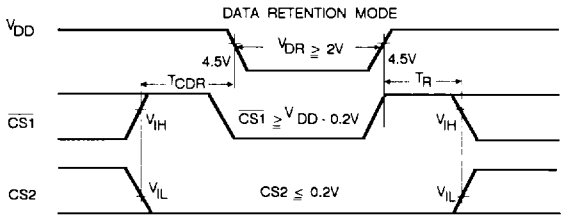
DATA RETENTION CHARACTERISTICS

(Ta = 0 to 70 °C)

PARAMETER	SYM.	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
V_{DD} for Data Retention	V_{DR}	$\overline{CS1} \geq V_{DD}$-0.2V, or CS2 ≤ 0.2V		2.0	-	-	V
Data Retention Current	I_{DDDR}	$\overline{CS1} \geq V_{DD}$-0.2V, or CS2 ≤ 0.2V V_{DD} = 3V	LL	-	-	20	μA
			L	-	-	50	μA
Chip Deselect to Data Retention Time	T_{CDR}	See retention waveform		0	-	-	nS
Operation Recovery Time	T_R			T_{RC}*	-	-	nS

T_{RC}* = Read Cycle Time

DATA RETENTION WAVEFORM



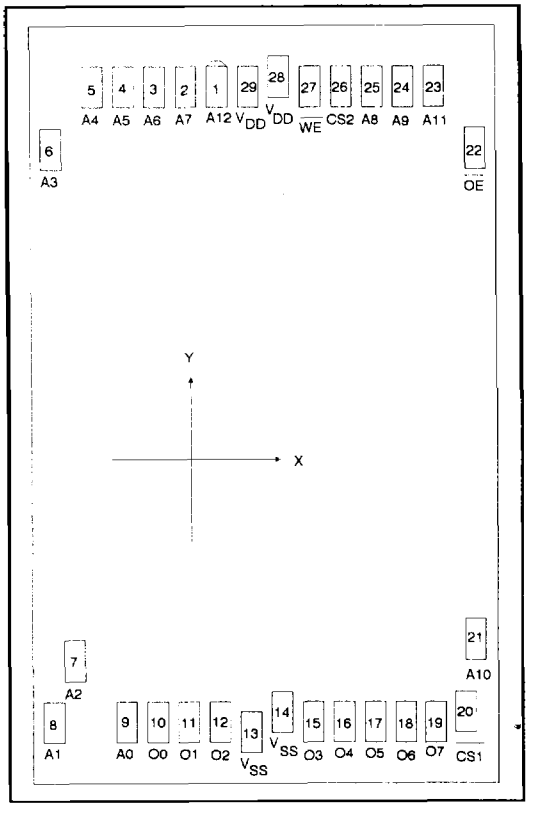
ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT Max. (mA)	STANDBY CURRENT Max. (mA)	PACKAGE
W2465-70LL	70	70	0.05	600mil DIP
W2465-10LL	100	60	0.05	600mil DIP
W2465-10L	100	60	0.1	600mil DIP
W2465S-70LL	70	70	0.05	330mil SOP
W2465S-10LL	100	60	0.05	330mil SOP
W2465S-10L	100	60	0.1	330mil SOP
W2465K-70LL	70	70	0.05	300mil Skinny
W2465K-10LL	100	60	0.05	300mil Skinny
W2465K-10L	100	60	0.1	300mil Skinny

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

BONDING PAD DIAGRAM



PAD NO.	X	Y
1	-259.5	1918.3
2	-418.1	1918.3
3	-608.7	1918.3
4	-767.3	1918.3
5	-957.9	1918.3
6	-1139.3	1677.0
7	-1043.8	-1719.5
8	-1135.6	-1907.3
9	-903.3	-1937.3
10	-706.2	-1973.4
11	-534.7	-1973.4
12	-369.3	-1973.4
13	-204.6	-2032.0
14	-45.7	-1922.3
15	132.3	-1973.4
16	297.7	-1973.4
17	469.2	-1973.4
18	634.6	-1973.4
19	806.1	-1973.4
20	1006.4	-1910.4
21	1043.8	-1740.7
22	1139.3	-1682.8
23	947.8	1918.3
24	757.2	1918.3
25	598.6	1918.3
26	408.0	1918.3
27	249.4	1918.3
28	75.1	1988.6
29	-84.9	1932.6

Note: For bare chip form (C. O. B.) applications, the substrate must be connected to V_{DD} or left floating in the PCB layout.