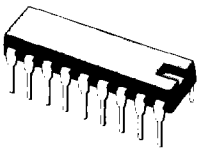
PROGRAMMABLE, OFF-LINE, PWM CONTROLLER

- ALL CONTROL, DRIVING, MONITORING, AND PROTECTION FUNCTIONS INCLUDED
- LOW-CURRENT, OFF-LINE START CIRCUIT
- FEED-FORWARD LINE REGULATION OVER 4 TO 1 INPUT RANGE
- PWM LATCH FOR SINGLE PULSE PER PERIOD
- PULSE-BY-PULSE CURRENT LIMITING PLUS SHUTDOWN FOR OVER-CURRENT FAULT
- NO START-UP OR SHUTDOWN TRANSIENTS
- SLOW TURN-ON AND MAXIMUM DUTY-CYCLE CLAMP
- SHUTDOWN UPON OVER-OR UNDERVOLTAGE SENSING
- LATCH OFF OR CONTINUOUS RETRY AFTER FAULT
- REMOTE, PULSE-COMMANDABLE START/STOP
- PWM OUTPUT SWITCH USABLE TO 1A PEAK CURRENT
- 1% REFERENCE ACCURACY
- 500 kHz OPERATION



DIP-18
(Plastic and Ceramic)

DESCRIPTION

Although containing most of the features required by all types of switching power supply controllers, the UC1840 family has been optimized for highly-efficient boot-strapped primaryside operation in forward or flyback power converters. Two important features for this mode are a starting circuit which requires little current from the primary input voltage and feed-forward control for constant volt-second operation over a wide input voltage range.

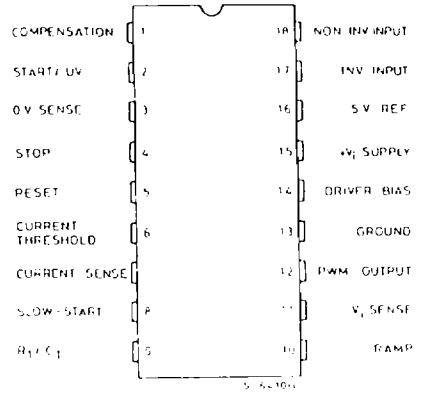
In addition to startup and normal regulating PWM functions, these devices offer built-in protection from over-voltage, under-voltage, and over-current fault conditions. This monitoring circuitry contains the added features that any fault will initiate a complete shutdown with provisions for either latch off or automatic restart. In the latch-off mode, the controller may be started and stopped with external pulsed or steady-state commands.

Other performance features of these devices include a 1% accurate reference, provision for slow-turn-on and duty-cycle limiting, and highspeed pulse-by-pulse current limiting in addition to current fault shutdown.

The UC1840's PWM output stage includes a latch to insure only a single pulse per period and is designed to optimize the turn off of an external switching device by conducting during the "OFF" time with a capability for both high peak current and low saturation voltage. These devices are available in an 18-pin dual-in-line plastic or ceramic package.

The UC1840 is characterized for operation over the full military temperature range of –55°C to +125°C. The UC2840 and UC3840 are designed for operation from –25°C to +85°C and 0°C to +70°C, respectively.

PIN CONNECTION AND ORDER CODES



Type	Plastic	Ceramic
UC1840	–	UC1840J
UC2840	UC2840N	UC2840J
UC3840	UC3840N	UC3840J

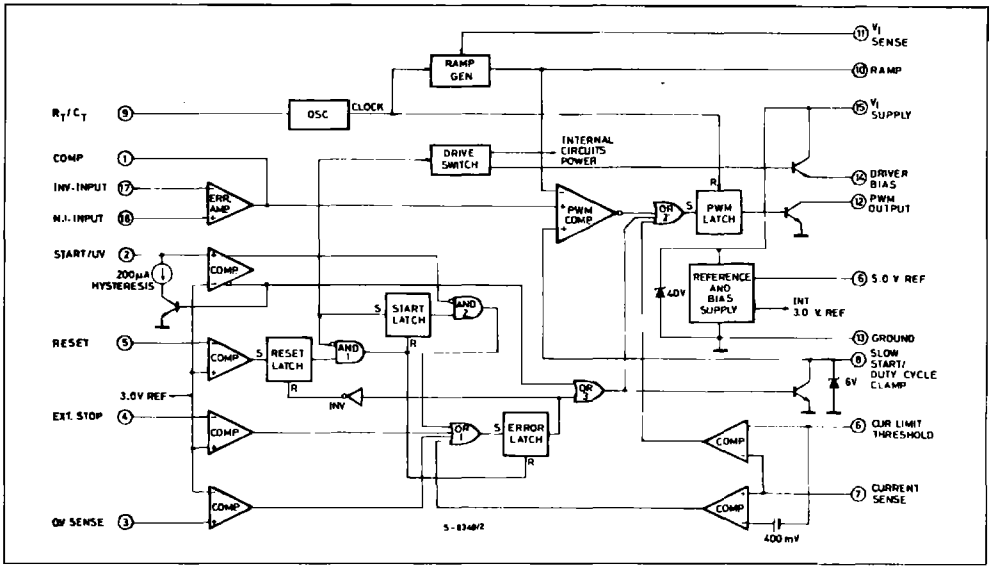
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test Conditions	Unit
V_i	Supply Voltage + V_i (pin 15) Voltage Driven Current Driven 100 mA Maximum	 32 Self Limiting	 V
V_o	PWM Output Volage (pin 12)	40	V
I_o	PWM Output Current, Steady-state (pin 12)	400	mA
E_{op}	PWM Output Peak Energy Discharge Driver Bias Current (pin 14)	20 –200	µJ mA
$I_{o(REF)}$	Reference Output Current (pin 16) Slow Start Sink Current (pin 8) V_i Sense Current (pin 11) Current Limit Inputs (pin 6, 7) Comparator Inputs (pins 2, 3, 4, 5, 17, 18)	– 50 20 10 – 0.5 to + 55 – 0.3 to + 32	mA mA mA V V
P_{tot}	Power Dissipation at T_{amb} = 70 °C	1000	mW
T_j	Junction Temperature Range	– 55 to + 150	°C
T_{op}	Operating Ambient Temperature Range : UC1840 UC2840 UC3840	– 55 to + 125 – 25 to + 85 0 to + 70	°C °C °C
T_{stg}	Storage Temperature	– 65 to + 150	°C

THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max	80	°C/W

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Name	Function

PWM CONTROL

OSCILLATOR	Generates a fixed-frequency internal clock from an external R_T and C_T. Frequency = $\frac{K_c}{R_T C_T}$ where K_c is a first-order correction factor = 0.3 log (C_T x 10^{12}).
RAMP GENERATOR	Develops a linear ramp with a slope defined externally by $\frac{dv}{dt} = \frac{\text{sense voltage}}{R_R C_R}$. C_R is normally selected ≤ C_T and its value will have some effect upon valley voltage. C_R terminal can be used as an input port for current mode control.
ERROR AMPLIFIER	Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance : unity-gain stable.
REFERENCE GENERATOR	Precision 5.0 V for internal and external usage to 50 mA. Tracking 3.0 V reference for internal usage only with nominal accuracy of ± 2 %. 40 V clamp zener for chip 0. V. protection, 100 mA maximum current.
PWM COMPARATOR	Generates output pulse wich starts at termination of clock pulse and ends when the ramp input crosses the lowest of two positive inputs.
PWM LATCH	Terminates the PWM output pulse when set by inputs for either the PWM comparator, the pulse-by-pulse current limit comparator, or the error latch. Resets wich each internal clock pulse.
PWM OUTPUT SWITCH	Transistor capable of sinking current to ground wich is off during the PWM on-time and turns on to terminate the power pulse. Current capacity is 400 mA saturated with peak capacitance discharge in excess of one amp.

FUNCTIONAL DESCRIPTION (continued)

Name	Function
SEQUENCING FUNCTIONS	
START/U. V. SENSE	This comparator performs three functions. With an increasing voltage, it generates a turn-on signal at a start threshold With a decreasing voltage, it generates a U. V. fault signal at a lower level separated by a 200 µA hysteresis current. At the U. V. threshold. it also resets the Error Latch if the Reset Latch has been set.
DRIVE SWITCH	Disables most of the chip to hold internal current consumption low. and Driver Bias OFF, until input voltage reaches start threshold.
DRIVE BIAS	Supplies drive current to external power switch to provide turn-on bias.
SLOW START	Clamps low to hold PWM OFF. Upon release. rises with rate controlled by R_sC_s for slow increase of output pulse width. Also used to clamp maximum duty cycle with divider R_s R_{DC}.
START LATCH	Keeps low input voltage at initial turn-on from being defined as a U. V. fault. Sets at start level to monitor for U. V. fault.
RESET LATCH	When reset, this latch insures no reset signal to either Start or Error latches so that first fault will lock the PWM off. When set. this latch resets the Start and Error latches at the U. V. low threshold, allowing a restart.
PROTECTION FUNCTIONS	
ERROR LATCH	When set by momentary input. this latch insures immediate PWM shutdown and hold off until reset. Inputs to Error Latch are : a. U. V. low (after turn-on) b. O. V. high c. Step low d. Current Sense 400 mV over threshold Error Latch resets at U. V. threshold if Reset Latch is set.
CURRENT LIMITING	Differential input comparator terminates individual output pulses each time sense voltage rises above threshold. When sense voltage rises to 400 mV above threshold. a shutdown signal it sent to Error Latch.

ELECTRICAL CHARACTERISTICS (refer to the test circuit. Unless otherwise stated, these specifications apply for T_j = – 55 to + 125 °C for the UC1840, – 25 °C to + 85 °C for the UC2840 and 0 to + 70 °C for the UC3840; V_i = 20 V, R_T = 20 KΩ, C_T = 0.001μF, C_R = 0.001 μF. current limit threshold = 200 mV)

Symbol	Parameter	Test Conditions	UC1840 UC2840			UC3840			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
POWER INPUTS									
I_{ST}	Start-up Current	V_i = 30 V. Pin 2 = 2.5 V. T_j = 25 °C		4	5.5		4	5.5	mA
	*Start-up Current T.C.	V_i = 30 V. Pin 2 = 2.5 V		– 0.1	– 0.2		– 0.1	– 0.2	%/°C
I_i	Operating Current	V_i = 30 V, Pin 2 = 3.5 V	5	10	15	5	10	15	mA
V_{SOV}	Supply O.V. Clamp	I_i = 20 m A	33	40	45	33	40	48	V
REFERENCE SECTION									
V_{REF}	Reference Voltage	T_j = 25 °C	4.95	5	5.05	4.9	5	5.1	V
ΔV_{REF}	Line Regulation	V_i = 8 to 30 V		10	15		10	20	mV
ΔV_{REF}	Load Regulation	I_L = 0 to 20mA		10	20		10	30	mV
$\Delta V_{REF}/\Delta T$*	Temperature Coeff.	Over Op. Temp. Range			± 0.4			± 0.4	mV/°C
I_{SC}	Short Circuit Curr.	V_{REF} = 0. T_j = 25 °C		– 80	– 100		– 80	– 100	mA
OSCILLATOR									
f_s	Nominal Frequency	T_j = 25 °C	47	50	53	45	50	55	KHz
	Voltage Stability	V_i = 8 to 30 V		0.5	1		0.5	1	%
	*Temperature Coeff.	Over Op. Temp. Range			± 0.8			± 0.8	%/°C
$f_{s(max)}$	Maxim. Frequency	R_T = 2 KΩ. C_T = 330 pF	500			500			KHz
RAMP GENERATOR									
	Ramp Current Min.	I_{SENSE} = – 10 μA		– 11	– 14		– 11	–14	μA
	Ramp Current Max.	I_{SENSE} = 1 mA	– 0.9	– 0.95		–0.9	–0.95		mA
	Ramp Valley		0.3	0.5	0.7	0.3	0.5	0.7	V
	Ramp Peak	Clamping Level	3.9	4.2	4.5	3.9	4.2	4.5	V

ELECTRICAL CHARACTERISTICS (continued)

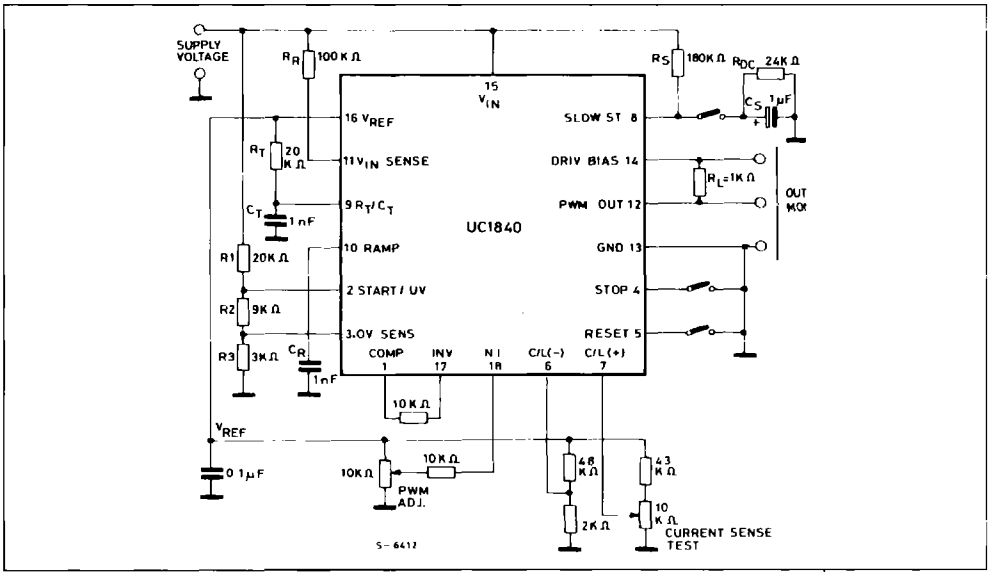
Symbol	Parameter	Test Conditions	UC1840 UC2840			UC3840			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
ERROR AMPLIFIER									
V_{os}	Input Offset Voltage	V_{CM} = 5 V		0.5	5		2	10	mV
I_b	Input Bias Current			0.5	2		1	5	µA
I_{os}	Input Offset Current				0.5			0.5	µA
G_v	Open Loop Gain	ΔV_o = 1 to 3 V	60	66		60	66		dB
	Output Swing (max Out ≤ Ramp Peak – 100 mV)	Minimum Total Range	0.3		3.5	0.3		3.5	V
CMR	Common Mode Rejection	V_{CM} = 1.5 to 5.5 V	70	80		70	80		dB
SVR	Supply Voltage Rejection	V_i = 8 to 30 V	40	50		40	50		dB
I_{SC}	Short Circuit Current	V_{comp} = 0V		– 4	– 10		– 4	– 10	mA
B*	Gain Bandwidth	T_j = 25 °C, G_V = 0 dB	1	2		1	2		MHz
SR*	Slew Rate	T_j = 25 °C, G_V = 0 dB		0.8			0.8		V/µs
PWM SECTION									
	*Continuous Duty Cycle Range (other than zero)	Min. Total Cont. Range Ramp Peak < 4.2 V	5		95	5		95	%
$V_{o(sat)}$	Output Saturation	I_o = 20 mA		0.2	0.4		0.2	0.4	V
$V_{o(sat)}$	Output Saturation	I_o = 200 mA		1.7	2.2		1.7	2.2	V
I_{OL}	Output Leakage	V_o = 40 V		0.1	10		0.1	10	µA
τ_d	*Comparator Delay	Pin 8 to pin 12 T_j = 25 °C, R_L = 1 KΩ		300	500		300	500	ns
SEQUENCING FUNCTIONS									
V_T	Comparator Threshold	Pins 2, 3, 4, 5	2.8	3	3.2	2.8	3	3.2	V
I_b	Input Bias Current	Pins 3, 4, 5 = 0V		– 1	– 3		–1	–3	µA
	Start/UV Hysteresis Current	Pin 2 = 2.5 V, T_j = 25 °C	120	180	240	120	180	240	µA
	Input Leakage	V_i = 20 V		0.1	10		0.1	10	µA
	Driver Bias Saturation Voltage V_{IN}–V_{OH}	I_B = – 50 mA		2	3		2	3	V
	Driver Bias Leakage	V_B = 0V		– 0.1	– 10		– 0.1	– 10	µA
	Slow-start Saturation	I_s = 2 mA		0.2	0.5		0.2	0.5	V
	Slow-start Leakage	V_s = 4.5 V		0.1	2		0.1	2	µA

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	UC1840 UC2840			UC3840			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
CURRENT CONTROL									
	Current Limit Offset			0	5		0	10	mV
	Current Shutdown Offset		340	400	440	340	400	440	mV
I_b	Input Bias Current	Pin 7 = 0V		− 2	− 5		− 2	− 5	µA
	*Common mode Range		− 0.3		3	− 0.3		3	V
τ_d*	Current Limit Delay	T_j = 25 °C, Pin 7 to 12 R_L = 1 KΩ		200	400		200	400	ns

* Guaranteed by design. Not 100 % tested in production.

Figure 1 : Open Loop Test Circuit.



Nominal frequency = $\frac{1}{R_T C_T}$ = 50 kHz

Start voltage = $3 \frac{(R1 + R2 + R3)}{R2 + R3}$ + 0.2 R1 = 12 V

U.V. fault voltage = $3 \frac{(R1 + R2 + R3)}{R2 + R3}$ = 8 V

O.V. fault voltage = $3 \frac{(R1 + R2 + R3)}{R3}$ = 32 V

Current limit = 200mV

Current fault voltage = 600mV

Duty cycle clamp = 50%

Figure 2 : Start U.V. Hysteresis Current.

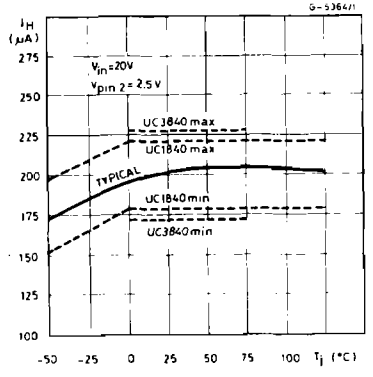


Figure 3 : PWM Output Saturation Voltage.

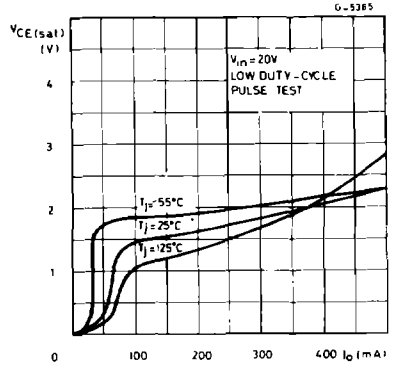


Figure 4 : Oscillator Frequency.

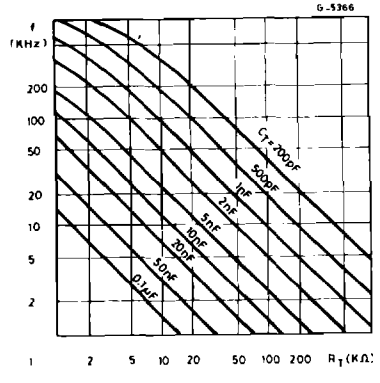


Figure 5 : PWM Output Minimum Pulse Width.

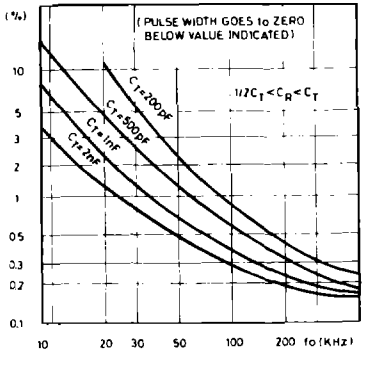


Figure 6 : Error Amplifier Open-loop Gain and Phase.

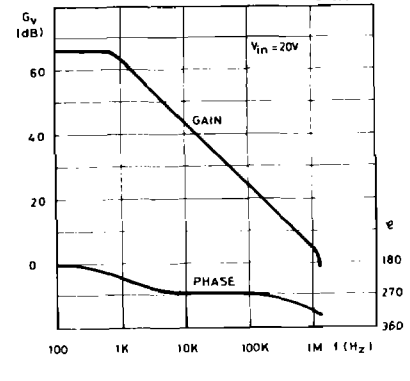
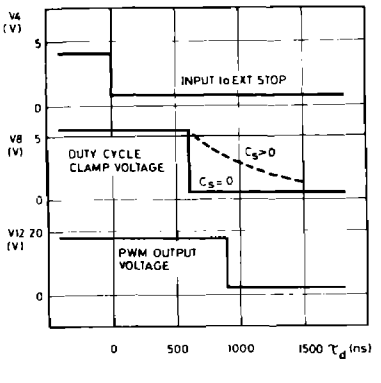
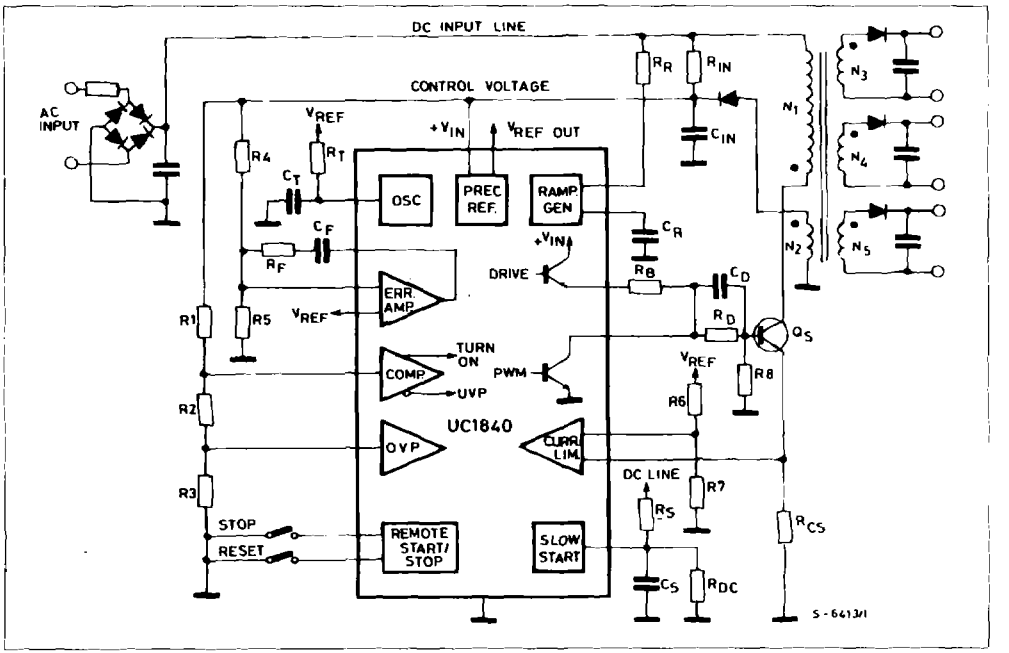


Figure 7 : Shutdown Timing.



APPLICATION INFORMATION

Figure 8 : Programmable PWM Controller in a Simplified Flyback Regulator.

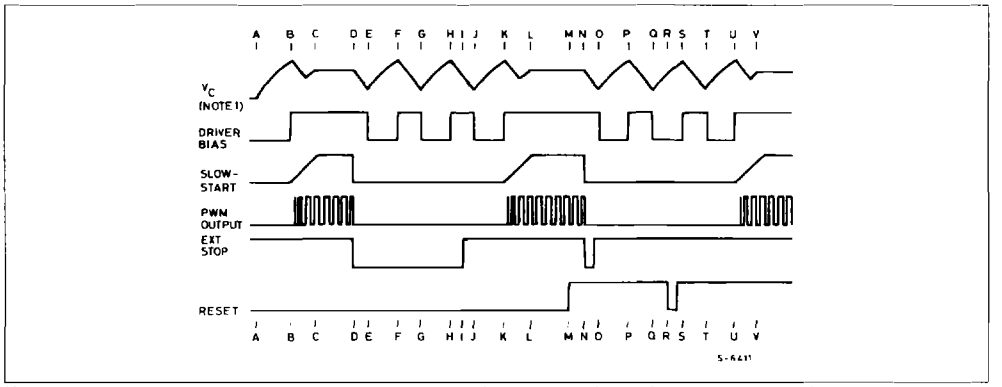


In this application [see Fig.8] complete control is maintained on the primary side. Control power is provided by R_{IN} and C_{IN} during start-up, and by a primary-referenced low voltage winding. N2, for efficient operation after start. The error amplifier loop is closed to regulate the DC voltage from N2 with other outputs following through their magnetic coupling - a task made even easier with the UC1840's feed-forward line regulation.

The UC1840 will readily accept digital start/stop commands transmitted from the secondary side by means of optical couplers.

Not shown are protective snubbers or additional interface circuitry which may be required by the choice of the high-voltage switch, Qs, or the application

Figure 9 : Power Sequencing Functions.



Notes : 1 VC represents an analog of the output voltage generated by a primary-referenced secondary winding of the power transformer. It is the voltage monitored by the start/U.V comparator and, in most cases, is the supply voltage. Vi, for the UC1840.
2. Although input to External Stop, Pin 4, is shown, results are the same for any fault input which sets the Error Latch.

POWER FREQUENCY FUNCTIONS

Time	Event
A	Initial Turn-on, V_c Rises with Light Load
B	Start Threshold. Driver Bias Loads V_c
C	Operating PWM Regulates V_c
D	Stop Input Sets Error Latch Turning off PWM
E	U. V. Low Threshold. Error Latch Remain Set
F	Start Turns on Driver Bias Bus Error Latch Still Set
G H	V_c and Driver Bias Continue to Cycle
I	Stop Command Removed
J	Error Latch Reset at U. V. Low Threshold
K	Start Threshold Now Removes Slow-start Clam

Time	Event
L	Return to Normal Run State
M	Reset Latch Set Signal Removed
N	Error Latch Set with Momentary Fault
O	Error Latch does not reset as Reset Latch is reset
P Q	V_c and Driver Bias Recycle with no Turn-on
R	Reset Latch Set is Set with Momentary Reset Signal
S	V_c must Complete Cycle to Turn-on
T	Start and Error Latches Reset
U	Normal Start Initiated
V	Return to Normal Run State