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# **SP8680B** 575MHz÷10/11

The SP8680B is an ECL variable modulus divider, with ECL and TTL compatible outputs. The circuit can operate from either ECL or TTL supplies. It divides by 10 when either of the ECL control inputs, <u>PE1</u> or <u>PE2</u>, is in the high state and by 11 when both are low (or open circuit). The divider can be set asynchronously to the eleventh state by applying a high level to the master set (MS) input.

#### **FEATURES**

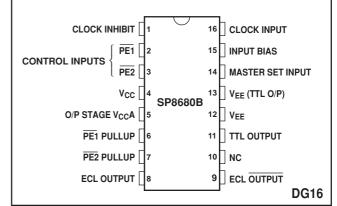
- Very High Speed 650MHz (Typ.)
- ECL and TTL Compatible Inputs/Outputs
- DC or AC Clocking
- Clock Inhibit
- Asynchronous Master Set
- Equivalent to Fairchild 11C90

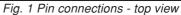
#### QUICK REFERENCE DATA

- Supply Voltage: -4.75V to -5.5V (ECL), 4.75V to 5.5V (TTL)
- Power Consumption: 420mW
- Temperature Range: -40°C to +85°C

#### **ABSOLUTE MAXIMUM RATINGS**

Supply voltage, $ V_{CC} - V_{FF} $	8V
ECL output source current	50mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
TTL output sink current	30mA
Max. clock input voltage	2·5V p-p





#### **ORDERING INFORMATION**

SP8680 B DG SP8680 NA 1C

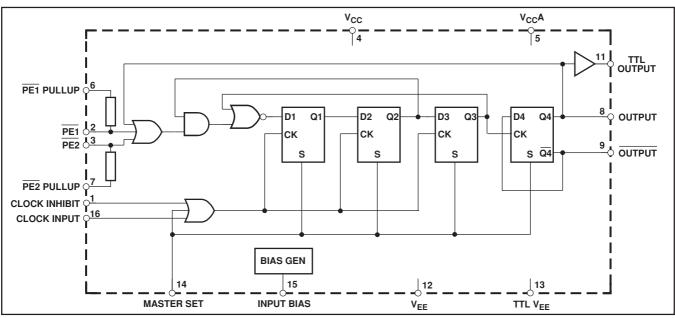


Fig. 2 Functional diagram

#### **ELECTRICAL CHARACTERISTICS**

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range ECL OPERATION

Supply voltage,  $V_{EE}$  = -4.75V to - 5.5V,  $V_{CC}$  = 0V Temperature,  $T_{_{AMB}}$  =  $-40^\circ C$  to  $+85^\circ C$ 

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.		Conditions	noice o
Maximum frequency (sinewave input)	f <sub>MAX</sub>	575		MHz	AC coupled clock = 350mV p-p	
Minimum frequency (sinewave input)	f <sub>MIN</sub>		10	MHz	AC coupled clock = 600mV p-p	5
Power supply current	I <sub>EE</sub>		105	mA	V <sub>EE</sub> = −5·5V, pins 6, 7, 13 o/c	
ECL output high voltage	V <sub>OH</sub>	-0.93	-0.78	V	$V_{EE} = -5.2V (25^{\circ}C), R_{L} = 100\Omega \text{ to } -2V$	
ECL output low voltage	V <sub>OL</sub>	-1.85	-1.62	V	$V_{EE} = -5.2V (25^{\circ}C), R_{L} = 100\Omega \text{ to } -2V$	
Input high voltage	V <sub>INH</sub>	-0.095	-0.81	V	$V_{EE} = -5.2V (25^{\circ}C)$	
Input low voltage	V <sub>INL</sub>	-1.85	-1.475	V	$V_{EE} = -5.2V (25^{\circ}C)$	
Input low currents	I <sub>IL</sub>	0.2		μA	25°C	
Input high current, clock and MS	I <sub>H</sub>		400	μA	$V_{IN} = -1.85V (25^{\circ}C)$	
Input high current, <u>PE1</u> and <u>PE2</u>	I <sub>H</sub>		400	μA	$V_{IN} = -0.8V (25^{\circ}C)$	
Propagation delay, clock to Q4 high	t <sub>pLH</sub>		3	ns	$R_L = 100\Omega$ to $-2V$ (25°C)	5
Propagation delay, MS to Q4 high	t <sub>pLH</sub>		6	ns	25°C	5
Modulus control set-up time	ts	4		ns	25°C	3, 5
Modulus control release time	tr	4		ns	25°C	4, 5
ECL output rise time (20% - 80%)	t <sub>ELH</sub>		2	ns	25°C	5
ECL output fall time (80% - 20%)	t <sub>EHL</sub>		2	ns	25°C	5

#### **TTL OPERATION**

Supply voltage,  $V_{CC} = V_{CC}A = 4.75V$  to 5.5V,  $V_{EE} = 0V$ Temperature,  $T_{AMB} = -40^{\circ}C$  to  $+85^{\circ}C$ 

Characteristic	Symbol	Value		Unito	Conditions	Notes
		Min.	Max.	- Units	Conditions	Notes
Maximum frequency (sinewave input)	f <sub>MAX</sub>	575		MHz	AC coupled clock = 350mV p-p	
Minimum frequency (sinewave input)	f <sub>MIN</sub>		10	MHz	AC coupled clock = 600mV p-p	5
Power supply current	I <sub>CC</sub>		111	mA	$V_{CC} = 5.5V$ , pins 6, 7 o/c, pin 13 to pin 12	
TTL output high voltage	V <sub>OH</sub>	2.3		V	$V_{CC} = 4.75V, I_{OH} = -640\mu A$	
TTL output low voltage	V <sub>OL</sub>		0.2	V	$V_{CC} = 5.5V, I_{OL} = -20\mu A$	
Input high voltage, <u>PE1</u> and <u>PE2</u>	V <sub>INH</sub>	3.9		V	$V_{CC} = 5.0V (25^{\circ}C)$	
Input low voltage, <u>PE1</u> and <u>PE2</u>	V <sub>INL</sub>		3.5	V	$V_{CC} = 5.0V (25^{\circ}C)$	
Input low current, <u>PE1</u> and <u>PE2</u>	I <sub>IL</sub>	-4		mA	$V_{CC} = 5.5V (25^{\circ}C)$ , pins 6, 7 = $V_{CC}$ ,	
					$V_{IN} = 0.4 V$	
Propagation delay, clock to TTL low	t <sub>pHL</sub>	6	14	ns	$V_{CC} = 5.0V (25^{\circ}C)$	5
Propagation delay, clock to TTL high	t <sub>pLH</sub>	6	14	ns	$V_{CC} = 5.0V (25^{\circ}C)$	5
Propagation delay, MS to TTL high	t <sub>p</sub>		17	ns	$V_{CC} = 5.0V (25^{\circ}C)$	5
Modulus control set-up time	t <sub>s</sub>	4		ns	$V_{CC} = 5.0V (25^{\circ}C)$	3, 5
Modulus control release time	t <sub>r</sub>	4		ns	$V_{\rm CC} = 5.0 V \ (25^{\circ} \rm C)$	4, 5
TTL output rise time (20% - 80%)	t <sub>TLH</sub>		5	ns	$V_{\rm CC} = 5.0 V \ (25^{\circ} \rm C)$	5
TTL output fall time (80% - 20%)	t <sub>THL</sub>		5	ns	$V_{CC} = 5.0V (25^{\circ}C)$	5

NOTES

1. The temperature coefficients of  $V_{OH} = +1.2mV/^{\circ}C$ ,  $V_{OL} = +0.25mV/^{\circ}C$  and of  $V_{IN} = +0.8mV/^{\circ}C$ . 2. The test configuration for dynamic testing is shown in Fig.6.

3. The set-up time  $t_s$  is defined as the minimum time that can elapse between L $\rightarrow$ H transition of control input and the next L $\rightarrow$ H clock pulse transition to ensure that the  $\div$ 10 mode is obtained.

The release time  $t_r$  is defined as the minimum time that can elapse between  $H \rightarrow L$  transition of control input and the next  $L \rightarrow H$  clock pulse transition 4. to ensure that the  $\div$ 11 mode is obtained.

5. Guaranteed but not tested.

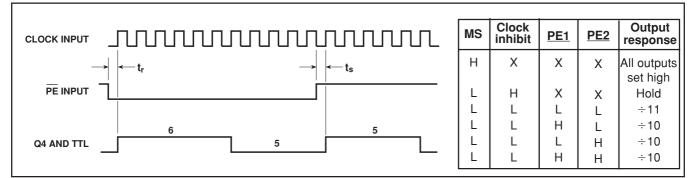


Fig. 3 Truth table and timing diagram

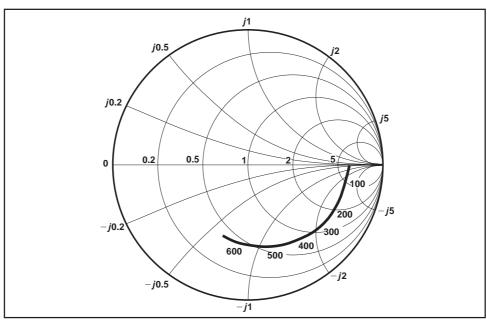


Fig. 4 Typical input impedance. Test conditions: Supply Voltage = 5V, Ambient Temperature =  $25^{\circ}$ C. Frequencies in MHz, impedances normalised to  $50\Omega$ .

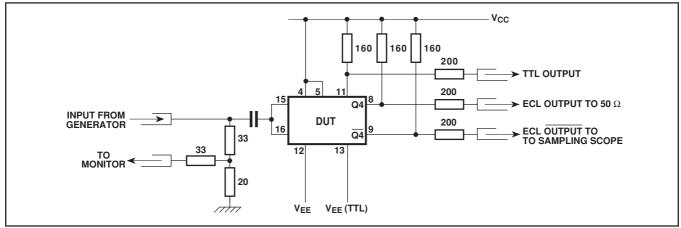


Fig. 5 Test circuit

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#### **OPERATING NOTES**

1. The clock input, which is ECL10K compatible throughout the temperature range, can also be coupled to TTL as shown in Fig. 8. The clock can also be capacitively coupled to the signal source (see Fig, 6). Connecting the internally-generated bias voltage to the clock input i.e., pin 15 to pin 16, centres the clock input about the switching threshold (see Fig.7).

2. The two complementary outputs are ECL10K compatible but internal pulldown resistors are not included and therefore external pulldown resistors to V<sub>EE</sub> are required. The outputs are capable of driving a 50Ωload to -2V over the temperature range -40°C to +85°C. The output high level will typically

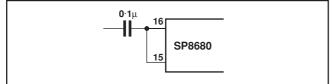


Fig. 6 AC coupled input

be reduced by 50mV.

3. The TTL totem pole output operates with the same supply and is powered up by connecting  $V_{EE}$  (pin 12) to TTL  $V_{EE}$  (pin 13). If the TTL output is not required then the TTL  $V_{EE}$  pin should be left open circuit, reducing the power consumption by 20mW, typically.

4. Both control inputs (<u>PE1</u> and <u>PE2</u>) are ECL10K compatible throughout the temperature range. Each control input is provided with pullup resistor, the remote ends of which are connected to pins 6 and 7, respectively. This allows the pullup resistors to be unused if so desired or to be used to interface from TTL (see Fig. 9). If interfacing to ECL is required then pins 6 and 7 should be left open circuit; alternatively, they can be connected to V<sub>EE</sub> to act as pulldown resistors. When high, the master set input sets the divider to the eleventh state, is asynchronous and overrides the clock input.

All the inputs have internal 50kΩ pulldown resistors.
The circuit will operate down to DC but inputslew rate

must be better than 20V/μs.

7. Input impedance is a function of frequency. See Fig. 5.

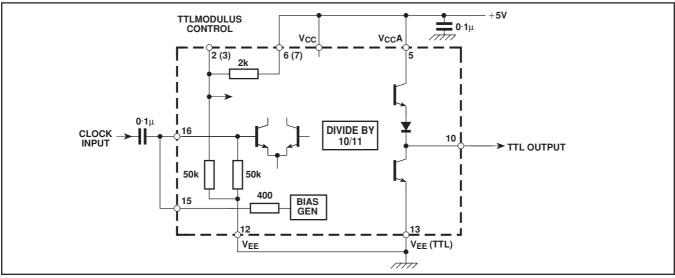


Fig. 7 Typical application showing TTL interfacing.

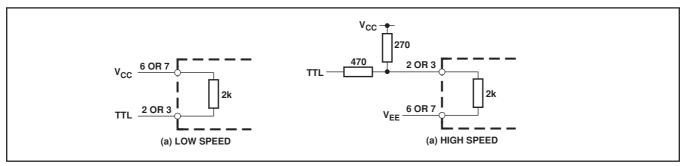
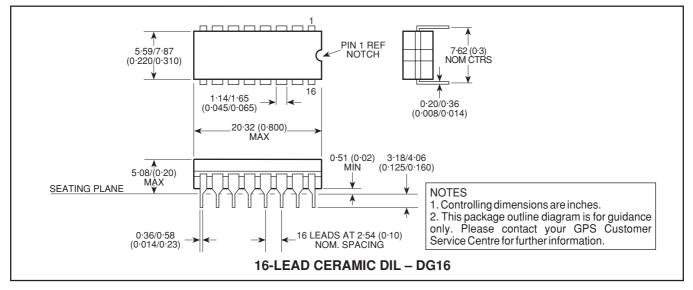


Fig. 8 TTL interface to PE1 and PE2

#### SP8680B

#### PACKAGE DETAILS

Dimensions are shown thus: mm (in).





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