MIC5002/5005/5007

4-Digit Counter/Display Decoder

Summary Information*

General Description

The MIC5002/5/7 is an ion-implanted, P-channel MOS, four-decade synchronous counter with latches, multiplexing circuits, and a read-only memory programmed for seven-segment outputs and BCD outputs. In addition, many on-chip control circuits provide flexibility of use with a minimum of external components.

The MIC5002/5/7 provides a means of counting up to 9999, transferring the count into latches without interrupting the counting operation, and supplying the latched information to the outputs one decade at a time. Scanning is controlled by the SCAN input which increments a one-of-four counter on its negative edge, thereby scanning the latches from MSD (Most Significant Digit) to LSD (Least Significant Digit).

Low-threshold voltages for input DTL/TTL compatibility are achieved through an ion-implementation process. Enhancement mode devices, as well as depletion-mode devices, are fabricated on the chip, allowing it to operate from a single +5V power supply. Depletion-mode technology also allows the entire circuit to operate on less than 25mW of power.

The block diagram, Figure 1, shows all options available on the MIC5002 MOS/LSI. Other members of this family which

Features

- Single-supply operation or double-supply for higher output drive
- Multiplexed seven-segment and/or BCD outputs
- TTL-compatible inputs
- Four decades of synchronous counting
- Minimum external component count
- Low power consumption

Ordering Information

Part Number	Temperature Range	Package
MIC5002CN	0°C to +70°C	28-Pin Plastic DIP
MIC5005CN	0°C to +70°C	24-Pin Plastic DIP
MIC5007CN	0°C to +70°C	16-Pin Plastic DIP

Functional Diagram

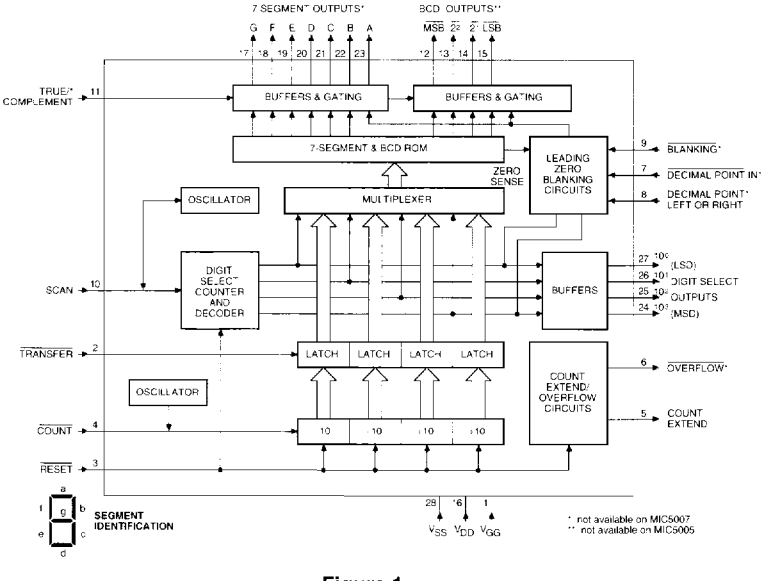

Figure 1

* Contact Micrel for more information.