

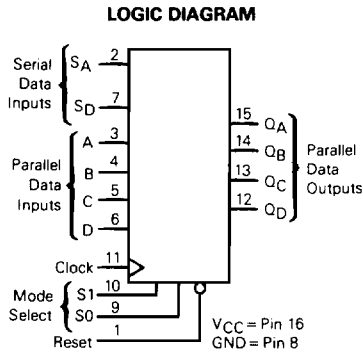
4-Bit Bidirectional Universal Shift Register

High-Performance Silicon-Gate CMOS

The MC54/74HC194 is identical in pinout to the LS194 and the MC14194B metal-gate CMOS device. The device inputs are compatible with standard CMOS outputs, with pull-up resistors, they are compatible with LSTTL outputs.

This static shift register features parallel load, serial load (shift right and shift left), hold, and reset modes of operation. These modes are tabulated in the Function Table, and further explanation can be found in the Pin Description section.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 164 FETs or 41 Equivalent Gates



MC54/74HC194



**J SUFFIX
 CERAMIC
 CASE 620-09**



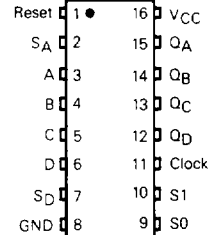
**N SUFFIX
 PLASTIC
 CASE 648-06**

ORDERING INFORMATION

MC74HCXXXN Plastic
 MC54HCXXXJ Ceramic

$T_A = -55^\circ$ to 125°C for all packages.
 Dimensions in Chapter 6.

PIN ASSIGNMENT



FUNCTION TABLE

Reset	Mode Select		Clock	Inputs				Outputs				Operating Mode		
	S1	S0		Serial Data		Parallel Data		QA	QB	QC	QD			
				SD	SA	A	B	C	D	QA	QB	QC	QD	
L	X	X	X	X	X	X	X	X	X	L	L	L	L	Reset
H	H	H	\nearrow	X	X	a	b	c	d	a	b	c	d	Parallel Load
H	L	H	\nearrow	X	H	X	X	X	X	H	QA _n	QB _n	QC _n	Shift Right
H	L	H	\searrow	X	L	X	X	X	X	L	QA _n	QB _n	QC _n	Shift Left
H	H	L	\nearrow	H	X	X	X	X	X	QB _n	QC _n	QD _n	H	Hold
H	H	L	\searrow	L	X	X	X	X	X	QB _n	QC _n	QD _n	L	Hold
H	L	L	X	X	X	X	X	X	X	no change	no change	no change	no change	Hold
H	X	X	L	X	X	X	X	X	X	no change	no change	no change	no change	Hold
H	X	X	H	X	X	X	X	X	X	no change	no change	no change	no change	Hold

H = high level (steady state)
 L = low level (steady state)
 X = don't care
 \nearrow = transition from low to high level.

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
 QA_n, QB_n, QC_n, QD_n = the level of QA, QB, QC, or QD, respectively, before the most-recent \nearrow transition of the clock.

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MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} + 1.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	± 20	mA
I _{out}	DC Output Current, per Pin	± 25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	± 50	mA
P _D	Power Dissipation in Still Air, Plastic or Ceramic DIP†	750	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: -10 mW/°C from 65° to 125°C

Ceramic DIP: -10 mW/°C from 100° to 125°C

For high frequency or heavy load considerations, see Chapter 4.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 1000 500 400	ns

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25°C to -55°C	≤ 85°C	≤ 125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{out} = 0.1 V or V _{CC} - 0.1 V I _{out} ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V _{OH}	Minimum High-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	6.0	5.9	5.9	5.9	
			6.0	5.48	5.34	5.20	
V _{OL}	Maximum Low-Level Output Voltage	V _{in} = V _{IH} or V _{IL} I _{out} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		V _{in} = V _{IH} or V _{IL} I _{out} ≤ 4.0 mA I _{out} ≤ 5.2 mA	6.0	0.1	0.1	0.1	
			6.0	0.26	0.33	0.40	
I _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	6.0	± 0.1	± 1.0	± 1.0	μA
			6.0	8	80	160	
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND I _{out} = 0 μA	6.0	8	80	160	μA

NOTE: Information on typical parametric values can be found in Chapter 4.

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AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q (Figures 1 and 4)	2.0	145	180	220	ns
		4.5	29	36	44	
		6.0	25	31	38	
t _{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 4)	2.0	150	190	225	ns
		4.5	30	38	45	
		6.0	26	33	38	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance	—	10	10	10	pF

NOTES:

1. For propagation delays with loads other than 50 pF, see Chapter 4.
2. Information on typical parametric values can be found in Chapter 4.

C _{PD}	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ For load considerations, see Chapter 4.	Typical @ 25°C, V _{CC} = 5.0 V	pF
		90	

TIMING REQUIREMENTS (Input t_r = t_f = 6 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25°C to -55°C	≤ 85°C	≤ 125°C	
t _{su}	Minimum Setup Time, Parallel Data Inputs to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _{su}	Minimum Setup Time, S1 or S2 to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _{su}	Minimum Setup Time, S _A or S _D to Clock (Figure 3)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t _h	Minimum Hold Time, Clock to any Input (except Reset) (Figure 3)	2.0	3	3	3	ns
		4.5	3	3	3	
		6.0	3	3	3	
t _{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	5	5	5	ns
		4.5	5	5	5	
		6.0	5	5	5	
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, Reset (Figure 2)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	

NOTE: Information on typical parametric values can be found in Chapter 4.

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PIN DESCRIPTIONS

DATA INPUTS

- A, B, C, D (PINS 3, 4, 5, 6)** — Parallel data inputs.
- S_A (PIN 2)** — Serial-data input when using shift-right mode.
- S_D (PIN 7)** — Serial-data input when using shift-left mode.

OUTPUTS

- Q_A, Q_B, Q_C, Q_D (PINS 15, 14, 13, 12)** — Parallel data outputs.

CONTROL INPUTS

CLOCK (PIN 11) — Clock Input. The shift register is completely static, allowing Clock rates down to DC in a continuous or intermittent mode.

RESET (PIN 1) — A low level applied to this pin resets all stages and forces all outputs low.

S₀, S₁ (PINS 9, 10) — Mode-select inputs. These inputs control the mode of operation as described in the function table and below.

Parallel Load Mode (S₁ = H, S₀ = H) — Data is loaded into the device with a positive transition of the Clock input.

Shift Right Mode (S₁ = L, S₀ = H) — With a positive transition of the Clock input, each bit is shifted right (in the direction Q_A toward Q_D) one stage and data on the S_A Serial Data Input is shifted into stage A.

Shift Left Mode (S₁ = H, S₀ = L) — With a positive transition of the Clock input, each bit is shifted left (in the direction Q_D toward Q_A) one stage and data on the S_D Serial Data Input is shifted into stage D.

Hold Mode (S₁ = L, S₀ = L) — Outputs are held.

SWITCHING WAVEFORMS

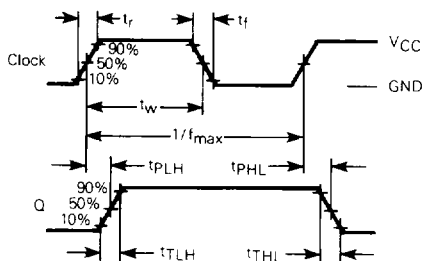


Figure 1.

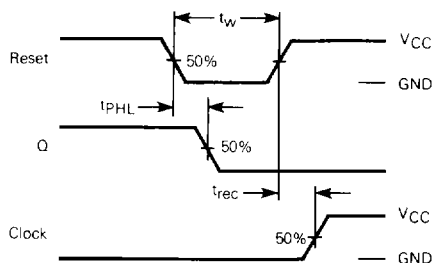


Figure 2.

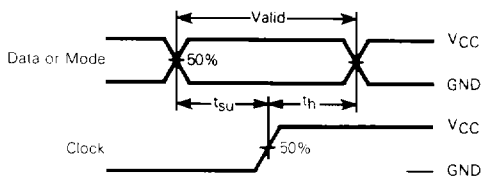
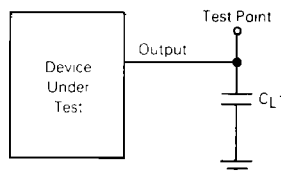


Figure 3.

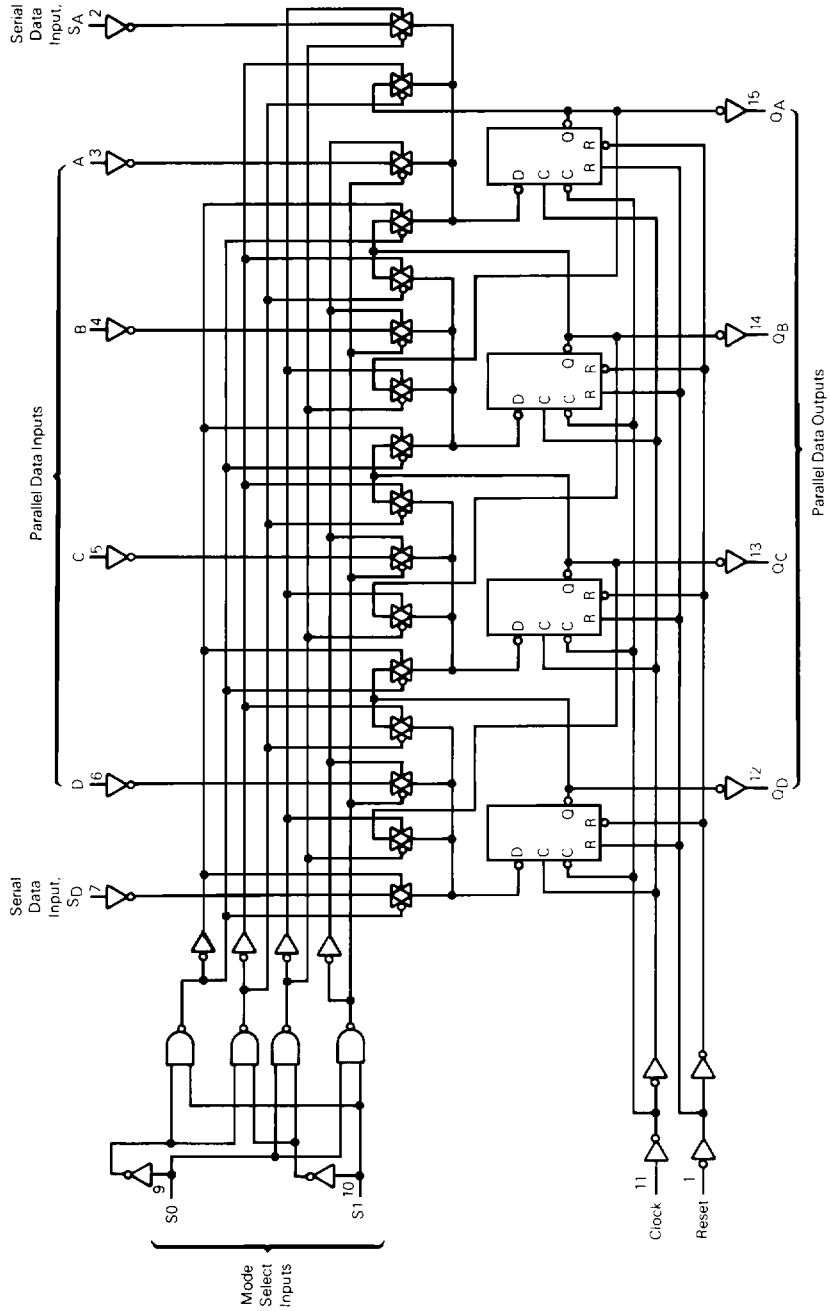


* Includes all probe and jig capacitance

Figure 4. Test Circuit

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EXPANDED LOGIC DIAGRAM



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TIMING DIAGRAM

