Ordering number : EN5775A

SANYO Semiconductors
DATA SHEET

LA7477W — Monolithic Linear IC For Digital Video Camera Audio Signal I/O Interface IC

Overview

The LA7477W is a digital video camera audio signal I/O interface IC that integrates on a single chip a block previous implemented with discrete components. The LA7477W integrates the volume control circuit used for both headphones and speakers, and thus supports the implementation of circuit structures ideal for digital video cameras that include an LCD panel.

Features

- Three-wire serial bus control
- Headphone and speaker volume controls (Support for both serial and parallel operation)
- Supports bilingual audio
- Supports record, playback, and overdubbing
- Low-power mode

Functions

- Three inputs (microphone, line 1, line 2)
- ALC (That can be turned on or off)
- Fader circuit
- Low-pass filter (used for both record and playback)
- Electronic volume control circuit
- Deemphasis circuit
- Left + right channel mixer
- Power muting function

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Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC}		7	V
Allowable power dissipation	Pd max	Ta ≤ 75°C	200	mV
Operating temperature	Topr		-10 to +75	°C
Storage temperature	Tstg		-55 to +150	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	$V_{CC}1$		3.15	V
	$V_{CC}2$		4.75	V
Operating supply voltage range	$V_{CC}1$ opg		3.0 to 3.6	V
	$V_{CC}2$ opg		4.5 to 5.5	V

Electrical Characteristics at Ta = 25°C, $V_{CC}1$ = 3.15V, $V_{CC}2$ = 4.75V, f = 1kHz, Lch, Rch, EVR ; CENTER

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Record current 1	$I_{CC}3R1$	V_{CC} (L) = 3.15V, REC	13.3	17.8	22.3	mA
Record current 2	$I_{CC}5R2$	V_{CC} (H) = 4.75V, REC	4.1	5.5	6.9	mA
Playback current 1	$I_{CC}3P1$	V_{CC} (L) = 3.15V, PB	6.9	9.3	11.7	mA
Playback current 2	$I_{CC}5P2$	V_{CC} (H) = 4.75V, PB	4.1	5.5	6.9	mA
Line output reference level	V_{OL}	V_{IN} (MIC) = -40dBV, V_{IN} (LINE1, 2) = -30dBV	-11	-10	-9	dBV
Line output left/right level difference (THD)	V_{OLD}	V_{IN} (MIC) = -40dBV, V_{IN} (LINE1, 2) = -30dBV		0	±1	dB
Line output total harmonic distortion	V_{OLTHD}	V_{IN} (MIC) = -40dBV, V_{IN} (LINE1, 2) = -30dBV		0.1	0.3	%
Line output noise voltage 1	$V_{NOL}1$	MIC IN MODE, ALC-ON, Rg = 1k, JIS-A FILTER		-73	-70	dBV
Line output noise voltage 2	$V_{NOL}2$	MIC IN MODE, ALC-OFF, Rg = 1k, JIS-A FILTER		-79	-76	dBV
Line output noise voltage 3	$V_{NOL}3$	LINE1, 2 IN MODE, ALC-ON, Rg = 1k, JIS-A FILTER		-83	-80	dBV
Line output noise voltage 4	$V_{NOL}4$	LINE1, 2 IN MODE, ALC-OFF, Rg = 1k, JIS-A FILTER		-87	-84	dBV
Line output ALC level	V_{OLa}	V_{IN} (MIC) = -30dBV, V_{IN} (LINE1, 2) = -20dBV	-4.5	-3.0	-1.5	dBV
Line output ALC (20dB boost) harmonic distortion (THD)	V_{OLaT}	V_{IN} (MIC) = -20dBV		0.2	0.5	%
Record output reference level	V_{OR}	V_{IN} (MIC) = -40dBV, V_{IN} (LINE1, 2) = -30dBV	-18	-17	-16	dBV
Record output left/right level difference	$V_{ORD}1$	V_{IN} (MIC) = -40dBV, V_{IN} (LINE1, 2) = -30dBV		0	±1	dB
Record output total harmonic distortion (THD)	V_{ORTHD}	V_{IN} (MIC) = -40dBV, V_{IN} (LINE1, 2) = -30dBV		0.1	0.3	%
Record output noise voltage 1	$V_{NOR}1$	MIC IN MODE, ALC-ON, Rg = 1k, JIS-A FILTER		-81	-78	dBV
Record output noise voltage 2	$V_{NOR}2$	MIC IN MODE, ALC-OFF, Rg = 1k, JIS-A FILTER		-86	-83	dBV
Record output noise voltage 3	$V_{NOR}3$	LINE1, 2 IN MODE, ALC-ON, Rg = 1k, JIS-A FILTER		-91	-88	dBV
Record output noise voltage 4	$V_{NOR}4$	LINE1, 2 IN MODE, ALC-OFF, Rg = 1k, JIS-A FILTER		-96	-93	dBV
Record output ALC level	V_{ORa}	V_{IN} (MIC) = -30dBV, V_{IN} (LINE1, 2) = -20dBV	-11.5	-10.0	-8.5	dBV
Record output maximum output level	V_{ORMAX}	ALC-OFF, V_{IN} (MIC, LINE1, 2) at REC OUT THD = 1%	-4			dBV
Record forward/reverse output level difference	$V_{ORD}2$	V_{IN} (MIC) = -40dBV, V_{IN} (LINE1, 2) = -30dB		0	±0.2	dB
Record forward/reverse output DC offset	V_{OROFF}	No signal		0	±7	mV

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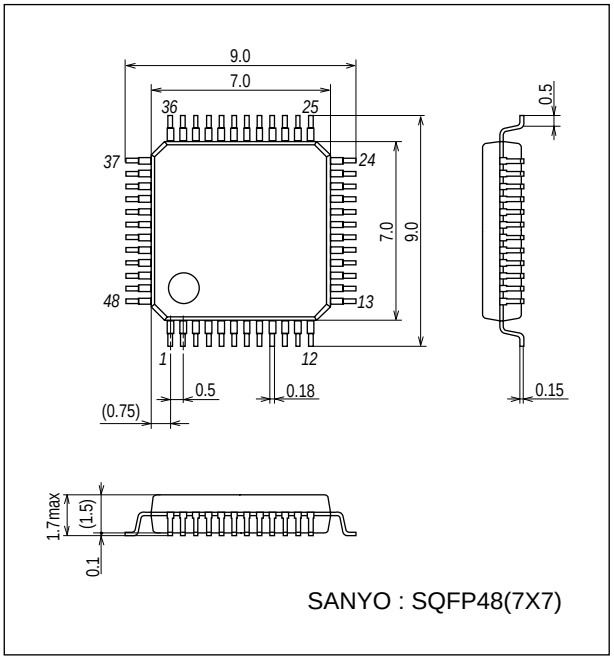
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Maximum input level	V_{IN} max	ALC-ON, V_{IN} (MIC, LINE1, 2) at LINE OUT THD = 1%	-5			dBV
Line maximum output level	V_{OL} max	ALC OFF at LINE OUT THD = 1%	2.5	3.5		dBV
Line muting attenuated output	V_{OMUTE}	V_{IN} (MIC) = -25dBV, JIS-A FILTER		-75	-73	dBV
Fader output at maximum attenuation	V_{OFADE}	V_{IN} (MIC) = -40dBV, JIS-A FILTER			-71	dBV
Record first-order low-pass filter frequency characteristics 1	$V_{RLPF}1$	V_{IN} (MIC) = -40dBV, the 20kHz/1kHz ratio		-0.5	-1.0	dB
Record first-order low-pass filter frequency characteristics 2	$V_{RLPF}2$	V_{IN} (MIC) = -40dBV, the 200kHz/1kHz ratio	-3.5	-5.0		dB
Inter-input crosstalk	IN_{CR}	V_{IN} (LINE1, 2) = -30dBV, MIC IN MODE, Rg = 1k, JIS-A FILTER		-75	-71	dBV
		V_{IN} (MIC) = -40dBV, V_{IN} (LINE1) = -30dBV, LINE2 IN MODE, Rg = 1k, JIS-A FILTER		-85	-81	dBV
		V_{IN} (MIC) = -40dBV, V_{IN} (LINE2) = -30dBV, LINE1 IN MODE, Rg = 1k, JIS-A FILTER		-85	-81	dBV
Headphone output level	V_{OHP}	V_{IN} (MIC) = -40dBV, EVR CENTER, 8Ω termination for a 47+8Ω load.	-38	-35	-32	dBV
Headphone output left/right level difference	V_{HPD}	V_{IN} (MIC) = -40dBV, EVR CENTER, 8Ω termination for a 47+8Ω load.		0	±2	dB
Headphone output harmonic distortion (THD)	V_{OHPD}	V_{IN} (MIC) = -40dBV, EVR CENTER, 8Ω termination for a 47+8Ω load.		0.2	0.5	%
EVR maximum fluctuation	E_{VR} max	V_{IN} (MIC) = -40dBV, EVR CENTER→MAX	10	12		dB
EVR minimum fluctuation	E_{VR} min	V_{IN} (MIC) = -40dBV, EVR CENTER→MIN		-70	-60	dB
Speaker output reference level	V_{OSP}	V_{IN} (MIC) = -40dBV, EVR CENTER	-21	-18	-15	dBV
Speaker output harmonic distortion (THD)	V_{OSPD}	V_{IN} (MIC) = -40dBV, EVR CENTER		0.1	0.3	%
Playback line output level	V_{OPB}	PB_{IN} = -21dBV	-10.5	-10.0	-9.5	dBV
Playback third-order low-pass filter frequency characteristics 1	$V_{PLPF}1$	PB_{IN} = -21dBV, the 20kHz/1kHz ratio		0	-1	dB
Playback third-order low-pass filter frequency characteristics 2	$V_{PLPF}2$	PB_{IN} = -21dBV, the 50kHz/1kHz ratio	-5	-9		dB
Inter-channel crosstalk	$CH_{CR}1$	V_{IN} (MIC) = -40dBV, (Rch/Lch) Rg = 1k (Lch/Rch), ALC-ON, LINE OUT, JIS-A FILTER		-70	-68	dBV
	$CH_{CR}2$	V_{IN} (MIC) = -40dBV, (Rch/Lch) Rg = 1k (Lch/Rch), ALC-OFF, LINE OUT, JIS-A FILTER		-76	-74	dBV
	$CH_{CR}3$	V_{IN} (LINE1, 2) = -30dBV, (Rch/Lch) Rg = 1k (Lch/Rch), ALC-ON, LINE OUT, JIS-A FILTER		-80	-78	dBV
	$CH_{CR}4$	V_{IN} (LINE1, 2) = -30dBV, (Rch/Lch) Rg = 1k (Lch/Rch), ALC-OFF, LINE OUT, JIS-A FILTER		-86	-84	dBV

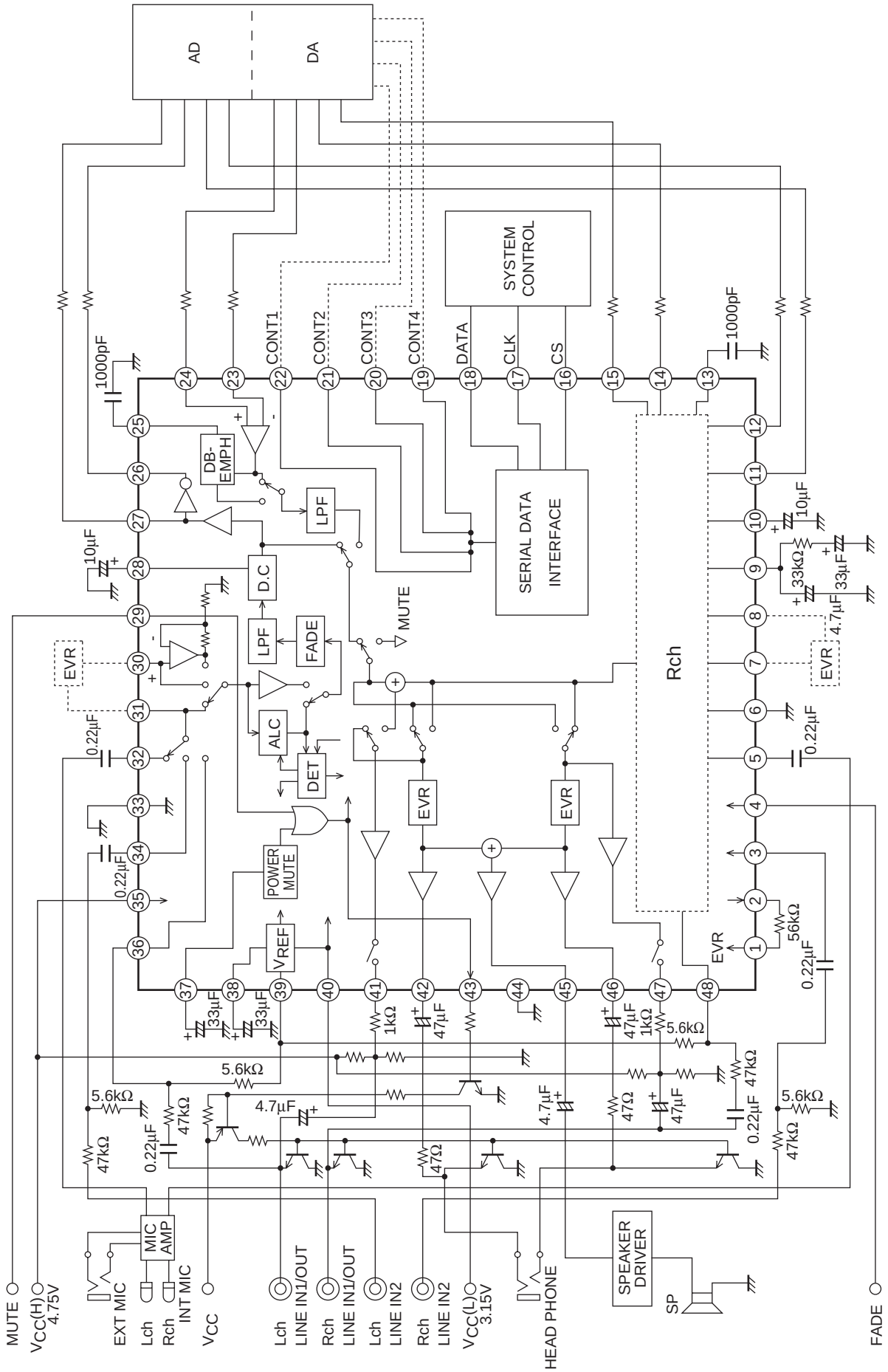
Package Dimensions

unit : mm (typ)

3163B



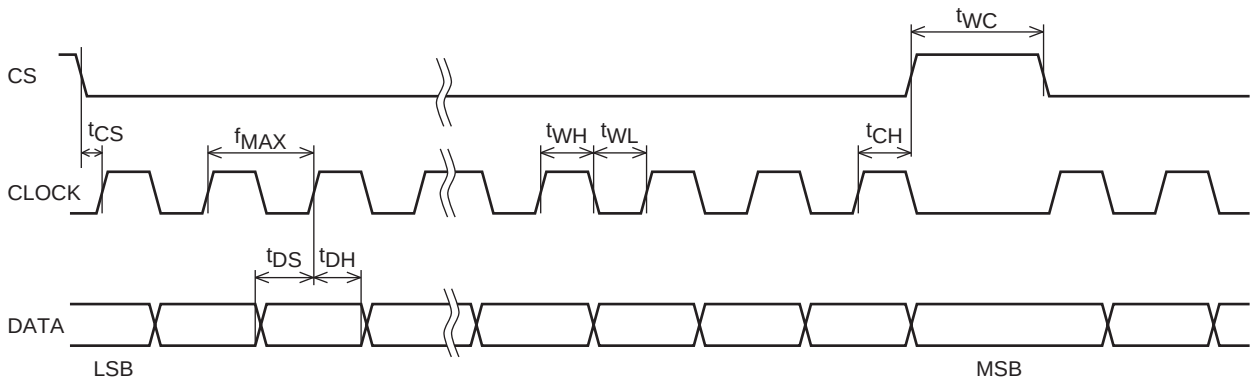
Block Diagram



Serial Communications

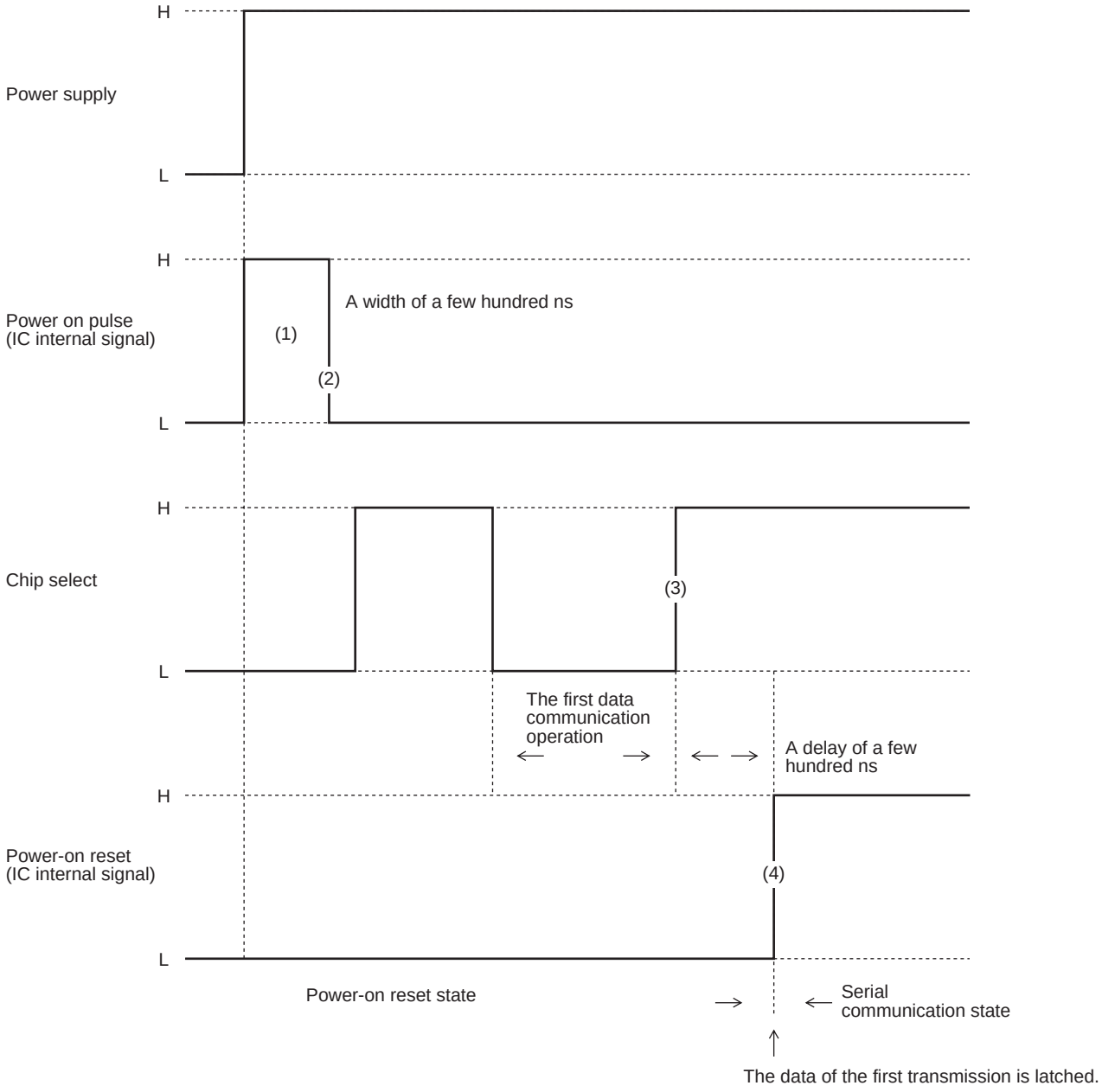
Serial data	Parameter		Initial values
Bit 1	EVR CTL 1	L : 0, H : 1	0
Bit 2	EVR CTL 2	L : 0, H : 1	0
Bit 3	EVR CTL 3	L : 0, H : 1	0
Bit 4	EVR CTL 4	L : 0, H : 1	0
Bit 5	EVR CTL 5	L : 0, H : 1	0
Bit 6	Headphone and speaker	ON : 0, OFF : 1	1
Bit 7	EVR SERIAL	ON : 0, OFF : 1	1
Bit 8	12dB amplifier through state	OFF : 0, ON : 1	1
Bit 9	REC EVR SW	OFF : 0, ON : 1	0
Bit 10	DE-EMPH	OFF : 0, ON : 1	0
Bit 11	CONT1 OUT	L : 0, H : 1	1
Bit 12	CONT2 OUT	L : 0, H : 1	1
Bit 13	CONT3 OUT	L : 0, H : 1	1
Bit 14	CONT4 OUT	L : 0, H : 1	1
Bit 15	RFU SW	OFF : 0, ON : 1	0
Bit 16	STEREO/MAIN/SUB	STEREO : 0, MAIN : 0, SUB : 1	0
Bit 17		STEREO : 0, MAIN : 1, SUB : 0	0
Bit 18	ALC SW	ON : 0, OFF : 1	0
Bit 19	LINE OUT	ON : 0, OFF : 1	0
Bit 20	MIC/LINE1/LINE2/SPEAKER OFF	MIC : 0, LINE1 : 0, LINE2 : 1, SPEAKER OFF : 1	0
Bit 21		MIC : 0, LINE1 : 1, LINE2 : 0, SPEAKER OFF : 1	0
Bit 22	MUTE SW	OFF : 0, ON : 1	1
Bit 23	REC/PB/EE/POWER SAVE	REC : 0, PB : 0, EE : 1, POWER SAVE : 1	0
Bit 24		REC : 0, PB : 1, EE : 0, POWER SAVE : 1	0

Serial Transfer Timing



Maximum clock frequency	f_{MAX}	800kHz
Clock pulse width (low)	t_{WL}	625ns minimum
Clock pulse width (high)	t_{WH}	625ns minimum
Chip enable setup time	t_{CS}	625ns minimum
Chip enable hold time	t_{CH}	625ns minimum
Data setup tim	t_{DS}	625ns minimum
Data hold time	t_{DH}	625ns minimum
Chip enable pulse width	t_{WC}	625ns minimum

Power on state (serial communication)



The power-on reset state lasts from the rise of the power on pulse (1) created internally in the IC at power on to the second chip select signal rising edge (3) that is input after (2). However, since there is actually a delay of a few hundred ns internally in the IC the first data state starts at (4) and the IC enters the normal serial communication state after (4).

Headphone, Speaker, and Line Out Output States

MODE	Serial data			Output		
	Bit 6	Bit 23	Bit 24	Headphone	Speaker	Line out
REC	0	0	0	ON	ON	*2
PB	0	0	1	ON	ON	*2
EE	0	1	0	ON	ON	*2
POWER SAVE	*1	1	1	OFF	OFF	OFF
Headphone and speaker switches	1	*1	*1	OFF	OFF	*2

Notes. *1 : These are don't care states.

*2 : In states other than power saving mode, this state does not depend on bits 6, 23, and 24 in the data, but rather is controlled by bit 19 in the data.

Furthermore, the speaker output can be controlled by bits 20 and 21 in the serial data, and has the logic shown below in each mode. However, note that the input selector goes to microphone mode if bits 20 and 21 are (1, 1).

The table below lists the speaker output control logic in each mode.

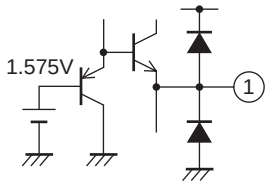
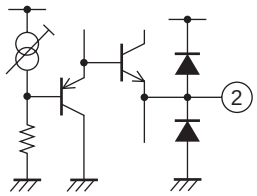
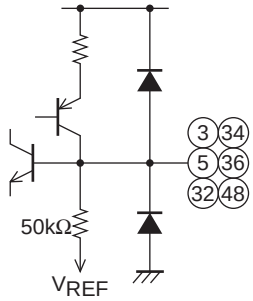
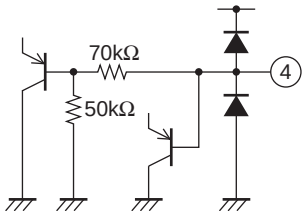
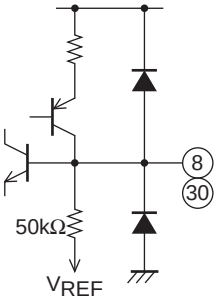
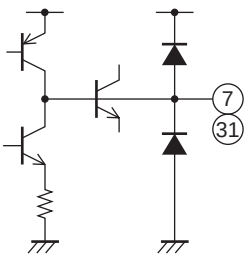
Serial data		REC	PB	EE	POWER SAVE
Bit 20	Bit 21				
0	0	ON	ON	ON	OFF
0	1	ON	ON	ON	OFF
1	0	ON	ON	ON	OFF
1	1	OFF	OFF	OFF	OFF

Note than in record mode, if bits 20 and 21 are (0, 0), care is require when using this IC, since the speakers will be turned on at the same time as the system switches to microphone mode.

Output Signal Table

Serial data			Output				
Bit 15	Bit 16	Bit 17	Line Left channel	Headphone Left	Speaker	Headphone Right	Line Right channel
0	0	0	L	L	L + R	R	R
1	0	0	L + R	L	L + R	R	R
0	0	1	L	L	L	L	L
1	0	1	L + R	L	L	L	L
0	1	0	R	R	R	R	R
1	1	0	L + R	R	R	R	R

Pin Functions

Pin No.	Pin Name	DC voltage	AC voltage	Description	Equivalent circuit
1	EVR CTL IN	1.575V		Controls the EVR. This pin can be used for external control by applying a voltage through an external resistor. This IC can also be controlled from serial data by connecting this pin to pin 2 through an external resistor.	
2	EVR CTL SERIAL OUT			Control output when EVR is controlled by serial data	
3 5 32 34 36 48	LINE IN2 R MIC IN R MIC IN L LINE IN2 L LINE IN1 L LINE IN1 R	1.80V	-30dBV -40dBV -40dBV -30dBV -30dBV -30dBV (Reference inputs)	Right channel line 2 input Right channel microphone input Left channel microphone input Left channel line 2 input Left channel line 1 input Right channel line 1 input	
4	FADE IN			Controls the fade characteristics	
6 33 44	GND R GND L GND LINE			Right channel ground Left channel ground Line input ground	
8 30	EXT EVR OUT R EXT EVR OUT L			Connect to the right channel external EVR output. Connect to the left channel external EVR output.	
7 31	EXT EVR IN R EXT EVR IN L	1.80V	-40dBV (Microphone mode) -30dBV (Line mode)	Connect to the right channel external EVR input. Connect to the left channel external EVR input.	

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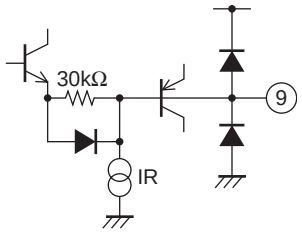
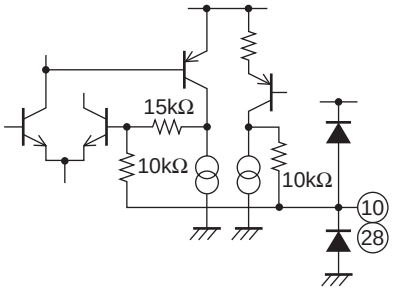
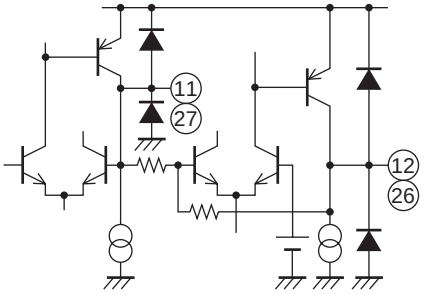
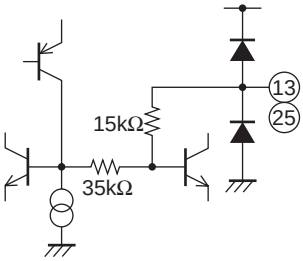
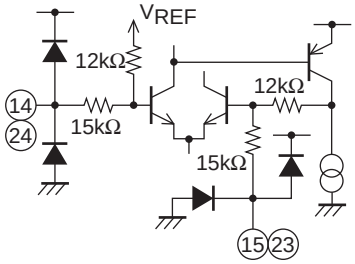
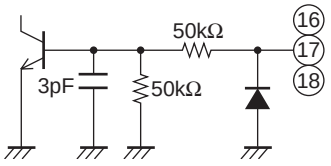
Pin No.	Pin Name	DC voltage	AC voltage	Description	Equivalent circuit
9	ALC DET			ALC detection IR (MIC) ≈ 1.8μA IR (LINE) ≈ 0.5μA	
10 28	DC DET R DC DET L	1.80V		Detects the DC level and cancels the offset.	
11 12 26 27	REC OUT + R REC OUT - R REC OUT - L REC OUT + L	1.80V	-17dBV (Reference inputs)	Right channel record output + phase Right channel record output - phase Left channel record output - phase Left channel record output + phase	
13 25	DE-EMPHASIS R DE-EMPHASIS L	1.80V		Deemphasis control	
14 15 23 24	AMP + IN R AMP - IN R AMP - IN L AMP + IN L	1.80V		Right channel playback + phase input Right channel playback - phase input Left channel playback - phase input Left channel playback + phase input	
16 17 18	CHIP SELECT IN CLOCK IN DATA IN			Chip select input Clock input Data input	

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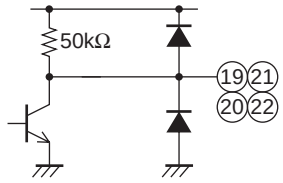
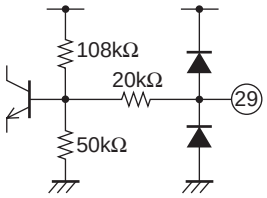
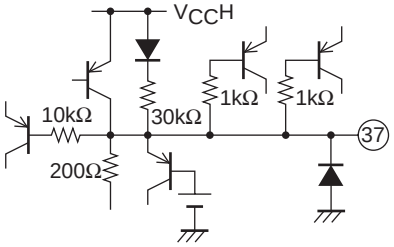
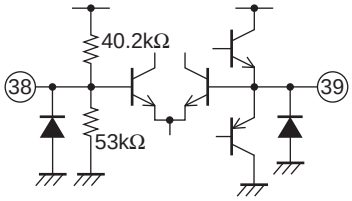
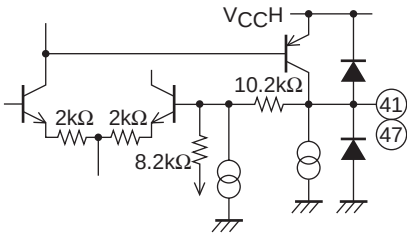
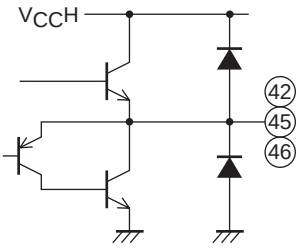
Pin No.	Pin Name	DC voltage	AC voltage	Description	Equivalent circuit
19 20 21 22	CONT4 CONT3 CONT2 CONT1			CONT outputs	
29	MUTE CTL			Muting control 2.3V or higher: Muting on 0.7V or lower: Muting off	
35	$V_{CC}H$	4.75V			
37	POWER MUTE			Used to temporarily set the IC to the muted state when power is applied or removed.	
38 39	V_{REF} V_{REF} OUT	1.80V 1.80V		Ripple rejection filter connection V_{REF} output	
40	$V_{CC}L$	3.15V			
41 47	LINE OUT L LINE OUT R	2.375V	-10dBV (Reference inputs)	Left channel line output Right channel line output	
42 45 46	HEADPHONE L SPEAKER OUT HEADPHONE R	2.375V	-35dBV -18dBV -35dBV (Reference inputs)	Left channel headphone output Speaker output Right channel headphone output	
43	POWER MUTE OUT			Muting control output used when power is applied or removed.