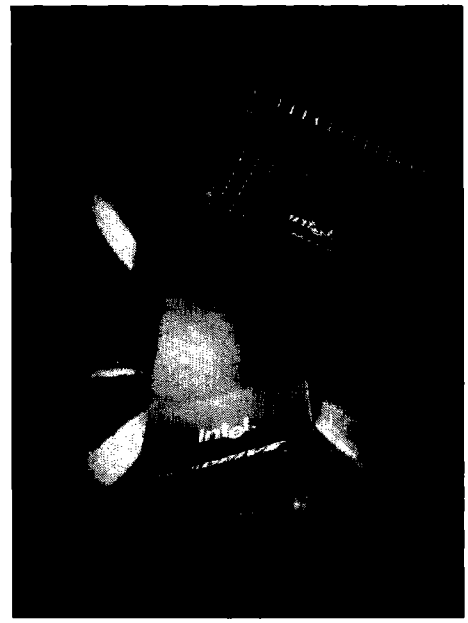
INTEL OverDrive™ PROCESSORS

- **Powerful Performance Boosters for Intel486™ Microprocessor-Based Systems**
  - **— Improve Overall System Performance by up to 70%**
  - **— Increase Both Integer and Floating-Point Performance**
  - **— Provides Next Level of CPU Performance**
- **Intel486 DX2 OverDrive Processors Upgrade Systems Based on**
  - **— Intel486™ SX CPUs**
  - **— Intel486™ DX CPUs**
- **Binary Compatible with Large Installed Software Base**
  - **— MS-DOS*, OS/2*, Windows***
  - **— UNIX* System V/386**
  - **— iRMX®, iRMK Kernals**



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Intel OverDrive processors are powerful, single-chip upgrades for Intel486 microprocessor-based systems. The Intel486 DX2 OverDrive processor upgrades Intel486 SX and DX CPU-based systems with Intel486 DX2's "speed doubling" technology. OverDrive processors accelerate integer and math performance, delivering an overall performance boost of up to 70 percent. Users see a performance boost for all DOS, Windows, OS/2 and UNIX applications from AutoCAD* to WordPerfect*.

*Other brands and names are the property of their respective owners.

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Intel OverDrive™ Processors

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CONTENTS

1.0 INTRODUCTION

This data sheet describes the Intel486 DX2 OverDrive processor. The Intel486 DX2 OverDrive processor is designed as an end-user upgrade for Intel486 SX and Intel486 DX CPU-based systems. This data sheet is intended to be used with the data sheet for the original CPU in the system—the Intel486 SX or Intel486 DX CPU—which describes the Intel486 Family Architecture and functionality. All enhancements or differences in the Intel486 DX2 OverDrive processor from the Intel486 SX or Intel486 DX CPU are described in this data sheet. Intel486 SX or Intel486 DX CPU-based systems that are compatible to the Intel OverDrive processor must be designed to both the original CPU specifications and the Intel OverDrive processor specifications.

1.1 Product Overview

The Intel486 DX2 OverDrive processor is based on Intel486 DX2 Microprocessor technology. Intel OverDrive processor are designed as a single-chip, powerful performance booster for Intel486 Microprocessor-based systems.

The Intel486 DX2 OverDrive processor is currently available in two basic product variants. The first product variant (ODP), shown in Figures 1A and 1B, is referred to as the OverDrive processor for Intel486 SX and DX CPU-based systems that have an OverDrive processor socket. This product, ODP, is described specifically in Section 1.2.

The second i486 DX2 OverDrive processor variant (ODPR), shown in Figure 1C, is referred to as the OverDrive processor for Intel486 DX CPU-based systems that do not have an OverDrive processor socket. This product is designed to replace the Intel486 DX CPU in systems that do not have an "End-User Easy" OverDrive processor socket. Section 1.3 describes this product variant, ODPR.

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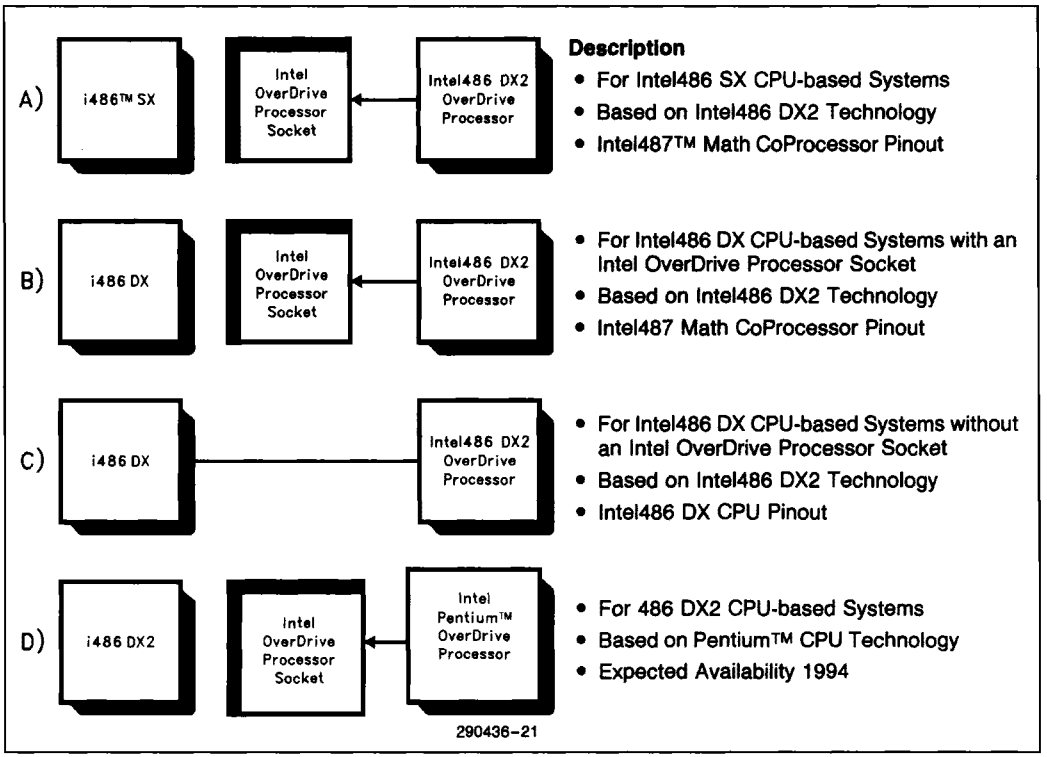

1.2 Intel486 DX2 OverDrive™ Processor for Intel486™ SX and DX Microprocessor-Based Systems (with an OverDrive™ Processor Socket)

- **Powerful Performance Booster for Intel486™ SX and DX CPU-Based Systems**
  - **Improves Overall System Performance by up to 70%**
  - **Increases Both Integer and Floating-Point Performance**
- **169-Lead Pin Grid Array Package**
  - **Pin Compatible with Intel487™ SX Math CoProcessor**
  - **"End-User Easy", Single-Chip Upgrade**
  - **169th Alignment Pin Ensures Proper Chip Orientation**
- **Math CoProcessor Included On-Chip**
- **High Integration Enables On-Chip**
  - **8 Kbyte Code and Data Cache**
  - **Floating Point Unit**
  - **Paged, Virtual Memory Management**
- **Utilizes Intel486™ DX2 Speed-Doubling Technology**
  - **CPU Core Runs at Twice the Frequency of the System Bus**
  - **Compatible with 33, 25, 20, and 16 MHz Systems**
- **Binary Compatible with Large Installed Software Base**
  - **MS-DOS, OS/2, Windows**
  - **UNIX System V/386**
  - **iRMX®, iRMK Kernals**
- **High Performance Design**
  - **Core Clock Speed up to 66 MHz**
  - **106 Mbyte/sec Burst Bus**
  - **CHMOS V Process Technology**
- **Complete 32-Bit Architecture**
  - **Address and Data Busses**
  - **Registers**
  - **8-, 16-, 32-Bit Data Types**
- **Compatible with Intel SL Enhanced Features**

The Intel486 DX2 OverDrive processor for Intel486 SX and DX microprocessor-based personal computers is a powerful, single-chip upgrade that is intrinsically cost effective and that offers excellent price/performance. Based on Intel486 DX2 technology, the Intel OverDrive processor integrates an integer unit, a floating point unit, a memory management unit, SL Enhanced features, and an 8 Kbyte cache on a single chip.

Using the Intel486 DX2's "speed doubling" technology, the Intel OverDrive processor operates internally at twice the speed of the system bus. This allows users of Intel486 SX and DX microprocessor-based systems to double the frequency of their computer's CPU by adding a single chip, without upgrading or modifying any other system components. For example, adding an Intel 486 DX2 OverDrive processor to an Intel486 DX 33 MHz system will double the CPUs internal operating speed to 66 MHz. Depending on the application, the OverDrive processor can provide an overall system performance boost of up to 70%.

The Intel486 DX2 OverDrive processor (ODP) is designed to be installed in the OverDrive processor socket of Intel486 microprocessor-based systems. In Intel486 SX systems, this is the same socket that was designed for the Intel487™ SX Math CoProcessor.

The Intel486 DX2 OverDrive processor is available in three product versions. The 20 MHz Intel OverDrive processor is designed to upgrade both 20 MHz and 16 MHz Intel486 SX Microprocessor-based systems. This product utilizes the standard 169-lead PGA package. The 25 MHz and 33 MHz Intel OverDrive processor is designed to upgrade 25 MHz and 33 MHz Intel486 SX or DX Microprocessor-based systems. This product has a heat sink attached to the standard 169-lead PGA package to aid in the heat dissipation in 25 MHz and 33 MHz systems.

1.2.1 Pinout

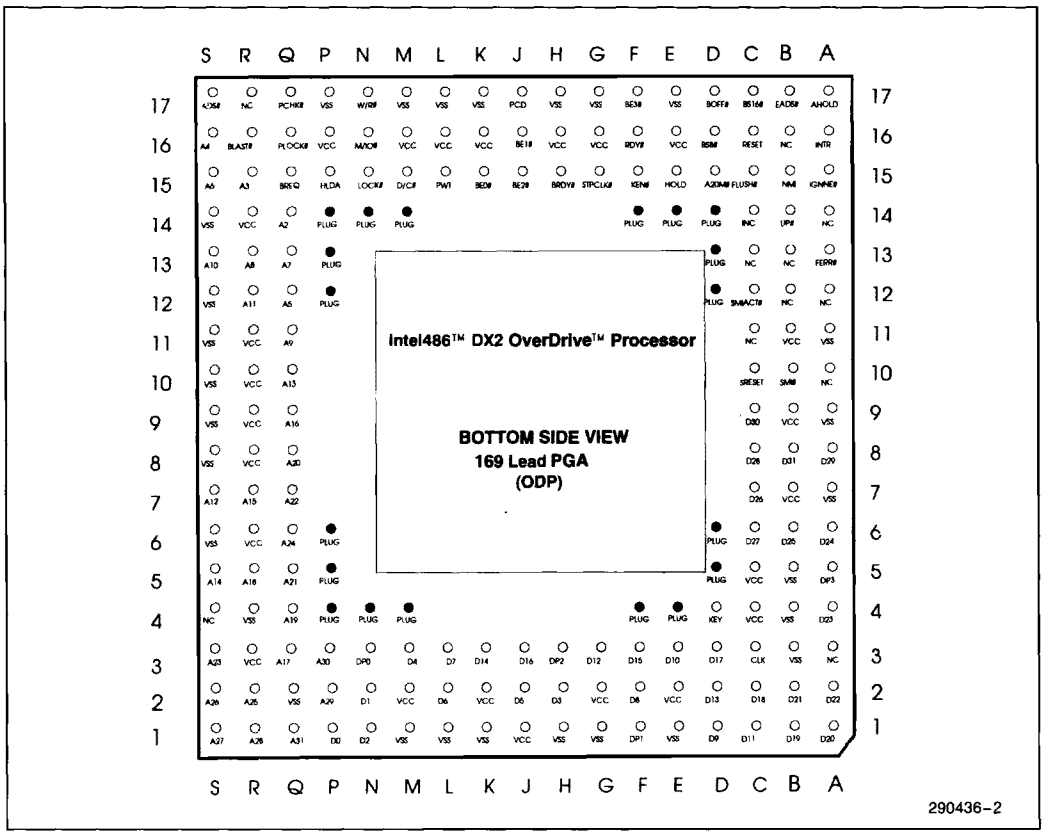

Figure 1.2.1

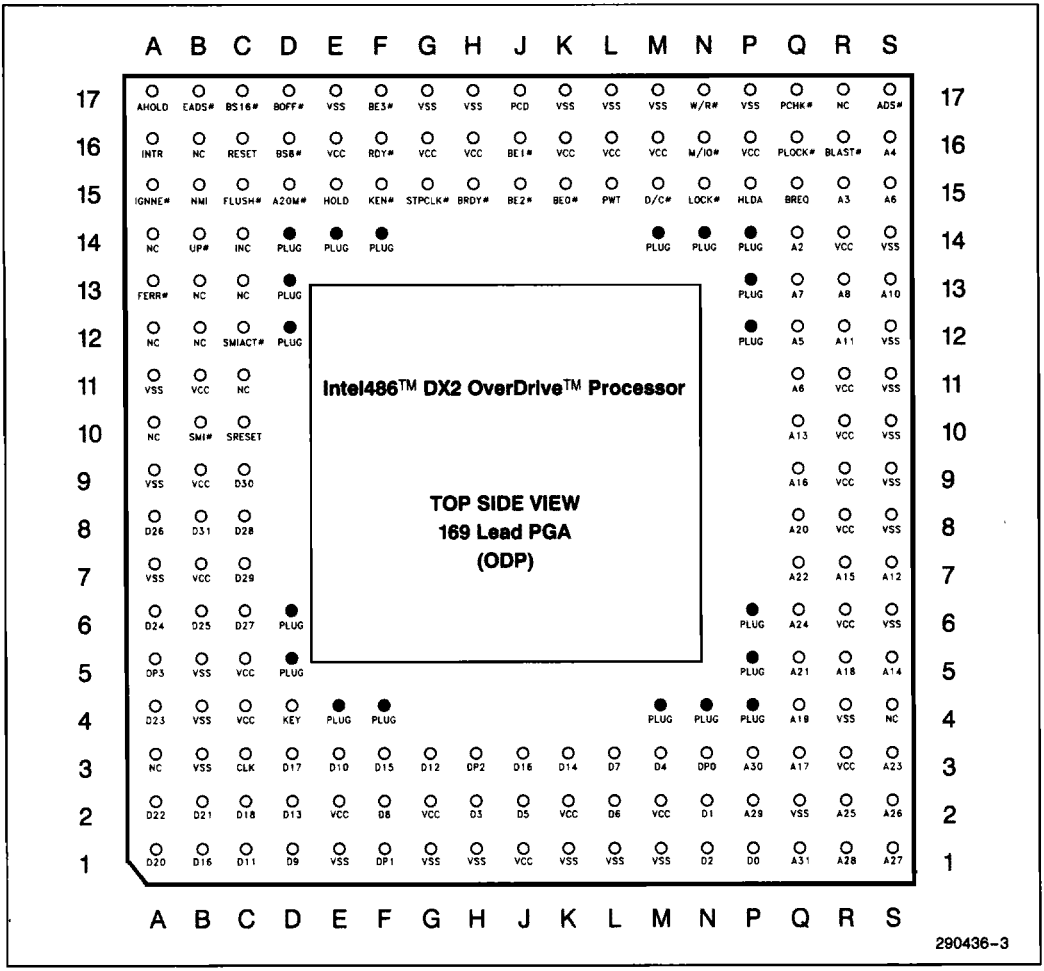
A B C D E F G H J K L M N P Q R S
17 AHOLD EADS# BS16# BOFF# VSS BE3# VSS VSS PCD VSS VSS VSS W/R# VSS PCHK# NC ADS#
16 INTR NC RESET BS8# VCC RDY# VCC VCC BE1# VCC VCC VCC M/IO# VCC PLOCK# BLAST# A4
15 IGNNE# NMI FLUSH# A20M# HOLD KEN# STPCLK# BRDY# BE2# BE0# PWT D/C# LOCK# HLDA BREQ A3 A6
14 NC UP# INC PLUG PLUG PLUG PLUG PLUG PLUG A2 VCC VSS
13 FERR# NC NC PLUG PLUG A7 A8 A10
12 NC NC SMIACT# PLUG PLUG A5 A11 VSS
11 VSS VCC NC A6 VCC VSS
10 NC SMI# SRESET A13 VCC VSS
9 VSS VCC D30 A16 VCC VSS
8 D26 D31 D28 A20 VCC VSS
7 VSS VCC D29 A22 A15 A12
6 D24 D25 D27 PLUG PLUG A24 VCC VSS
5 DP3 VSS VCC PLUG PLUG A21 A18 A14
4 D23 VSS VCC KEY PLUG PLUG PLUG PLUG PLUG A19 VSS NC
3 NC VSS CLK D17 D10 D15 D12 DP2 D16 D14 D7 D4 DP0 A30 A17 VCC A23
2 D22 D21 D18 D13 VCC D8 VCC D3 D5 VCC D6 VCC D1 A29 VSS A25 A26
1 D20 D16 D11 D9 VSS DP1 VSS VSS VCC VSS VSS VSS D2 D0 A31 A28 A27
Intel486™ DX2 OverDrive™ Processor
TOP SIDE VIEW
169 Lead PGA
(ODP)
290436-3

Figure 1.2.2

Table 1.2. Pin Cross Reference by Pin Name (ODP)

Address		Data		Control		N/C(1)	V_{CC}	V_{SS}
A_2	Q14	D_0	P1	A20M#	D15	A10	B7	A7
A_3	R15	D_1	N2	ADS#	S17	A12	B9	A9
A_4	S16	D_2	N1	AHOLD	A17	A14	B11	A11
A_5	Q12	D_3	H2	BE0#	K15	B12	C4	B3
A_6	S15	D_4	M3	BE1#	J16	B13	C5	B4
A_7	Q13	D_5	J2	BE2#	J15	C13	E16	B5
A_8	R13	D_6	L2	BE3#	F17	R17	G16	E1
A_9	Q11	D_7	L3	BLAST#	R16	S4	H16	E17
A_{10}	S13	D_8	F2	BOFF#	D17	A3	J1	G1
A_{11}	R12	D_9	D1	BRDY#	H15	B16	K16	G17
A_{12}	S7	D_{10}	E3	BREQ#	Q15	C11	L16	H1
A_{13}	Q10	D_{11}	C1	BS8#	D16		M2	H17
A_{14}	S5	D_{12}	G3	BS16#	C17		M16	K1
A_{15}	R7	D_{13}	D2	CLK	C3		P16	K17
A_{16}	Q9	D_{14}	K3	D/C#	M15	INC(2)	R3	L1
A_{17}	Q3	D_{15}	F3	DP0	N3			L17
A_{18}	R5	D_{16}	J3	DP1	F1	C14	R6	M1
A_{19}	Q4	D_{17}	D3	DP2	H3		R8	M17
A_{20}	Q8	D_{18}	C2	DP3	A5		R9	P17
A_{21}	Q5	D_{19}	B1	EADS#	B17	PLUG	R10	Q2
A_{22}	Q7	D_{20}	A1	FERR#	A13			R4
A_{23}	S3	D_{21}	B2	FLUSH#	C15	D5	R11	S6
A_{24}	Q6	D_{22}	A2	HLDA	P15	D6	R14	S8
A_{25}	R2	D_{23}	A4	HOLD	E15	D12		S9
A_{26}	S2	D_{24}	A6	IGNNE#	A15	D13		S10
A_{27}	S1	D_{25}	B6	INTR	A16	D14		S11
A_{28}	R1	D_{26}	C7	KEN#	F15	E4		S12
A_{29}	P2	D_{27}	C6	LOCK#	N15	E14		S14
A_{30}	P3	D_{28}	C8	M/IO#	N16	F4		
A_{31}	Q1	D_{29}	A8	NMI	B15	F14		
		D_{30}	C9	PCD	J17	M4		
		D_{31}	B8	PCHK#	Q17	M14		
				PWT	L15	N4		
				PLOCK#	Q16	N14		
				RDY#	F16	P4		
				RESET	C16	P5		
				SMI#	B10	P6		
				SMIACT#	C12	P12		
				SRESET	C10	P13		
				STPCLK#	G15	P14		
				UP#	B14			
				W/R#	N17			
				KEY	D4			

NOTES:
1. All NC pins must remain unconnected.
2. The INC pin is defined to be an internal no-connect. This means that the pin is not internally connected and may be used for the routing of external signals.

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1.3 Intel486 DX2 OverDrive™ Processor for PGA Intel486™ DX Microprocessor-Based Systems (without an OverDrive™ Processor Socket)

- **Powerful Performance Booster for PGA Intel486™ DX CPU-Based Systems**
  - **Improves Overall System Performance by up to 70%**
  - **Increases Both Integer and Floating-Point Performance**
- **168-Lead Pin Grid Array Package**
  - **Pin Compatible with Intel486™ DX CPU**
- **Math CoProcessor Included On-Chip**
- **High Integration Enables On-Chip**
  - **8 Kbyte Code and Data Cache**
  - **Floating Point Unit**
  - **Paged, Virtual Memory Management**
- **Compatible with SL Enhanced Features**
- **Utilizes Intel486™ DX2 Speed-Doubling Technology**
  - **CPU Core Runs at Twice the Frequency of the System Bus**
  - **Compatible with 33 and 25 MHz Systems**
- **Binary Compatible with Large Installed Software Base**
  - **MS-DOS, OS/2, Windows**
  - **UNIX System V/386**
  - **iRMX®, iRMK Kernals**
- **High Performance Design**
  - **Core Clock Speed up to 66 MHz**
  - **106 Mbyte/sec Burst Bus**
  - **CHMOS V Process Technology**
- **Complete 32-Bit Architecture**
  - **Address and Data Busses**
  - **Registers**
  - **8-, 16-, 32-Bit Data Types**

The Intel486 DX2 OverDrive processor for Intel486 DX microprocessor-based personal computers is a powerful, single-chip upgrade that is intrinsically cost effective and that offers excellent price/performance. Based on Intel486 DX2 technology, the Intel OverDrive processor integrates an integer unit, a floating point unit, a memory management unit and an 8 Kbyte cache on a single chip.

Using the Intel486 DX2's "speed doubling" technology, the Intel OverDrive processor operates internally at twice the speed of the system bus. This allows users of Intel486 DX microprocessor-based systems to double the frequency of their computer's CPU by replacing a single chip, without upgrading or modifying any other system components. For example, adding an Intel486 DX2 OverDrive processor to an Intel486 DX 33 MHz system will double the CPUs internal operating speed to 66 MHz. Depending on the application, the OverDrive processor can provide an overall system performance boost of up to 70%.

The Intel486 DX2 OverDrive processor, ODPR, is designed to be installed in the Intel486 DX CPU socket after the Intel486 DX CPU has been removed.

Both the 25 MHz and 33 MHz versions of the OverDrive processor for Intel486 DX CPU-based Systems without an OverDrive processor socket have a heat sink attached to the standard 168-lead PGA package.

1.3.1 Pinout

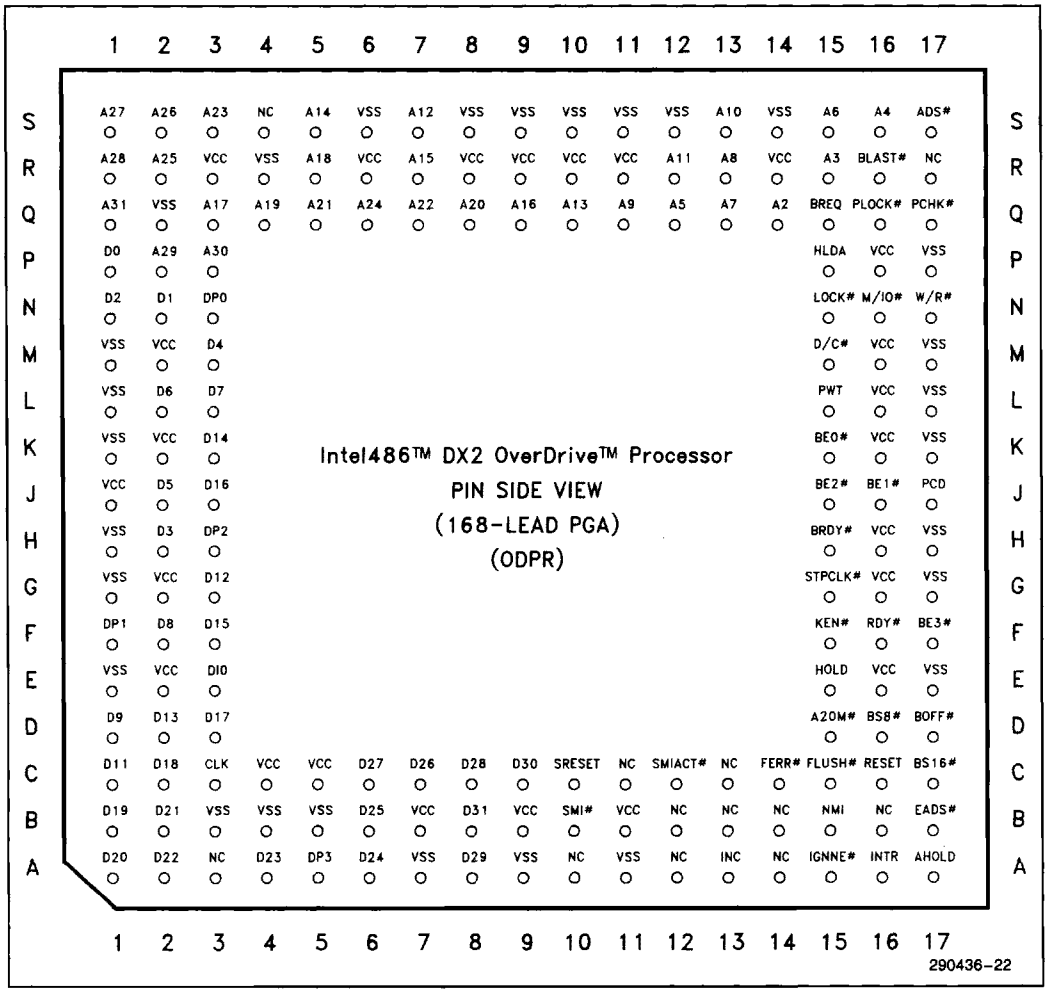


Figure 1.3.1

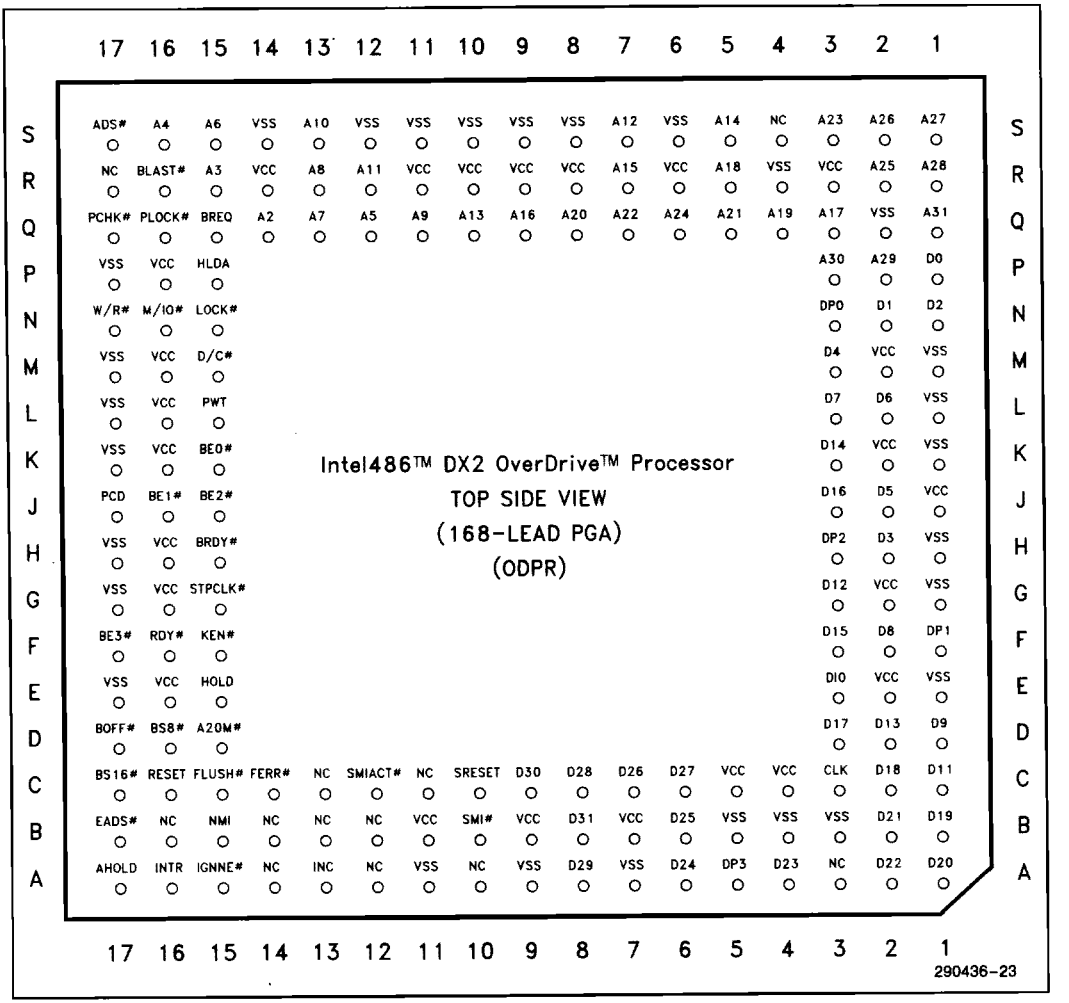

17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
S ADS# A4 A6 VSS A10 VSS VSS VSS VSS VSS A12 VSS A14 NC A23 A26 A27
R NC BLAST# A3 VCC A8 A11 VCC VCC VCC VCC A15 VCC A18 VSS VCC A25 A28
Q PCHK# PLOCK# BREQ A2 A7 A5 A9 A13 A16 A20 A22 A24 A21 A19 A17 VSS A31
P VSS VCC HLDA A30 A29 D0
N W/R# M/IO# LOCK# DP0 D1 D2
M VSS VCC D/C# D4 VCC VSS
L VSS VCC PWT D7 D6 VSS
K VSS VCC BE0# D14 VCC VSS
J PCD BE1# BE2# D16 D5 VCC
H VSS VCC BRDY# DP2 D3 VSS
G VSS VCC STPCLK# D12 VCC VSS
F BE3# RDY# KEN# D15 D8 DP1
E VSS VCC HOLD DI0 VCC VSS
D BOFF# BS8# A20M# D17 D13 D9
C BS16# RESET FLUSH# FERR# NC SMIACT# NC SRESET D30 D28 D26 D27 VCC VCC CLK D18 D11
B EADS# NC NMI NC NC NC VCC SMI# VCC D31 VCC D25 VSS VSS VSS D21 D19
A AHOLD INTR IGNNE# NC INC NC VSS NC VSS D29 VSS D24 DP3 D23 NC D22 D20
Intel486™ DX2 OverDrive™ Processor
TOP SIDE VIEW
(168-LEAD PGA)
(ODPR)
17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
290436-23

Figure 1.3.2

Table 1.3. Pin Cross Reference by Pin Name (ODPR)

Address		Data		Control		N/C(1)	V_{CC}	V_{SS}
A_2	Q14	D_0	P1	A20M#	D15	A3	B7	A7
A_3	R15	D_1	N2	ADS#	S17	A10	B9	A9
A_4	S16	D_2	N1	AHOLD	A17	A12	B11	A11
A_5	Q12	D_3	H2	BE0#	K15	A14	C4	B3
A_6	S15	D_4	M3	BE1#	J16	B12	C5	B4
A_7	Q13	D_5	J2	BE2#	J15	B13	E2	B5
A_8	R13	D_6	L2	BE3#	F17	B14	E16	E1
A_9	Q11	D_7	L3	BLAST#	R16	B16	G2	E17
A_{10}	S13	D_8	F2	BOFF#	D17	C11	G16	G1
A_{11}	R12	D_9	D1	BRDY#	H15	C13	H16	G17
A_{12}	S7	D_{10}	E3	BREQ#	Q15	R17	J1	H1
A_{13}	Q10	D_{11}	C1	BS8#	D16	S4	K2	H17
A_{14}	S5	D_{12}	G3	BS16#	C17		K16	K1
A_{15}	R7	D_{13}	D2	CLK	C3		L16	K17
A_{16}	Q9	D_{14}	K3	D/C#	M15	INC(2)	M2	L1
A_{17}	Q3	D_{15}	F3	DP0	N3		M16	L17
A_{18}	R5	D_{16}	J3	DP1	F1	A13	P16	M1
A_{19}	Q4	D_{17}	D3	DP2	H3		R3	M17
A_{20}	Q8	D_{18}	C2	DP3	A5		R6	P17
A_{21}	Q5	D_{19}	B1	EADS#	B17		R8	Q2
A_{22}	Q7	D_{20}	A1	FERR#	C14		R9	R4
A_{23}	S3	D_{21}	B2	FLUSH#	C15		R10	S6
A_{24}	Q6	D_{22}	A2	HLDA	P15		R11	S8
A_{25}	R2	D_{23}	A4	HOLD	E15		R14	S9
A_{26}	S2	D_{24}	A6	IGNNE#	A15			S10
A_{27}	S1	D_{25}	B6	INTR	A16			S11
A_{28}	R1	D_{26}	C7	KEN#	F15			S12
A_{29}	P2	D_{27}	C6	LOCK#	N15			S14
A_{30}	P3	D_{28}	C8	M/IO#	N16			
A_{31}	Q1	D_{29}	A8	NMI	B15			
		D_{30}	C9	PCD	J17			
		D_{31}	B8	PCHK#	Q17			
				PWT	L15			
				PLOCK#	Q16			
				RDY#	F16			
				RESET	C16			
				SMI#	B10			
				SMIACT#	C12			
				SRESET	C10			
				STPCLK#	G15			
				W/R#	N17			

NOTES:
1. All NC pins must remain unconnected.
2. The INC pin is defined to be internal no-connect. This means that the pin is not internally connected and may be used for the routing of external signals.

1.4 PIN DESCRIPTIONS

What follows is a brief pin description.

Symbol	Type	Name and Function
CLK	I	*Clock* provides the fundamental timing for the bus interface unit and is multiplied by two (2x) to provide the internal frequency for the Intel OverDrive processor. All external timing parameters are specified with respect to the rising edge of CLK.
ADDRESS BUS		
A31–A4 A2–A3	I/O O	A31–A2 are the *address lines* of the processor. A31–A2, together with the byte enables BE0#–BE3#, define the physical area of memory or input/output space accessed. Address lines A31–A4 are used to drive addresses into the processor to perform cache line invalidations. Input signals must meet setup and hold times t_{22} and t_{23}. A31–A2 are not driven during bus or address hold.
BE0–3#	O	The *byte enable* signals indicate active bytes during read and write cycles. During the first cycle of a cache fill, the external system should assume that all byte enables are active. BE3# applies to D24–D31, BE2# applies to D16–D23, BE1# applies to D8–D15 and BE0# applies to D0–D7. BE0#–BE3# are active LOW and are not driven during bus hold.
DATA BUS		
D31–D0	I/O	These are the *data lines* for the Intel OverDrive processor. Lines D0–D7 define the least significant byte of the data bus while lines D24–D31 define the most significant byte of the data bus. These signals must meet setup and hold times t_{22} and t_{23} for proper operation on reads. These pins are driven during the second and subsequent clocks of write cycles.
DATA PARITY		
DP0–DP3	I/O	There is one *data parity* pin for each byte of the data bus. Data parity is generated on all write data cycles with the same timing as the data driven by the Intel OverDrive processor. Even parity information must be driven back into the microprocessor on the data parity pins with the same timing as read information to insure that the correct parity check status is indicated by the Intel OverDrive processor. The signals read on these pins do not affect program execution. Input signals must meet setup and hold times t_{22} and t_{23}. DP0–DP3 should be connected to V_{CC} through a pullup resistor in systems which do not use parity. DP0–DP3 are active HIGH and are driven during the second and subsequent clocks of write cycles.
PCHK#	O	*Parity Status* is driven on the PCHK# pin the clock after ready for read operations. The parity status is for data sampled at the end of the previous clock. A parity error is indicated by PCHK# being LOW. Parity status is only checked for enabled bytes as indicated by the byte enable and bus size signals. PCHK# is valid only in the clock immediately after read data is returned to the microprocessor. At all other times PCHK# is inactive (HIGH). PCHK# is never floated.

1.4 PIN DESCRIPTIONS (Continued)

Symbol	Type	Name and Function
BUS CYCLE DEFINITION		
M/IO# D/C# W/R#	O O O	The *memory/input-output, data/control* and *write/read* lines are the primary bus definition signals. These signals are driven valid as the ADS# signal is asserted.

M/IO#	D/C#	W/R#	Bus Cycle Initiated
0	0	0	Interrupt Acknowledge
0	0	1	Halt/Special Cycle
0	1	0	I/O Read
0	1	1	I/O Write
1	0	0	Code Read
1	0	1	Reserved
1	1	0	Memory Read
1	1	1	Memory Write

The bus definition signals are not driven during bus hold and follow the timing of the address bus. Refer to Section 7.2.11 for a description of the special bus cycles.

LOCK#	O	The *bus lock* pin indicates that the current bus cycle is locked. The Intel OverDrive processor will not allow a bus hold when LOCK# is asserted (but address holds are allowed). LOCK# goes active in the first clock of the first locked bus cycle and goes inactive after the last clock of the last locked bus cycle. The last locked cycle ends when RDY# is returned. LOCK# is active LOW and is not driven during bus hold. Locked read cycles will not be transformed into cache fill cycles if KEN# is returned active.
PLOCK#	O	The *pseudo-lock* pin indicates that the current bus transaction requires more than one bus cycle to complete. Examples of such operations are floating point long reads and writes (64 bits), segment table descriptor reads (64 bits), in addition to cache line fills (128 bits). The Intel OverDrive processor will drive PLOCK# active until the addresses for the last bus cycle of the transaction have been driven regardless of whether RDY# or BRDY# have been returned. Normally PLOCK# and BLAST# are inverse of each other. However during the first bus cycle of a 64-bit floating point write, both PLOCK# and BLAST# will be asserted. PLOCK# is a function of the BS8#, BS16# and KEN# inputs. PLOCK# should be sampled only in the clock RDY# is returned. PLOCK# is active LOW and is not driven during bus hold.
BUS CONTROL		
ADS#	O	The *address status* output indicates that a valid bus cycle definition and address are available on the cycle definition lines and address bus. ADS# is driven active in the same clock as the addresses are driven. ADS# is active LOW and is not driven during bus hold.
RDY#	I	The *non-burst ready* input indicates that the current bus cycle is complete. RDY# indicates that the external system has presented valid data on the data pins in response to a read or that the external system has accepted data from the Intel OverDrive processor in response to a write. RDY# is ignored when the bus is idle and at the end of the first clock of the bus cycle. RDY# is active during address hold. Data can be returned to the processor while AHOLD is active. RDY# is active LOW, and is not provided with an internal pullup resistor. RDY# must satisfy setup and hold times t_{16} and t_{17} for proper chip operation.

1.4 PIN DESCRIPTIONS (Continued)

Symbol	Type	Name and Function
BURST CONTROL		
BRDY#	I	The *burst ready input* performs the same function during a burst cycle that RDY# performs during a non-burst cycle. BRDY# indicates that the external system has presented valid data in response to a read or that the external system has accepted data in response to a write. BRDY# is ignored when the bus is idle and at the end of the first clock in a bus cycle. BRDY# is sampled in the second and subsequent clocks of a burst cycle. The data presented on the data bus will be strobed into the microprocessor when BRDY# is sampled active. If RDY# is returned simultaneously with BRDY#, BRDY# is ignored and the burst cycle is prematurely interrupted BRDY# is active LOW and is provided with a small pullup resistor. BRDY# must satisfy the setup and hold times t_{16} and t_{17}.
BLAST#	O	The *burst last* signal indicates that the next time BRDY# is returned the burst bus cycle is complete. BLAST# is active for both burst and non-burst bus cycles. BLAST# is active LOW and is not driven during bus hold.
INTERRUPTS		
RESET	I	The **RESET** input forces the CPU to begin execution at a known state. Reset is asynchronous, but must meet setup and hold times t20 and t21 for recognition in any specific clock. The CPU cannot begin execution of instructions until at least 1 ms after V_{CC} and CLK have reached their proper AC and DC specifications. However, for soft resets, RESET should remain active for at least 15 CLK periods. The RESET pin should remain active during this time to ensure proper CPU operation. RESET is active HIGH. RESET sets the SMBASE descriptor to a default address of 30000H. If the system uses SMBASE relocation, then the SRESET pin should be used for soft resets.
SRESET	I	The SRESET pin duplicates all the functionality of the RESET pin with the following two exceptions: 1. The SMBASE register will retain its previous value. 2. If UP# (I) is asserted, SRESET will not have an effect on the host microprocessor. For soft resets, SRESET should remain active for at least 15 CLK periods. SRESET is active HIGH. SRESET is asynchronous but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
SMI#	I	The **System Management Interrupt** input is used to invoke the System Management Mode (SMM). SMI# is a falling edge triggered signal which forces the CPU into SMM at the completion of the current instruction. SMI# is recognized on an instruction boundary and at each iteration for repeat string instructions. SMI# does not break LOCKed bus cycles and cannot interrupt a currently executing SMM. The CPU will latch the falling edge of one pending SMI# signal while the CPU is executing an existing SMI. The nested SMI will not be recognized until after the execution of a Resume (RSM) instruction.
SMIACT#	O	The **System Management Interrupt ACTive** is an active low output, indicating that the processor is operating in SMM. It is asserted when the CPU begins to execute the SMI state save sequence and will remain active LOW until the processor executes the last state restore cycle out of SMRAM.
STPCLK#	I	The **SToP CLocK request** input signal indicates a request has been made to turn off the CLK input. When the CPU recognizes a STPCLK#, the processor will stop execution on the next instruction boundary, unless superseded by a higher priority interrupt, empty all internal pipelines and the write buffers and generate a Stop Grant acknowledge bus cycle. STPCLK# is active LOW and is provided with an internal pull-up resistor. STPCLK# is asynchronous but setup and hold times t_{20} and t_{21} must be met to ensure recognition in any specific clock.

1.4 PIN DESCRIPTIONS (Continued)

Symbol	Type	Name and Function
INTERRUPTS (Continued)		
INTR	I	The *maskable interrupt* indicates that an external interrupt has been generated. If the internal interrupt flag is set in EFLAGS, active interrupt processing will be initiated. The Intel OverDrive processor will generate two locked interrupt acknowledge bus cycles in response to the INTR pin going active. INTR must remain active until the interrupt acknowledges have been performed to assure that the interrupt is recognized. INTR is active HIGH and is not provided with an internal pulldown resistor. INTR is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
NMI	I	The *non-maskable interrupt* request signal indicates that an external non-maskable interrupt has been generated. NMI is rising edge sensitive. NMI must be held LOW for at least four CLK periods before this rising edge. NMI is not provided with an internal pulldown resistor. NMI is asynchronous, but must meet setup and hold times t_{20} and t_{21} for recognition in any specific clock.
BUS ARBITRATION		
BREQ	O	The *internal cycle pending* signal indicates that the Intel OverDrive processor has internally generated a bus request. BREQ is generated whether or not the Intel OverDrive processor is driving the bus. BREQ is active HIGH and is never floated.
HOLD	I	The *bus hold request* allows another bus master complete control of the Intel OverDrive processor bus. In response to HOLD going active the Intel OverDrive processor will float most of its output and input/output pins. HLDA will be asserted after completing the current bus cycle, burst cycle or sequence of locked cycles. The Intel OverDrive processor will remain in this state until HOLD is deasserted. HOLD is active high and is not provided with an internal pulldown resistor. HOLD must satisfy setup and hold times t_{18} and t_{19} for proper operation.
HLDA	O	*Hold acknowledge* goes active in response to a hold request presented on the HOLD pin. HLDA indicates that the Intel OverDrive processor has given the bus to another local bus master. HLDA is driven active in the same clock that the Intel OverDrive processor floats its bus. HLDA is driven inactive when leaving bus hold. HLDA is active HIGH and remains driven during bus hold.

1.4 PIN DESCRIPTIONS (Continued)

Symbol	Type	Name and Function
BUS ARBITRATION (Continued)		
BOFF#	I	The *backoff* input forces the Intel OverDrive processor to float its bus in the next clock. The microprocessor will float all pins normally floated during bus hold but HLDA will not be asserted in response to BOFF#. BOFF# has higher priority than RDY# or BRDY#; if both are returned in the same clock, BOFF# takes effect. The microprocessor remains in bus hold until BOFF# is negated. If a bus cycle was in progress when BOFF# was asserted the cycle will be restarted. BOFF# is active LOW and must meet setup and hold times t_{18} and t_{19} for proper operation.
CACHE INVALIDATION		
AHOLD	I	The *address hold* request allows another bus master access to the Intel OverDrive processor's address bus for a cache invalidation cycle. The Intel OverDrive processor will stop driving its address bus in the clock following AHOLD going active. Only the address bus will be floated during address hold, the remainder of the bus will remain active. AHOLD is active HIGH and is provided with a small internal pulldown resistor. For proper operation AHOLD must meet setup and hold times t_{18} and t_{19}.
EADS#	I	This signal indicates that a *valid external address* has been driven onto the Intel OverDrive processor address pins. This address will be used to perform an internal cache invalidation cycle. EADS# is active LOW and is provided with an internal pullup resistor. EADS# must satisfy setup and hold times t_{12} and t_{13} for proper operation.
CACHE CONTROL		
KEN#	I	The *cache enable* pin is used to determine whether the current cycle is cacheable. When the Intel OverDrive processor generates a cycle that can be cached and KEN# is active, the cycle will become a cache line fill cycle. Returning KEN# active one clock before RDY# during the last read in the cache line fill will cause the line to be placed in the on-chip cache. KEN# is active LOW and is provided with a small internal pullup resistor. KEN# must satisfy setup and hold times t_{14} and t_{15} for proper operation.
FLUSH#	I	The *cache flush* input forces the Intel OverDrive processor to flush its entire internal cache. FLUSH# is active low and need only be asserted for one clock. FLUSH# is asynchronous but setup and hold times t_{20} and t_{21} must be met for recognition in any specific clock. FLUSH# being sampled low in the clock before the falling edge of RESET causes the Intel OverDrive processor to enter the tri-state test mode.
PAGE CACHEABILITY		
PWT PCD	O O	The *page write-through* and *page cache disable* pins reflect the state of the page attribute bits, PWT and PCD, in the page table entry or page directory entry. If paging is disabled or for cycles that are not paged, PWT and PCD reflect the state of the PWT and PCD bits in control register 3. PWT and PCD have the same timing as the cycle definition pins (M/IO#, D/C# and W/R#). PWT and PCD are active HIGH and are not driven during bus hold. PCD is masked by the cache disable bit (CD) in Control Register 0.
NUMERIC ERROR REPORTING		
FERR#	O	The *floating point error* pin is driven active when a floating point error occurs. FERR# is similar to the ERROR# pin on the Intel387™ math coprocessor. FERR# is included for compatibility with systems using DOS type floating point error reporting. FERR# will not go active if FP errors are masked in FPU register. FERR# is active LOW, and is not floated during bus hold.

1.4 PIN DESCRIPTIONS (Continued)

Symbol	Type	Name and Function
NUMERIC ERROR REPORTING (Continued)		
IGNNE#	I	When the *ignore numeric error* pin is asserted the Intel OverDrive processor will ignore a numeric error and continue executing non-control floating point instructions, but FERR# will still be activated by the Intel OverDrive processor. When IGNNE# is deasserted the Intel OverDrive processor will freeze on a non-control floating point instruction, if a previous floating point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set. IGNNE# is active LOW and is provided with a small internal pullup resistor. IGNNE# is asynchronous but setup and hold times t_{20} and t_{21} must be met to insure recognition on any specific clock.
BUS SIZE CONTROL		
BS16# BS8#	I I	The *bus size 16* and *bus size 8* pins (bus sizing pins) cause the Intel OverDrive processor to run multiple bus cycles to complete a request from devices that cannot provide or accept 32 bits of data in a single cycle. The bus sizing pins are sampled every clock. The state of these pins in the clock before ready is used by the Intel OverDrive processor to determine the bus size. These signals are active LOW and are provided with internal pullup resistors. These inputs must satisfy setup and hold times t_{14} and t_{15} for proper operation.
ADDRESS MASK		
A20M#	I	When the *address bit 20 mask* pin is asserted, the Intel OverDrive processor masks physical address bit 20 (A20) before performing a lookup to the internal cache or driving a memory cycle on the bus. A20M# emulates the address wraparound at one Mbyte which occurs on the 8086. A20M# is active LOW and should be asserted only when the processor is in real mode. This pin is asynchronous but should meet setup and hold times t_{20} and t_{21} for recognition in any specific clock. For proper operation, A20M# should be sampled high at the falling edge of RESET.
I486 DX AND I486 SX CPU INTERFACE		
UP#(1,2)	O	The *upgrade present* pin is used to signal the Intel486 Microprocessor to float its outputs and get off the bus. It is active low and is never floated. UP# is driven low at power-up and remains active for the entire duration of the Upgrade Processor operation.
KEY PIN		
KEY(2)		The KEY pin is an electrically non-functional pin which is used to ensure correct Upgrade Processor orientation in a 169-pin socket.

NOTE:
1. The UP# pin was previously named the MP# pin in the i486 SX Microprocessor/i487 SX Math CoProcessor data book. The functionality is the same, only the name has changed.
2. The UP# input pin and KEY pin are not defined on the OverDrive processor for replacement of PGA Intel486 DX Microprocessor (ODPR).

Table 1.4.1. Output Pins

Name	Active Level	When Floated
BREQ	HIGH	
HLDA	HIGH	
BE0#-BE3#	LOW	Bus Hold
PWT, PCD	HIGH	Bus Hold
W/R#, D/C#, M/IO#	HIGH	Bus Hold
LOCK#	LOW	Bus Hold
PLOCK#	LOW	Bus Hold
ADS#	LOW	Bus Hold
BLAST#	LOW	Bus Hold
PCHK#	LOW	
FERR#	LOW	
SMIACT#	LOW	
UP#	LOW	
A2-A3	HIGH	Bus, Address Hold

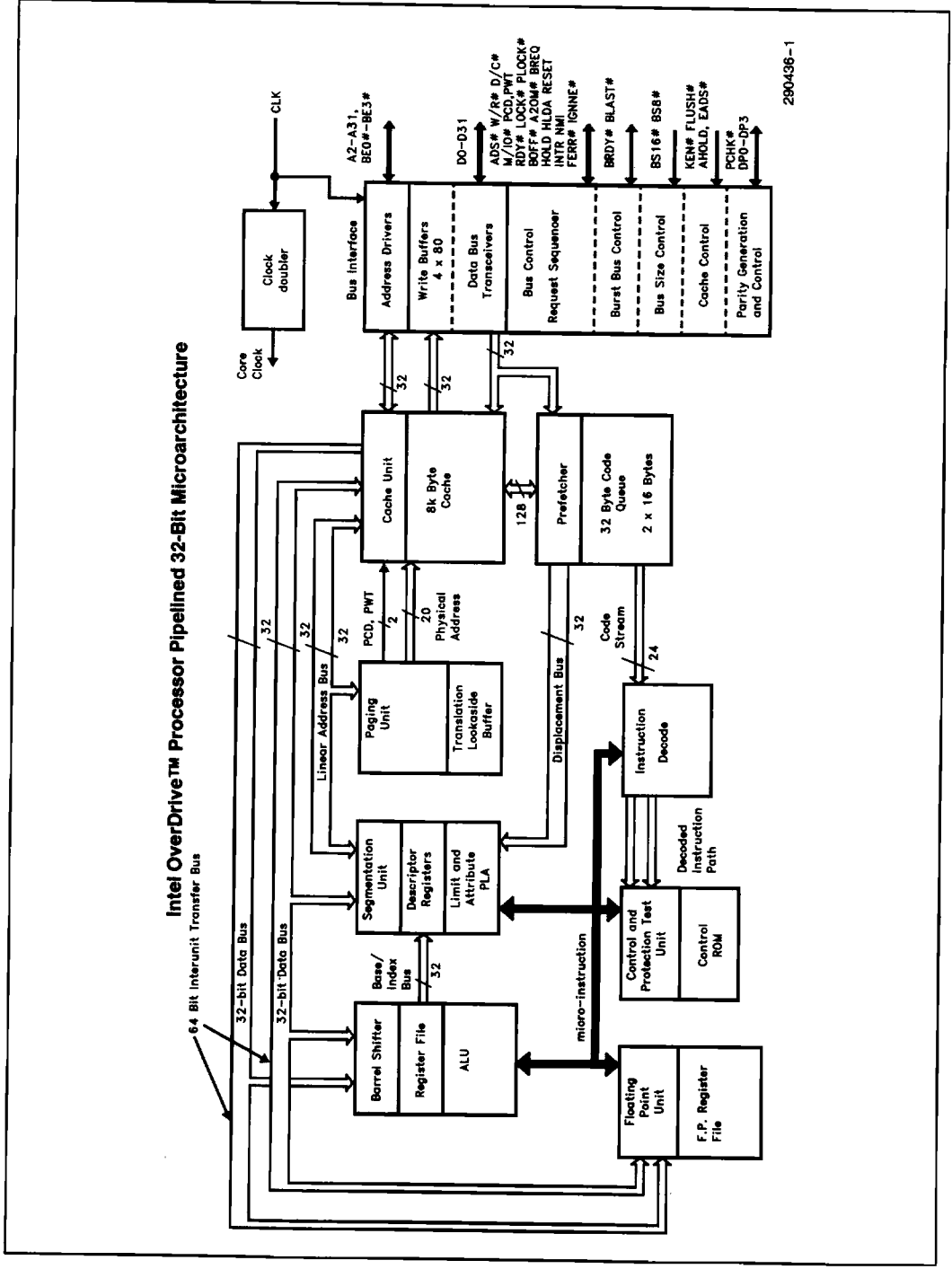
Table 1.4.2. Input Pins

Name	Active Level	Synchronous/ Asynchronous
CLK		
RESET	HIGH	Asynchronous
HOLD	HIGH	Synchronous
AHOLD	HIGH	Synchronous
EADS#	LOW	Synchronous
BOFF#	LOW	Synchronous
FLUSH#	LOW	Asynchronous
A20M#	LOW	Asynchronous
BS16#, BS8#	LOW	Synchronous
KEN#	LOW	Synchronous
RDY#	LOW	Synchronous
BRDY#	LOW	Synchronous
INTR	HIGH	Asynchronous
NMI	HIGH	Asynchronous
SRESET	HIGH	Asynchronous
SMI#	LOW	Asynchronous
STPCLK#	LOW	Asynchronous
IGNNE#	LOW	Asynchronous

Table 1.4.3. Input/Output Pins

Name	Active Level	When Floated
D0-D31	HIGH	Bus Hold
DP0-DP3	HIGH	Bus Hold
A4-A31	HIGH	Bus, Address Hold

1.5 Block Diagram



2.0 DIFFERENCES FROM Intel486™ SX AND Intel486™ DX CPU FUNCTIONALITY

The Intel486 DX2 OverDrive processor is essentially an enhanced Intel486 Microprocessor. There are three functional differences between the Intel OverDrive processor and Intel486 Microprocessors. First, the Intel OverDrive processor has an internal clock doubling circuit which decreases the time required to execute instructions. Second, the Intel OverDrive processor does not support the JTAG boundary scan test feature. Third, the Intel OverDrive processor has a different CPU revision identification than the Intel486 SX or Intel486 DX CPUs. These three differences are described in the following sections according to how they effect the CPU functionality.

2.1 Hardware Interface

The Intel OverDrive processor bus has been designed to be identical with the Intel486 Microprocessor bus. Although the external clock is internally doubled and data and instructions are manipulated in the CPU core at twice the external frequency, the external bus is functionally identical with the Intel486 CPU.

The four boundary scan test signals (TCK, Test clock; TMS, Test Mode select; TDI, Test Data Input; TDO, Test Data Output), defined for some Intel486 CPUs, are not specified for the Intel486 DX2 OverDrive processor.

The UP# (Upgrade Present) signal, which is defined as an input for some Intel486 CPUs, is an output signal on the Intel OverDrive processor. The UP# pin on the Intel OverDrive processor provides a logical low output signal which can be used to enable logic to recognize and configure the system for the Intel OverDrive processor. This signal is identical to the MP# output defined for the Intel487 SX Math CoProcessor. Refer to Section 3 for examples of use of the UP# signal.

The DX register always contains the component identifier at the conclusion of RESET. The Intel OverDrive processor has a different revision identifier in the DL register than the Intel486 SX or Intel486 DX Microprocessors (refer to Section 4.1). When the OverDrive processor is installed in a system the component identifier is supplied by the OverDrive processor, rather than the original CPU. The stepping identification portion of the component identification will change with different revisions of the OverDrive processor. The designer should only assume that the component identification for the OverDrive processor will be 043xH, where 'x' is the stepping identifier.

2.2 Testability

As detailed in Section 2.1, the Intel OverDrive processor does not support the JTAG boundary scan testability feature.

2.3 Instruction Set Summary

The Intel OverDrive processor supports all Intel486 extensions to the 8086/80186/80286 instruction set. In general, instructions will execute faster on the Intel OverDrive processor than the Intel486 Microprocessor. Specifically, an instruction that only uses memory from the on-chip cache executes at the full core clock rate while all bus accesses execute at the bus clock rate. To calculate the elapsed time of an instruction, the number of clock counts for that instruction must be multiplied by the clock period for the system. The instruction set clock count summary tables from the Intel486 SX and Intel486 DX Microprocessor Data Sheets can be used for the OverDrive processor with the following modifications:

— Clock counts for a cache hit: This value represents the number of internal CPU core clocks for an instruction that requires no external bus accesses or the base core clocks for an instruction requiring external bus accesses.

— Penalty clock counts for a cache miss: This value represents the worst-case approximation of the additional number of external clock counts that are required for an instruction which must access the external bus for data (a cache miss). This number must be multiplied by 2 to convert it to an equal number of internal CPU core clock counts and added to the base core clocks to compute the total number of core clocks for this instruction.

The actual number of core clocks for an instruction with a cache miss may be less than the base clock counts (from the cache hit column) plus the penalty clock counts (2 times the cache miss column number). The clock counts in the cache miss penalty column can be a cumulative value of external bus clocks (for data reads) and internal clocks for manipulating the data which has been loaded from the external bus. The number of clocks which are related to external bus accesses are correctly represented in terms of internal core clocks by multiplying by two. However, the clock counts related to internal data manipulation should not be multiplied by two. Therefore the total number of CPU core clock counts for an instruction with a cache miss represents a worst-case approximation.

To calculate the execution time for an OverDrive processor instruction, multiply the total CPU core clock counts by the core clock period. For example, in a 25 MHz system the core clock period is 20 ns (1/50 MHz).

Additionally, the assumptions specified below should be understood in order to estimate instruction execution time.

A cache miss will force the OverDrive processor to run an external bus cycle. The Intel486 microprocessor 32-bit burst bus is defined as r−b−w.

Where:

r = The number of bus clocks in the first cycle of a burst read or the number of clocks per data cycle is a non-burst read.

b = The number of bus clocks for the second and subsequent cycles in a burst read.

w = The number of bus clocks for a write.

The fastest bus the OverDrive processor can support is 2−1−2 assuming 0 waits states. The clock counts in the cache miss penalty column assume a 2−1−2 bus. For slower busses add r−2 clocks to the cache miss penalty for the first dword accessed. Other factors also affect instruction clock counts.

Instruction Clock Count Assumptions

1. The external bus is available for reads or writes at all times. Else add bus clocks to reads until the bus is available
2. Accesses are aligned. Add three core clocks to each misaligned access.
3. Cache fills complete before subsequent accesses to the same line. If a read misses the cache during a cache fill due to a previous read or prefetch, the read must wait for the cache fill to complete. If a read or write accesses a cache line still being filled, it must wait for the fill to complete.
4. If an effective address is calculated, the base register is not the destination register of the preceding instruction. If the base register is the destination register of the preceding instruction add 1 to the core clock counts shown. Back-to-back PUSH and POP instructions are not affected by this rule.
5. An effective address calculation uses one base register and does not use an index register. However, if the effective address calculation uses an index register. 1 core clock may be added to the clock shown.
6. The target of a jump is in the cache. If not, add r clocks for accessing the destination instruction of a jump. If the destination instruction is not completely contained in the first dword read, add a maximum of 3b bus clocks. If the destination instruction is not completely contained in the first 16 byte burst, add a maximum of another r+3b bus clocks.
7. If no write buffer delay, w bus clocks are added only in the case in which all write buffers are full.
8. Displacement and immediate not used together. If displacement and immediate used together, 1 core clock may be added to the core clock count shown.
9. No invalidate cycles. Add a delay of 1 bus clock for each invalidate cycle if the invalidate cycle contends for the internal cache/external bus when the OverDrive processor needs to use it.
10. Page translation hits in TLB. A TLB miss will add 13, 21 or 28 bus clocks + 1 possible core clock to the instruction depending on whether the Accessed and/or Dirty bit in neither, one or both of the page entries needs to be set in memory. This assumes that neither page entry is in the data cache and a page fault does not occur on the address translation.
11. No exceptions are detected during instruction execution. Refer to interrupt core Clock Counts Table for extra clocks if an interrupt is detected.
12. Instructions that read multiple consecutive data items (i.e., task switch, POPA, etc.) and miss the cache are assumed to start the first access on a 16-byte boundary. If not, an extra cache line fill may be necessary which may add up to (r+3b) bus clocks to the cache miss penalty.

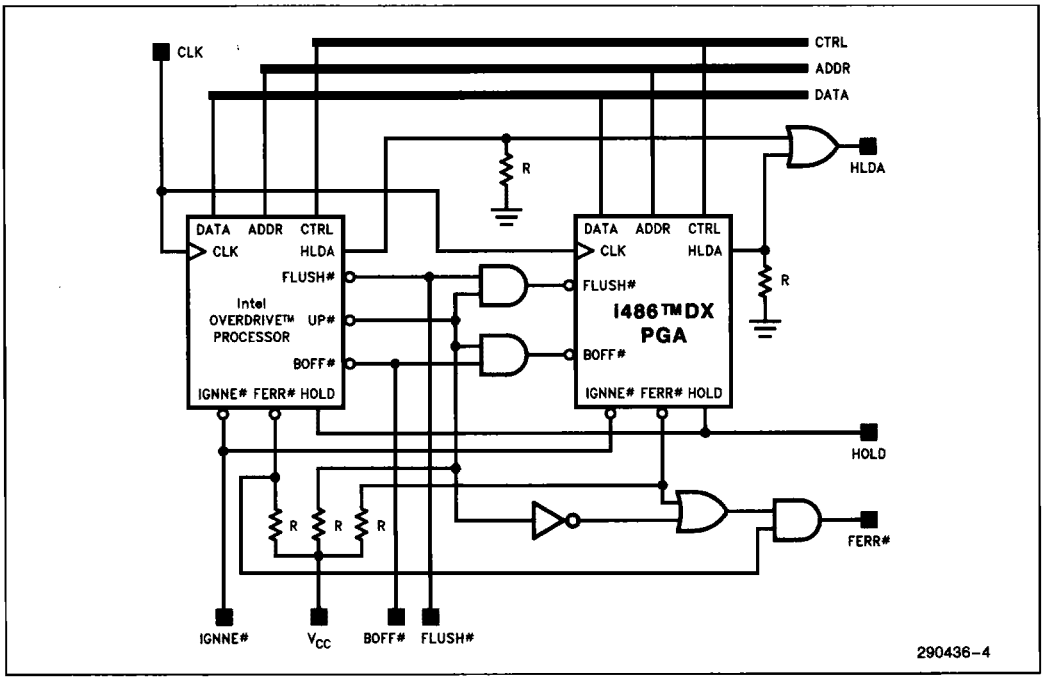


Figure 3.1. Intel OverDrive™ Socket Circuit Diagram for PGA Intel486™ DX CPU Based Systems

3.0 Intel OverDrive™ PROCESSOR CIRCUIT DESIGN

Figures 3.1, 3.2 and 3.3 show the circuits which interface the original CPU with the Intel OverDrive processor socket. These circuits allow Intel486 DX and Intel486 SX CPU based systems to be upgraded with the Intel OverDrive processor.

The circuits shown in Figures 3.1 and 3.2 may only be used for Intel486 CPUs that do not have the UP# input pin. The circuit shown in Figure 3.3 should be used for all Intel486 CPUs that have the UP# input pin.

3.1 Upgrade Circuit for PGA Intel486™ DX Based Systems

The Intel OverDrive processor socket Circuit for PGA Intel486 DX CPU based systems allows the Intel486 DX CPU complete control of the system when the Intel OverDrive processor socket is unpopulated. The HLDA signal from the Intel OverDrive processor socket should be tied low through a resistor while the UP# and FERR# signals from the Intel OverDrive processor socket should be tied high through a resistor to insure that the Intel486 DX CPU functions correctly when an Intel OverDrive processor socket component is not installed.

When the Intel OverDrive rocessor is installed, the Upgrade Present output, UP# pin, causes the FLUSH# and BOFF# signals to be driven active to the Intel486 DX CPU. When the Intel486 DX CPU samples FLUSH# active during reset, the Intel486 DX CPU enters tri-state output test mode after reset, which causes the Intel486 DX CPU to float all of its output signals. To float most of the Intel486 DX CPU's output pins before the end of reset, BOFF# is also driven active to the Intel486 DX CPU. BOFF# immediately causes all output signals to float except PCHK#, BREQ, HLDA and FERR#.

In addition to floating the PGA Intel486 DX CPU's outputs, the Intel486 DX CPU's HLDA and FERR# signals must be gated to prevent potential bus contention with the Intel OverDrive processor's HLDA and FERR# signals during reset. During reset the Intel486 DX CPU may not recognize HOLD active because BOFF# is driven active to the Intel486 DX CPU by the Intel OverDrive processor. If the Intel486 DX CPU does not recognize HOLD active, it will not drive HLDA active. However, the Intel OverDrive processor will recognize HOLD active and drive HLDA. By gating the HLDA signals from the Intel486 DX CPU and Intel OverDrive processor socket, bus contention is avoided if HOLD is driven active during reset. Because the state of FERR# is undefined during reset, bus contention is also avoided by gating FERR#.

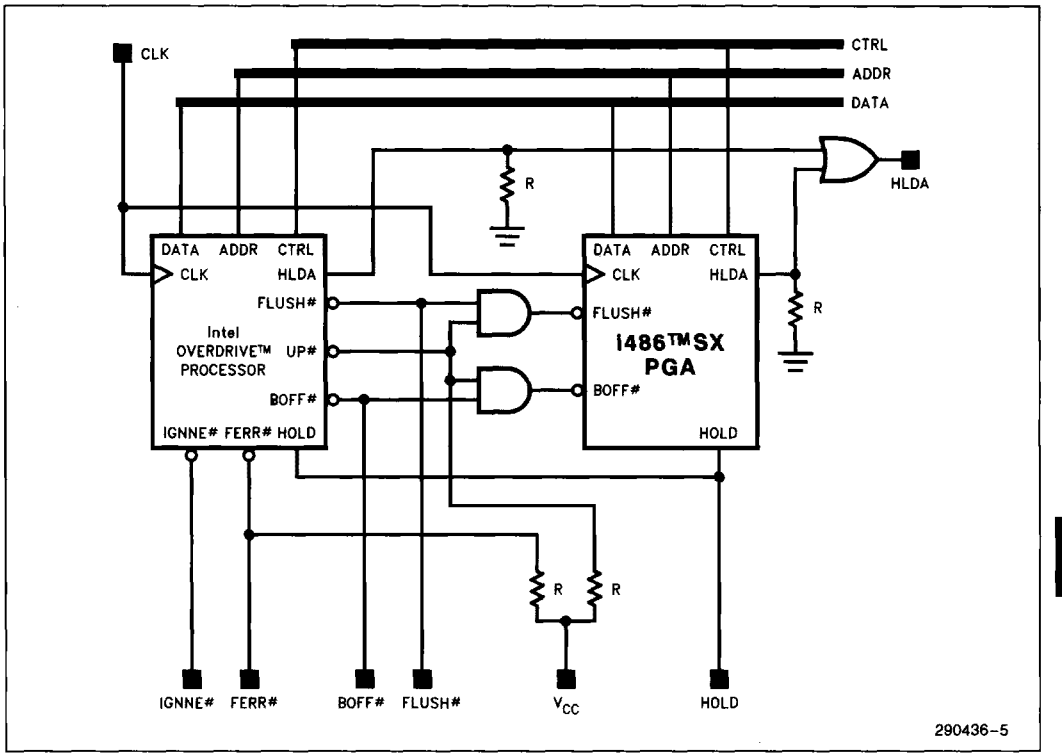


Figure 3.2. Intel OverDrive Socket Circuit Diagram for PGA Intel486 SX CPU Based Systems

3.2 Upgrade Circuit for PGA Intel486 SX CPU Based Systems

The Intel OverDrive processor socket Circuit for PGA Intel486 SX CPU based systems is the same as the Intel OverDrive processor socket Circuit for the PGA Intel486 DX CPU based system except that no gates are needed for the FERR# signal. The OverDrive processor socket Circuit allows the PGA Intel486 SX CPU complete control of the system when the Intel OverDrive processor socket is unpopulated. The HLDA signal from the Intel OverDrive processor socket should be tied low through a resistor while the UP# and FERR# signals from the Intel OverDrive processor socket should be tied high through a resistor to insure that the PGA Intel486 SX CPU functions correctly when an Intel OverDrive processor is not installed.

When the Intel OverDrive processor is installed, the Upgrade Present output, UP# pin, causes the FLUSH# and BOFF# signals to be driven active to the PGA Intel486 SX CPU. When the PGA Intel486 SX CPU samples FLUSH# active during reset, the PGA Intel486 SX CPU enters tri-state output test mode after reset which causes the PGA Intel486 SX CPU to float all of its output signals. To float most of the PGA Intel486 SX CPU's output pins before the end of reset, BOFF# is also driven active to the PGA Intel486 SX CPU. BOFF# immediately causes all output signals to float except PCHK#, BREQ, and HLDA.

In addition to floating the PGA Intel486 SX CPU's outputs, the PGA Intel486 SX CPU's HLDA signal must be gated to prevent potential bus contention with the Intel OverDrive processor's HLDA signal during reset. During reset, the PGA Intel486 SX CPU may not recognize HOLD active because BOFF# is driven active to the PGA Intel486 SX CPU by the Intel OverDrive processor. If the PGA Intel486 SX CPU does not recognize HOLD active, it will not drive HLDA active. However, the Intel OverDrive processor will recognize HOLD active and drive HLDA. By gating the HLDA signals from the PGA Intel486 SX CPU and Intel OverDrive processor, bus contention is avoided if HOLD is driven active during reset.

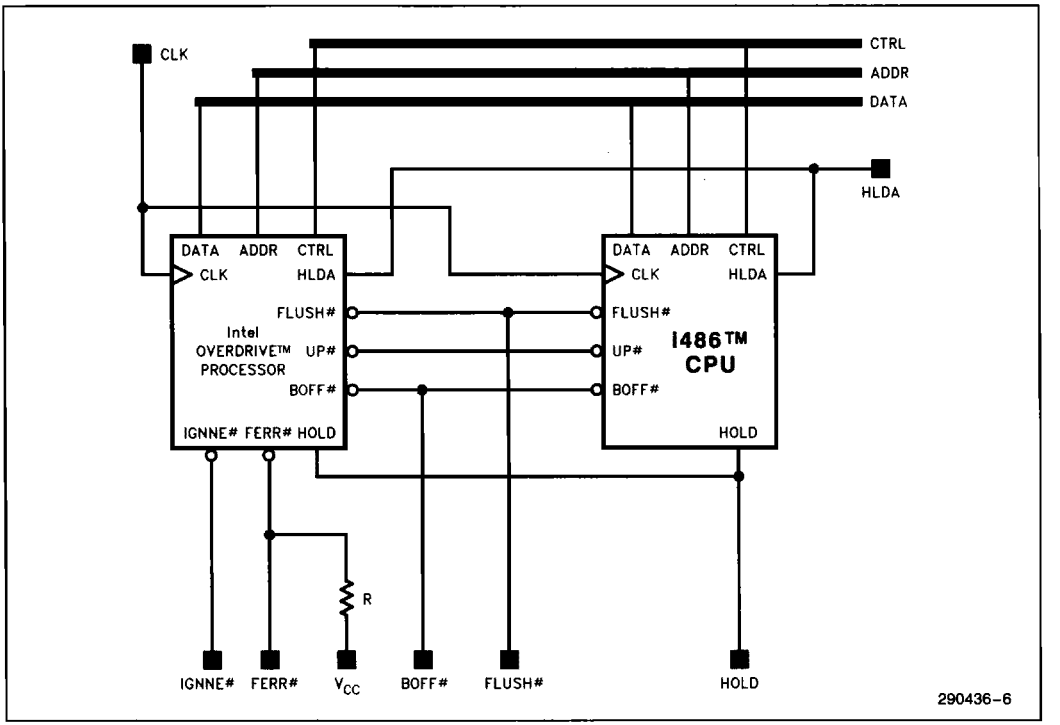


Figure 3.3. Intel OverDrive™ Socket Circuit Diagram for Systems Based on Intel486 CPUs That Have the UP# Input Pin

3.3 Upgrade Circuit for Intel486 CPU Based Systems with UP#

The Intel OverDrive processor socket circuit for UP# Intel486 CPU based systems requires no additional gates. The Upgrade Present input, UP# pin, allows the Intel486 CPU to directly recognize when the Intel OverDrive processor socket is populated. When the UP# pin is driven active to the Intel486 CPU, the Intel486 CPU tri-states all of its output pins and enters power-down mode.

4.0 BIOS AND SOFTWARE

The following should be considered when designing a system for upgrade with an Intel OverDrive processor.

4.1 Intel OverDrive Processor Detection

The component identifier and stepping/revision identifier for the Intel OverDrive processor is readable in DH and DL registers respectively, immediately after RESET, where

DH = 04h

DL = 30h–3Fh.

As it is difficult to differentiate between the Intel486 DX CPU and the Intel OverDrive processor in software, it is recommended that the BIOS save the contents of the DX register, immediately after RESET, so that this information can be used later, if required, to identify an Intel OverDrive processor in the system.

NOTE:
Initialization routines for Intel486 SX CPU systems should check for the presence of a floating point unit and set the CR0 register accordingly. (Refer to the Intel486 SX Microprocessor Data Book for specific details.)

4.2 Timing Dependent Loops

The Intel OverDrive processor executes instructions at twice the frequency of the input clock. Thus, software (or instruction based) timing loops will execute faster on the Intel OverDrive processor than on the Intel486 DX or Intel486 SX CPU (at the same input clock frequency). Instructions such as NOP, LOOP, and JMP $+2, have been used by BIOS to implement timing loops that are required, for example, to enforce recovery time between consecutive accesses for I/O devices. These instruction based timing loop implementations may require modification for systems intended to be upgradable with the Intel OverDrive processor.

In order to avoid any incompatibilities, it is recommended that timing requirements be implemented in hardware rather than in software. This provides transparency and also does not require any change in BIOS or I/O device drivers in the future when moving to higher processor clock speeds. As an example, a timing routine may be implemented as follows: The software performs a dummy I/O instruction to an unused I/O port. The hardware for the bus controller logic recognizes this I/O instruction and delays the termination of the I/O cycle to the CPU by keeping RDY# or BRDY# deasserted for the appropriate amount of time.

5.0 ELECTRICAL DATA

The following sections describe recommended electrical connections for the Intel OverDrive processor, and its electrical specifications.

5.1 Power and Grounding

5.1.1 POWER CONNECTIONS

Power and ground connections must be made to all external V_{CC} and GND pins of the Intel OverDrive processor. On the circuit board, all V_{CC} pins must be connected on a V_{CC} plane. All V_{SS} pins must be likewise connected on a GND plane.

5.1.2 POWER DECOUPLING RECOMMENDATIONS

Liberal decoupling capacitance should be placed near the Intel OverDrive processor. The Intel OverDrive processor driving its 32-bit parallel address and data busses at high frequencies can cause transient power surges, particularly when driving large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening circuit board traces between the Intel OverDrive processor and decoupling capacitors as much as possible. Capacitors specifically for PGA packages are also commercially available.

5.1.3 OTHER CONNECTION RECOMMENDATIONS

N.C. pins should always remain unconnected.

For reliable operation, always connect unused inputs to an appropriate signal level. Active LOW inputs should be connected to V_{CC} through a pullup resistor. Pullups in the range of 20 KΩ are recommended. Active HIGH inputs should be connected to GND.

5.2 Maximum Ratings

Table 5.1 is a stress rating only, and functional operation at the maximums is not guaranteed. Function operating conditions are given in Section 5.3 D.C. Specifications and Section 5.4 A.C. Specifications.

Extended exposure to the Maximum Ratings may affect device reliability. Furthermore, although the Intel OverDrive processor contains protective circuitry to resist damage from static electric discharge, always take precautions to avoid high static voltages or electric fields.

Table 5.1. Absolute Maximum Ratings

Case Temperature under Bias	−65°C to +110°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin with Respect to Ground	−0.5 to V_{CC} + 0.5V
Supply Voltage with Respect to V_{SS}	−0.5V to +6.5V

5.3 D.C. Specifications

Functional Operating Range: V_{CC} = 5V ±5%; (Note 1)

Table 5-2. DC Parametric Values

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	−0.3	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.3	V	
V_{OL}	Output Low Voltage		0.45	V	(Note 2)
V_{OH}	Output High Voltage	2.4		V	(Note 3)
I_{CC}	Power Supply Current CLK = 33 MHz CLK = 25 MHz CLK = 20 MHz CLK = 16 MHz		200 [illegible] 775 625	mA	(Note 4)
I_{LI}	Input Leakage Current		±15	µA	(Note 5)
I_{IH}	Input Leakage Current		200	µA	(Note 6)
I_{IL}	Input Leakage Current		−400	µA	(Note 7)
I_{LO}	Output Leakage Current		±15	µA	
C_{IN}	Input Capacitance		13	pF	F_C = 1 MHz (Note 8)
C_O	I/O or Output Capacitance		17	pF	F_C = 1 MHz (Note 8)
C_{CLK}	CLK Capacitance		15	pF	F_C = 1 MHz (Note 8)

NOTES:
1. The function operating temperature range is:
   OverDrive processor—20 MHz, T_{case} = 0°C to +95°C
   OverDrive processor—25 MHz, T_{sink} = 0°C to +85°C
   OverDrive processor—33 MHz, T_{sink} = 0°C to +85°C
2. This parameter is measured at:
   Address, Data, BEn 4.0 mA
   Definition, Control 5.0 mA
3. This parameter is measured at:
   Address, Data, BEn −1.0 mA
   Definition, Control −0.9 mA
4. Typical supply current:
   525 mA @ CLK = 16 MHz
   625 mA @ CLK = 20 MHz
   775 mA @ CLK = 25 MHz
   975 mA @ CLK = 33 MHz
5. This parameter is for inputs without internal pullups or pulldowns and $0 \le V_{IN} \le V_{CC}$.
6. This parameter is for inputs with internal pulldowns and V_{IH} = 2.4V.
7. This parameter is for inputs with internal pullups and V_{IL} = 0.45V.
8. Not 100% tested.

5.4 A.C. Specifications

The A.C. specifications, given in Tables 5.3.1, 5.3.2, 5.3.3, and 5.3.4, consist of output delays, input setup requirements and input hold requirements. All A.C. specifications are relative to the rising edge of the CLK signal.

A.C. specifications measurement is defined by Figures 5.1–5.6. All timings are referenced to 1.5V unless otherwise specified. Inputs must be driven to the voltage levels indicated by Figure 5.3 when A.C. specifications are measured. Intel OverDrive processor output delays are specified with minimum and maximum limits, measured as shown. The minimum Intel OverDrive processor delay times are hold times provided to external circuitry. Intel OverDrive processor input setup and hold times are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct Intel OverDrive processor operation.

Table 5.3.1. 33 MHz Intel OverDrive™ Processor A.C. Characteristics

V_{CC} = 5V ±5%; T_{sink} = 0°C to +85°C; C_l = 50 pF unless otherwise specified (Note 2)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	8	33	MHz		1X Clock Driven to OverDrive processor
t_1	CLK Period	30	125	ns	5.1	
t_{1a}	CLK Period Stability		0.1%	Δ		Adjacent Clocks
t_2	CLK High Time	11		ns	5.1	at 2V
t_3	CLK Low Time	11		ns	5.1	at 0.8V
t_4	CLK Fall Time		3	ns	5.1	2V to 0.8V
t_5	CLK Rise Time		3	ns	5.1	0.8V to 2V
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, SMIACT#, FERR#, BREQ, HLDA Valid Delay	3	14	ns	5.5	(Note 3)
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# Float Delay		20	ns	5.6	(Note 1)
t_8	PCHK# Valid Delay	3	22	ns	5.4	(Note 3)
t_{8a}	BLAST#, PLOCK# Valid Delay	3	20	ns	5.5	(Note 3)
t_9	BLAST#, PLOCK# Float Delay		20	ns	5.6	(Note 1)
t_{10}	D0–D31, DP0–3 Write Data Valid Delay	3	18	ns	5.5	(Note 3)
t_{11}	D0–D31, DP0–3 Write Data Float Delay		20	ns	5.6	(Note 1)
t_{12}	EADS# Setup Time	5		ns	5.2	
t_{13}	EADS# Hold Time	3		ns	5.2	
t_{14}	KEN#, BS16#, BS8# Setup Time	5		ns	5.2	
t_{15}	KEN#, BS16#, BS8# Hold Time	3		ns	5.2	
t_{16}	RDY#, BRDY# Setup Time	5		ns	5.3	
t_{17}	RDY#, BRDY# Hold Time	3		ns	5.3	
t_{18}	HOLD, AHOLD Setup Time	6		ns	5.2	
t_{18a}	BOFF# Setup Time	7		ns	5.2	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	3		ns	5.2	
t_{20}	RESET, FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, IGNNE# Setup Time	5		ns	5.2	
t_{21}	RESET, FLUSH#, A20M#, NMI, INTR, SMI#, STPCLK#, SRESET, IGNNE# Hold Time	3		ns	5.2	
t_{22}	D0–D31, DP0–3, A4–A31 Read Setup Time	5		ns	5.2, 5.3	
t_{23}	D0–D31, DP0–3, A4–A31 Read Hold Time	3		ns	5.2, 5.3	

NOTES:
1. Not 100% tested. Guaranteed by design characterization.
2. All timing specifications assume C_L = 50 pF. Charts 5.7.1–5.7.3 provides the charts that may be used to determine the delay due to derating, depending on the lumped capacitive loading, that must be added to these specification values.
3. The minimum Intel OverDrive processor output valid delays are hold times provided to external circuitry.
4. A reset pulse width of 15 CLK cycles is required for warm resets. Power-up resets require RESET to be asserted for at least 1 ms after V_{CC} and CLK are stable.

Table 5.3.2. 25 MHz Intel OverDrive Processor A.C. Characteristics

V_{CC} = 5V ±5%; T_{sink} = 0°C to +85°C; C_l = 50 pF unless otherwise specified (Note 2)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	8	25	MHz		1X Clock Driven to OverDrive Processor
t_1	CLK Period	40	125	ns	5.1	
t_{1a}	CLK Period Stability		0.1%	Δ		Adjacent Clocks
t_2	CLK High Time	14		ns	5.1	at 2V
t_3	CLK Low Time	14		ns	5.1	at 0.8V
t_4	CLK Fall Time		4	ns	5.1	2V to 0.8V
t_5	CLK Rise Time		4	ns	5.1	0.8V to 2V
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BREQ, HLDA, SMIACT#, Valid Delay	3	19	ns		(Note 3)
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# Float Delay		28	ns	5.6	(Note 1)
t_8	PCHK# Valid Delay	3	24	ns	5.4	(Note 3)
t_{8a}	BLAST#, PLOCK# Valid Delay	3	24	ns	5.5	(Note 3)
t_9	BLAST#, PLOCK# Float Delay		28	ns	5.6	(Note 1)
t_{10}	D0–D31, DP0–3 Write Data Valid Delay	3	20	ns	5.5	(Note 3)
t_{11}	D0–D31, DP0–3 Write Data Float Delay		28	ns	5.6	(Note 1)
t_{12}	EADS# Setup Time	8		ns	5.2	
t_{13}	EADS# Hold Time	3		ns	5.2	
t_{14}	KEN#, BS16#, BS8# Setup Time	8		ns	5.2	
t_{15}	KEN#, BS16#, BS8# Hold Time	3		ns	5.2	
t_{16}	RDY#, BRDY# Setup Time	8		ns	5.3	
t_{17}	RDY#, BRDY# Hold Time	3		ns	5.3	
t_{18}	HOLD, AHOLD, BOFF# Setup Time	8		ns	5.2	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	3		ns	5.2	
t_{20}	RESET, FLUSH#, A20M#, NMI, SMI#, STPCLK#, SRESET, INTR, IGNNE# Setup Time	8		ns	5.2	
t_{21}	RESET, FLUSH#, A20M#, NMI, SMI#, STPCLK#, SRESET, INTR, IGNNE# Hold Time	3		ns	5.2	
t_{22}	D0–D31, DP0–3, A4–A31 Read Setup Time	5		ns	5.2, 5.3	
t_{23}	D0–D31, DP0–3, A4–A31 Read Hold Time	3		ns	5.2, 5.3	

3

NOTES:
1. Not 100% tested. Guaranteed by design characterization.
2. All timing specifications assume C_L = 50 pF. Charts 5.7.1–5.7.3 provides the charts that may be used to determine the delay due to derating, depending on the lumped capacitive loading, that must be added to these specification values.
3. The minimum Intel OverDrive processor output valid delays are hold times provided to external circuitry.
4. A reset pulse width of 15 CLK cycles is required for warm resets. Power-up resets require RESET to be asserted for at least 1 ms after V_{CC} and CLK are stable.

Table 5.3.3. 20 MHz Intel OverDrive Processor A.C. Characteristics

V_{CC} = 5V ±5%; T_{case} = 0°C to +95°C; C_l = 50 pF unless otherwise specified (Note 2)

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	8	20	MHz		1X Clock Driven to OverDrive Processor
t_1	CLK Period	50	125	ns	5.1	
t_{1a}	CLK Period Stability		0.1%	Δ		Adjacent Clocks
t_2	CLK High Time	16		ns	5.1	at 2V
t_3	CLK Low Time	16		ns	5.1	at 0.8V
t_4	CLK Fall Time		6	ns	5.1	2V to 0.8V
t_5	CLK Rise Time		6	ns	5.1	0.8V to 2V
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BREQ, HLDA, SMIACT# Valid Delay	3	23	ns	5.5	(Note 3)
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# Float Delay		37	ns	5.6	(Note 1)
t_8	PCHK# Valid Delay	3	26	ns	5.4	(Note 3)
t_{8a}	BLAST#, PLOCK# Valid Delay	3	26	ns	5.5	(Note 3)
t_9	BLAST#, PLOCK# Float Delay		37	ns	5.6	(Note 1)
t_{10}	D0–D31, DP0–3 Write Data Valid Delay	3	26	ns	5.5	(Note 3)
t_{11}	D0–D31, DP0–3 Write Data Float Delay		37	ns	5.6	(Note 1)
t_{12}	EADS# Setup Time	10		ns	5.2	
t_{13}	EADS# Hold Time	3		ns	5.2	
t_{14}	KEN#, BS16#, BS8# Setup Time	10		ns	5.2	
t_{15}	KEN#, BS16#, BS8# Hold Time	3		ns	5.2	
t_{16}	RDY#, BRDY# Setup Time	10		ns	5.3	
t_{17}	RDY#, BRDY# Hold Time	3		ns	5.3	
t_{18}	HOLD, AHOLD, Setup Time	12		ns	5.2	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	3		ns	5.2	
t_{20}	RESET, FLUSH#, A20M#, NMI, SMI#, STPCLK#, SRESET, INTR, IGNNE# Setup Time	12		ns	5.2	(Note 4)
t_{21}	RESET, FLUSH#, A20M#, NMI, SMI#, STPCLK#, SRESET, INTR, IGNNE# Hold Time	3		ns	5.2	(Note 4)
t_{22}	D0–D31, DP0–3, A4–A31 Read Setup Time	6		ns	5.2, 5.3	
t_{23}	D0–D31, DP0–3, A4–A31 Read Hold Time	3		ns	5.2, 5.3	

NOTES:
1. Not 100% tested. Guaranteed by design characterization.
2. All timing specifications assume C_L = 50 pF. Charts 5.7.1–5.7.3 provides the charts that may be used to determine the delay due to derating, depending on the lumped capacitive loading, that must be added to these specification values.
3. The minimum Intel OverDrive processor output valid delays are hold times provided to external circuitry.
4. A reset pulse width of 15 CLK cycles is required for warm resets. Power-up resets require RESET to be asserted for at least 1 ms after V_{CC} and CLK are stable.

Table 5.3.4. 16 MHz Intel OverDrive Processor A.C. Characteristics

V_{CC} = 5V ±5%; T_{case} = 0°C to +95°C; C_l = 50 pF unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	8	16	MHz		1X Clock Driven to OverDrive Processor
t_1	CLK Period	62.5	125	ns	5.1	
t_{1a}	CLK Period Stability		0.1%	Δ		Adjacent Clocks
t_2	CLK High Time	20		ns	5.1	at 2V
t_3	CLK Low Time	20		ns	5.1	at 0.8V
t_4	CLK Fall Time		8	ns	5.1	2V to 0.8V
t_5	CLK Rise Time		8	ns	5.1	0.8V to 2V
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, FERR#, BREQ, HLDA, SMIACT# Valid Delay	3	26	ns	5.5	(Note 3)
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# Float Delay		42	ns	5.6	(Note 1)
t_8	PCHK# Valid Delay	3	30	ns	5.4	(Note 3)
t_{8a}	BLAST#, PLOCK# Valid Delay	3	30	ns	5.5	(Note 3)
t_9	BLAST#, PLOCK# Float Delay		42	ns	5.6	(Note 1)
t_{10}	D0–D31, DP0–3 Write Data Valid Delay	3	30	ns	5.5	(Note 3)
t_{11}	D0–D31, DP0–3 Write Data Float Delay		42	ns	5.6	(Note 1)
t_{12}	EADS# Setup Time	12		ns	5.2	
t_{13}	EADS# Hold Time	4		ns	5.2	
t_{14}	KEN#, BS16#, BS8# Setup Time	12		ns	5.2	
t_{15}	KEN#, BS16#, BS8# Hold Time	4		ns	5.2	
t_{16}	RDY#, BRDY# Setup Time	12		ns	5.3	
t_{17}	RDY#, BRDY# Hold Time	4		ns	5.3	
t_{18}	HOLD, AHOLD, BOFF# Setup Time	12		ns	5.2	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	4		ns	5.2	
t_{20}	RESET, FLUSH#, A20M#, NMI, SMI#, STPCLK#, SRESET, INTR, IGNNE# Setup Time	14		ns	5.2	(Note 4)
t_{21}	RESET, FLUSH#, A20M#, NMI, SMI#, STPCLK#, SRESET, INTR, IGNNE# Hold Time	4		ns	5.2	(Note 4)
t_{22}	D0–D31, DP0–3, A4–A31 Read Setup Time	10		ns	5.2, 5.3	
t_{23}	D0–D31, DP0–3, A4–A31 Read Hold Time	4		ns	5.2, 5.3	

NOTES:
1. Not 100% tested. Guaranteed by design characterization.
2. All timing specifications assume C_L = 50 pF. Charts 5.7.1–5.7.3 provides the charts that may be used to determine the delay due to derating, depending on the lumped capacitive loading, that must be added to these specification values.
3. The minimum Intel OverDrive processor output valid delays are hold times provided to external circuitry.
4. A reset pulse width of 15 CLK cycles is required for warm resets. Power-up resets require RESET to be asserted for at least 1 ms after V_{CC} and CLK are stable.

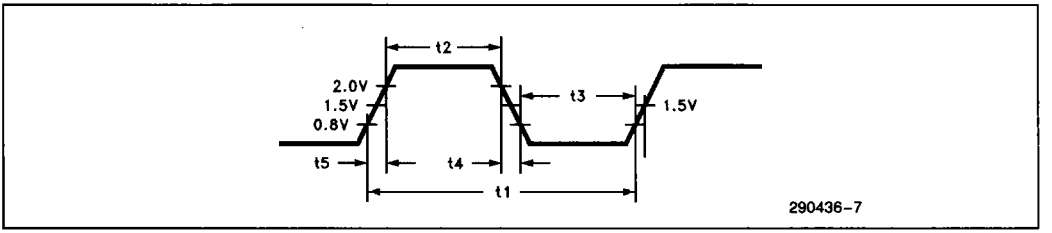


Figure 5.1. CLK Waveforms

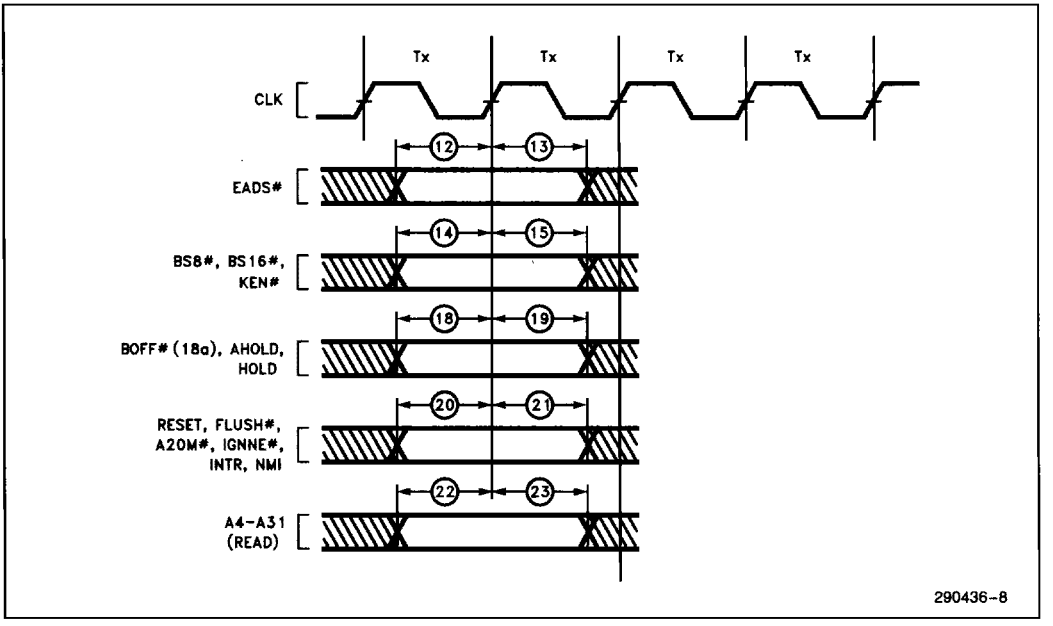


Figure 5.2. Input Setup and Hold Timing

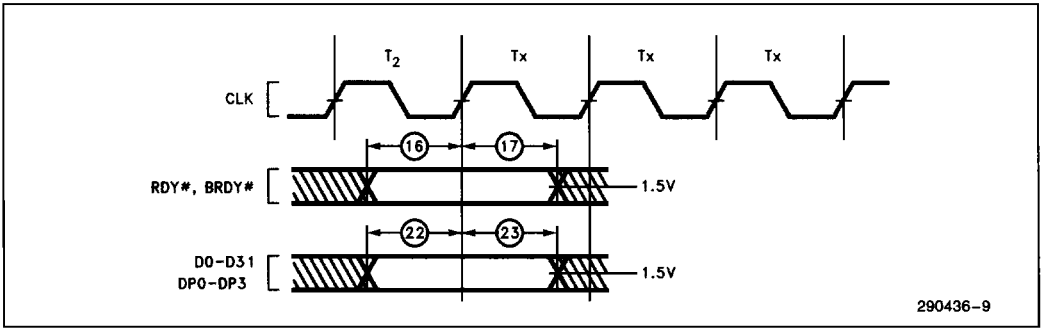


Figure 5.3. Input Setup and Hold Timing

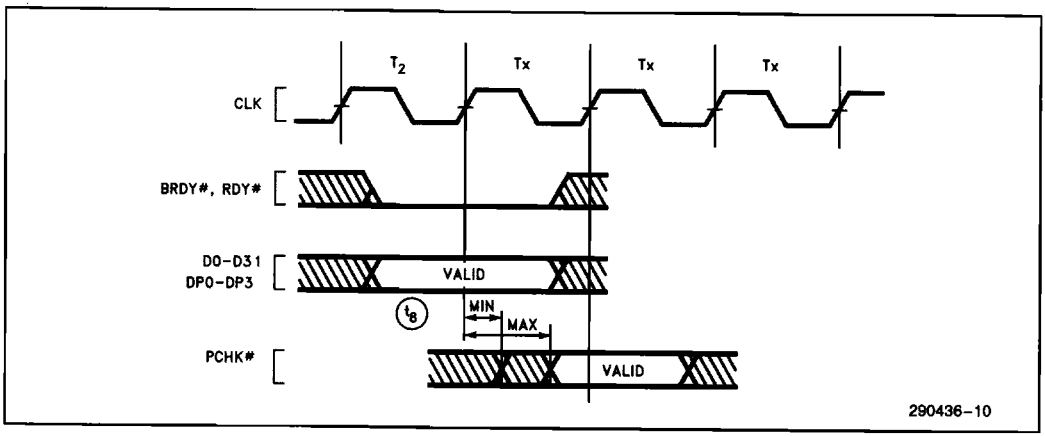


Figure 5.4. PCHK# Valid Delay Timing

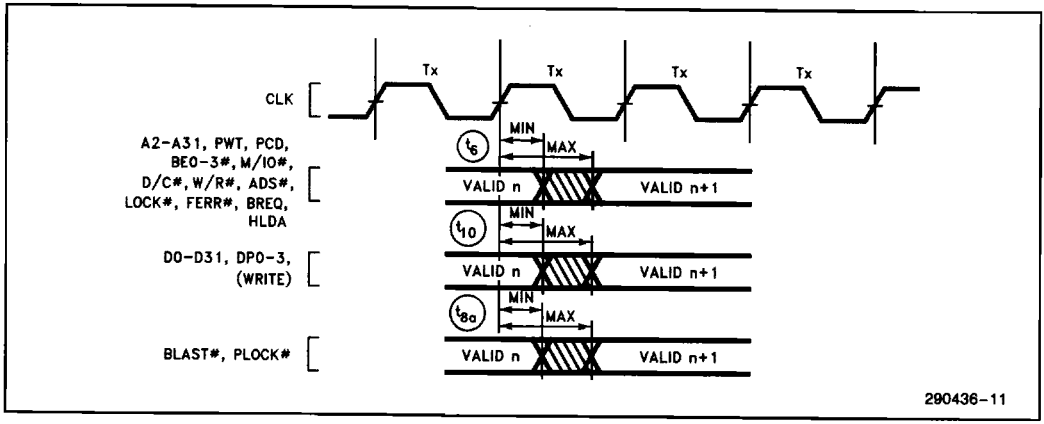


Figure 5.5. Output Valid Delay Timing

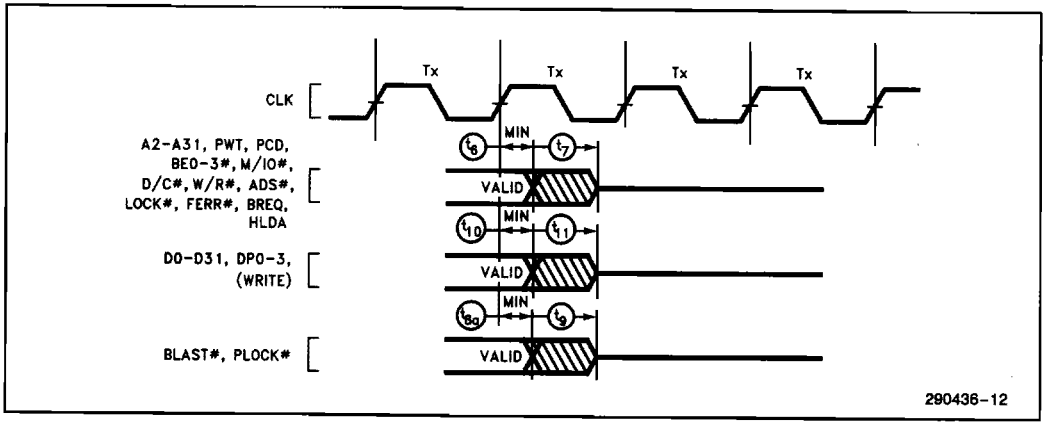
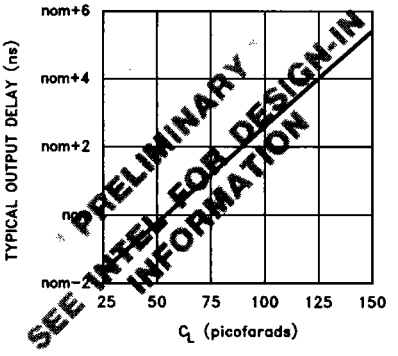


Figure 5.6. Maximum Float Delay Timing

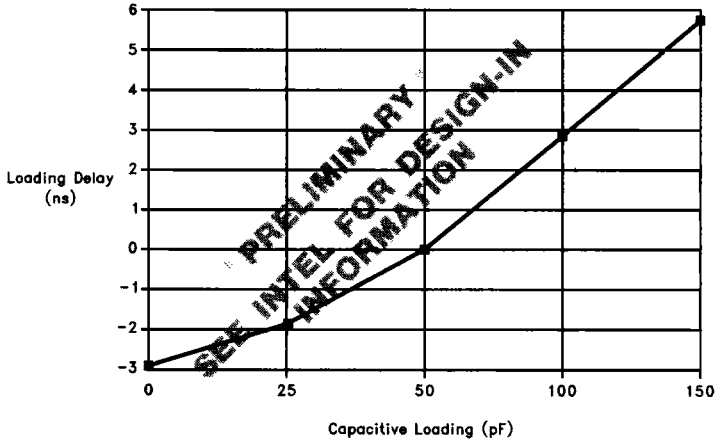
5.7.1 TYPICAL OUTPUT VALID DELAY VERSUS LOAD CAPACITANCE UNDER WORST CASE CONDITIONS FOR THE Intel OverDrive PROCESSOR



290436-13

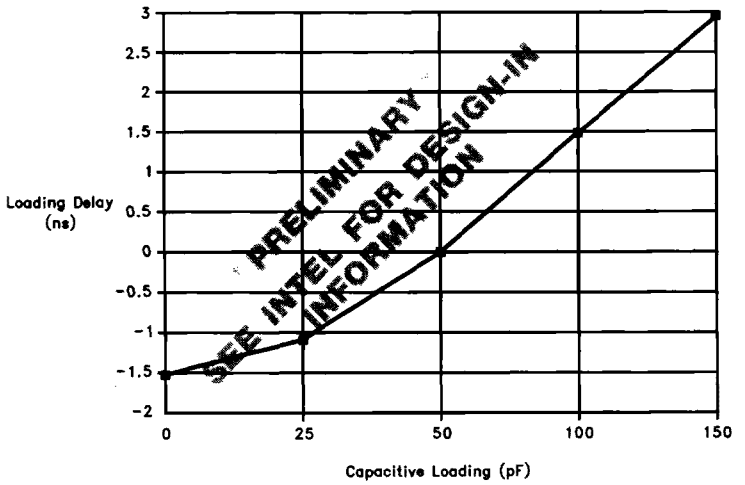
NOTES:
This graph will not be linear outside of the C_L range shown.
nom = nominal value given in A.C. Characteristics table.

5.7.2a TYPICAL LOADING DELAY VERSUS CAPACITIVE LOADING UNDER WORST-CASE CONDITIONS FOR A HIGH TO LOW TRANSITION ON THE Intel OverDrive PROCESSOR



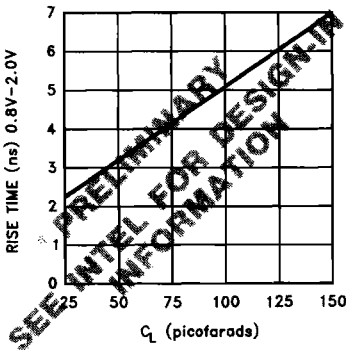
290436-14

5.7.2b TYPICAL LOADING DELAY VERSUS CAPACITIVE LOADING UNDER WORST-CASE CONDITIONS FOR A LOW TO HIGH TRANSITION ON THE Intel OverDrive PROCESSOR



290436-15

5.7.3 TYPICAL OUTPUT RISE TIME VERSUS LOAD CAPACITANCE UNDER WORST-CASE CONDITIONS

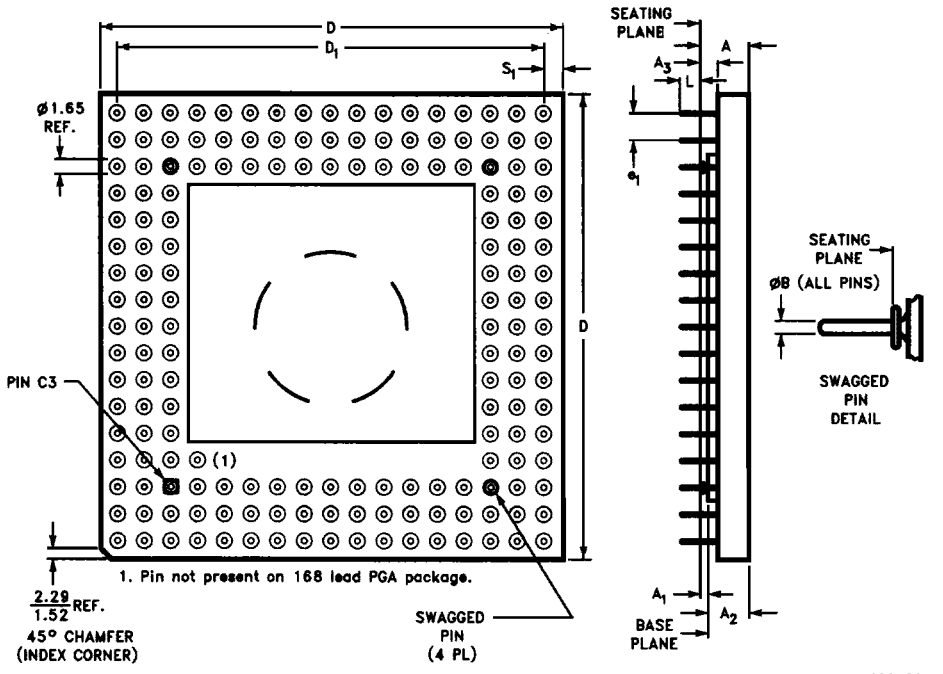


290436-16

NOTE:
This graph will not be linear outside of the C_L range shown.

6.0 MECHANICAL DATA

6.1 Package Dimensions



Family: Ceramic Pin Grid Array Package						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	3.56	4.57		0.140	0.180	
A_1	0.64	1.14	SOLID LID	0.025	0.045	SOLID LID
A_2	2.8	3.5	SOLID LID	0.110	0.140	SOLID LID
A_3	1.14	1.40		0.045	0.055	
B	0.43	0.51		0.017	0.020	
D	44.07	44.83		1.735	1.765	
D_1	40.51	40.77		1.595	1.605	
e_1	2.29	2.79		.090	0.110	
L	2.54	3.30		0.100	0.130	
N	168, 169			168, 169		
S_1	1.52	2.54		0.060	0.100	
ISSUE	IWS REV X 7/15/88					

Figure 6.1. 168 and 169 Lead Ceramic PGA Package Dimensions

Table 6.1. Ceramic PGA Package Dimension Symbols

Letter or Symbol	Description of Dimensions
A	Distance from seating plane to highest point of body
A_1	Distance between seating plane and base plane (lid)
A_2	Distance from base plane to highest point of body
A_3	Distance from seating plane to bottom of body
B	Diameter of terminal lead pin
D	Largest overall package dimension of length
D_1	A body length dimension, outer lead center to outer lead center
e_1	Linear spacing between true lead position centerlines
L	Distance from seating plane to end of lead
S_1	Other body dimension, outer lead center to edge of body

NOTES:
1. Controlling dimension: millimeter.
2. Dimension "e_1" ("e") is non-cumulative.
3. Seating plane (standoff) is defined by P.C. board hole size: 0.0415–0.0430 inch.
4. Dimensions "B", "B_1" and "C" are nominal.
5. Details of Pin 1 identifier are optional.

3

6.2 Heat Sink Dimensions

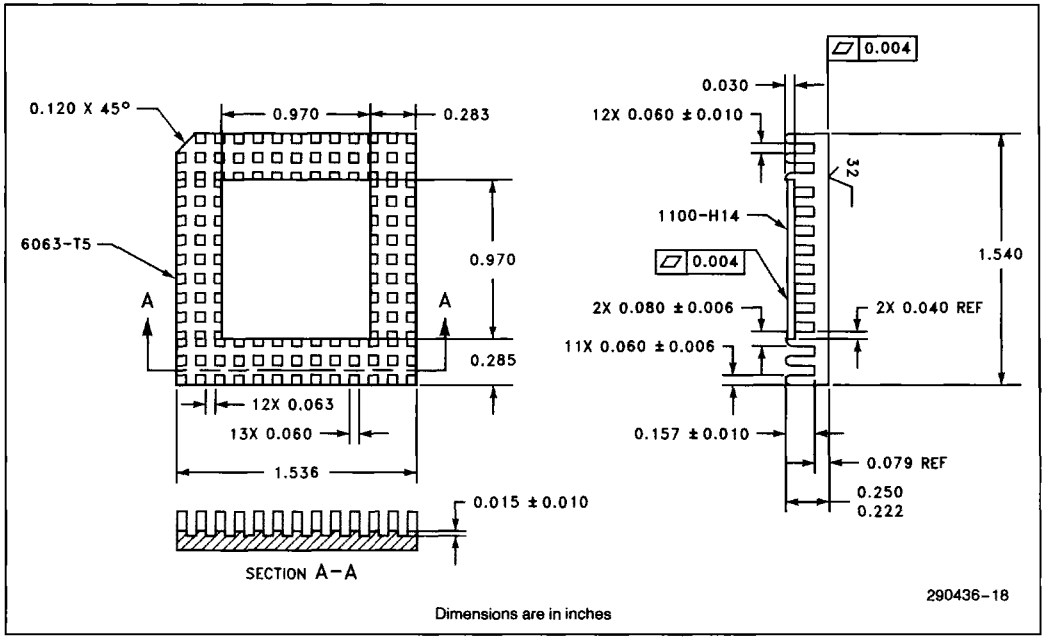


Figure 6.2. Intel OverDrive™ Processor Heat Sink Dimensions

7.0 THERMAL MANAGEMENT

The heat generated by the Intel OverDrive processor requires that heat dissipation be managed carefully. The 33 MHz and 25 MHz Intel OverDrive processors are supplied with a heat sink attached with adhesive to the package. 33 MHz and 25 MHz system designs must, therefore, provide space for the heat sink on the Intel OverDrive processor.

7.1 The Intel OverDrive™ Processor with Attached Heat Sink

The heat sink for the Intel OverDrive processor is adhesively attached to the standard PGA package. Figure 7.1 shows a drawing of the Intel OverDrive processor with the heat sink (see Table 7.1 for dimensions).

The maximum and minimum dimensions for the PGA package with heat sink are shown in Table 7.1.

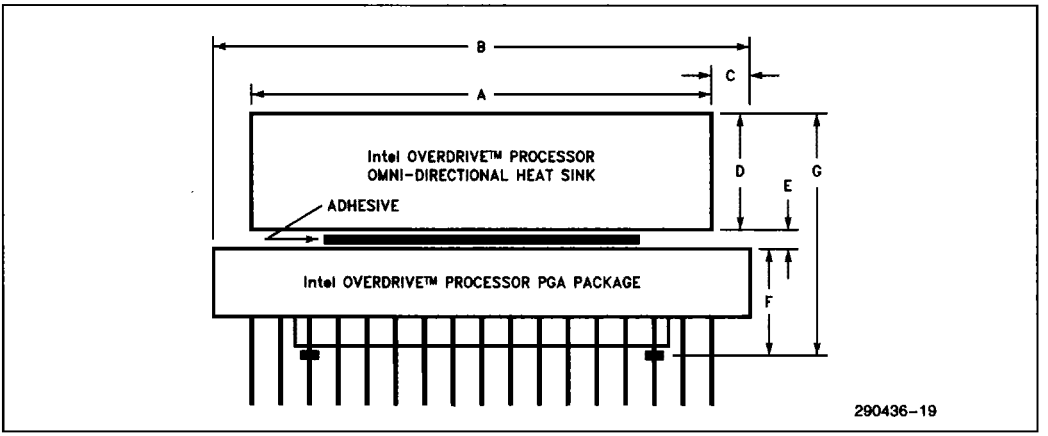


Figure 7.1. OverDrive™ Processor PGA Package with Heat Sink

Table 7.1. Intel OverDrive™ Processor PGA Package Dimensions with Heat Sink Attached

Dimension (Inches)	Min	Max
A. Heat Sink Width	1.520	1.550
B. PGA Package Width	1.735	1.765
C. Heat Sink Edge Gap	0.065	0.155
D. Heat Sink Height	0.212	0.260
E. Adhesive Thickness	0.008	0.012
F. Package Height from Stand-Offs	0.140	0.180
G. Total Height from Package Stand-Offs to Top of Heat Sink	0.360	0.452

The standard product markings and logo for the Intel OverDrive processor with the attached heat sink will be included on a 1 in^2 plate located on the top, center of the heat sink. The heat sink is omni-directional which allows the air to flow from any direction to achieve adequate cooling. The thermal resistance values for the Intel OverDrive processor with attached heat sink are shown in Table 7.2.

Table 7.2. Thermal Resistance for the Intel OverDrive™ Processor with Attached Heat Sink

θ_{JS} = 2.5°C/W	Airflow (Ft/min, LFM)				
	0	200	400	600	800
θ_{JA}(°C/W)	14.0*	10.0	7.5	6.2	5.7

NOTE:
*The thermal resistance from junction to ambient (θ_{JA}) in static air is actually a linear function of power dissipation. The value shown in the table (14.0°C/W) represents the worst case expected value which is derived from a power dissipation of 2.9W. The maximum expected power dissipation of 6W yields a θ_{JA} value of 13.1°C/W.

7.2 Intel OverDrive™ Processor without Heat Sink

The 20 MHz Intel OverDrive processor, for 16 MHz and 20 MHz i486 SX CPU systems, is supplied without a heat sink. Table 7.3 contains the thermal resistance values for the Intel OverDrive processor without heat sink.

Table 7.3. Thermal Resistance for the Intel OverDrive™ Processor without Heat Sink

θ_{JC} = 2.0°C/W	Airflow (Ft/min, LFM)				
	0	200	400	600	800
θ_{JA}(°C/W)	19.0*	16.0	12.5	11.0	10.0

NOTE:
*The thermal resistance from junction to ambient (θ_{JA}) in static air is actually a linear function of power dissipation. The value shown in the table (19.0°C/W) represents the worst case expected value which is derived from a power dissipation of 2.9W. The maximum expected power dissipation of 4W yields a θ_{JA} value of 18.5°C/W.

7.3 Thermal Equations

The methodology for calculating the heat dissipation for the 20 MHz Intel OverDrive processor (without a heat sink) and the 25 MHz or 33 MHz Intel OverDrive processor (with a heat sink) is identical except that the reference point for measuring the product temperature is different. The 20 MHz Intel OverDrive processor specifies T_{case} (the temperature at the outside center of the PGA package, opposite the pins—see Figure 7.2) and θ_{JC} (the thermal resistance from the silicon junction to the package case) but the 25 MHz and 33 MHz Intel OverDrive processor specifies T_{sink} (the temperature at the outside center base of the heat sink, not on the heat sink marking plate or cooling posts—see Figure 7.3) and θ_{JS} (the thermal resistance from the silicon junction to the heat sink base). The relationships between temperature, thermal resistance and power are shown in the following equations:

$$T_{case} = T_{ambient} + (P_{max} * \theta_{CA}) \text{ and}$$

$$T_{sink} = T_{ambient} + (P_{max} * \theta_{SA})$$

where,

$T_{ambient}$ = Ambient Temperature

P_{max} = Power ($I_{CC} * V_{CC}$),

$\theta_{CA} = \theta_{JA} - \theta_{JC}$,

$\theta_{SA} = \theta_{JA} - \theta_{JS}$.

3

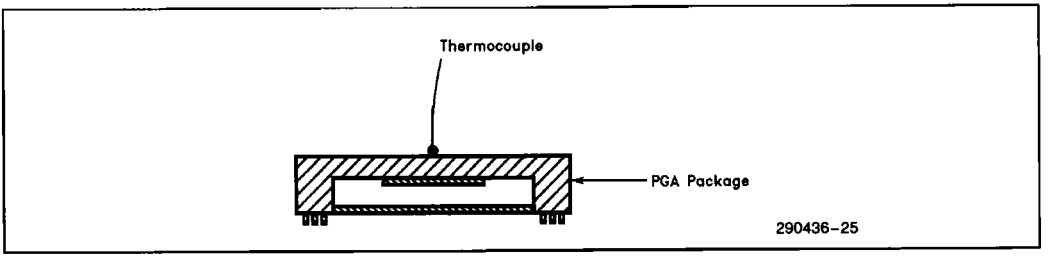


Figure 7.2. Case Temperature Measurement without Heat Sink (0.005" Dia. Thermocouple on the Center of Package Top Surface with a 90° Angle Adhesive Bond)

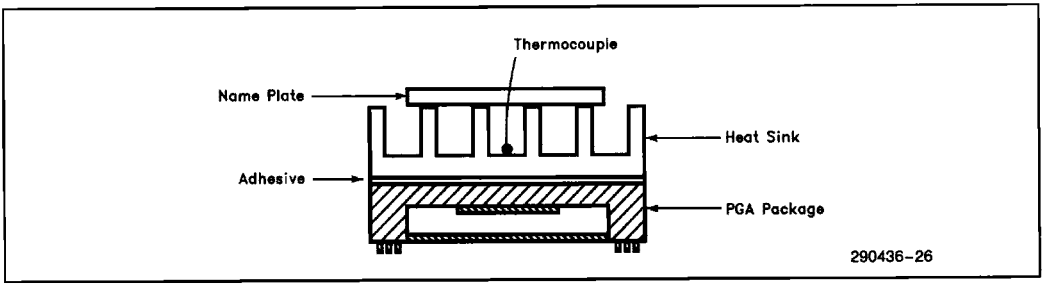


Figure 7.3. Heat Sink Measurement (0.005" Dia. Thermocouple on the Center of Heat Sink with a 90° Angle Adhesive Bond through a Hole Drilled through the Center of the Name Plate)

The maximum allowable ambient temperature as computed from these thermal equations is shown in Table 7.4.

Table 7.4. T_A (°C) for the OverDrive™ Processor

	f_{CLK} (MHz)	Airflow—Linear ft/min (m/sec)				
		0 (0)	200 (1.01)	400 (2.03)	600 (3.04)	800 (4.06)
OverDrive Processor without Heat Sink(1)	16	42	51	62	67	70
	20	29	41	54	60	64
OverDrive Processor with Heat Sink(2)	25	30	49	61	67	70
	33	16	40	55	63	66

NOTES:
1. The 20 MHz OverDrive processor does not have a heat sink.
2. The 25 MHz and 33 MHz OverDrive processors have a heat sink attached.

APPENDIX A
"END USER EASY" UPGRADABILITY*

PC buyers value easy and safe upgrade installation. PC manufacturers can make the Intel OverDrive processor installation in the Intel OverDrive processor socket simple and foolproof for the end user and reseller by implementing the suggestions listed in Table A-1.

Table A-1. Socket and Layout Considerations

"End User Easy" Feature	Implementation
Visible OverDrive Processor Socket	The Intel OverDrive processor socket should be easily visible when the PC's cover is removed. Label the Intel OverDrive processor socket and the location of pin 1 by silk screening this information on the PC board.
Accessible OverDrive Processor Socket	Make the Intel OverDrive processor socket easily accessible to the end user (i.e., do not place the Intel OverDrive processor socket under a disk drive). If a Low Insertion Force (LIF) or screw machine socket is used, position the Intel OverDrive processor socket on the PC board such that there is ample clearance around the socket.
Foolproof Chip Orientation	Intel packages all Intel OverDrive processors in a 169-pin, PGA package. The 169th pin is called the "key" pin and insures that the Intel OverDrive processor fits into a 169-pin socket in only the correct orientation. Supplying a 169-pin socket as the Intel OverDrive processor socket eliminates the possibility of end users or resellers damaging the PC board or Intel OverDrive processor by powering up the system with the Intel OverDrive processor incorrectly oriented.
Zero Insertion Force Upgrade Socket	The high pin count of the Intel OverDrive processor makes the insertion force required for installation in a screw machine PGA socket excessive for end users or resellers. Even most Low Insertion Force (LIF) sockets often require more than 60 lbs. of insertion force. A Zero Insertion Force (ZIF) socket insures that the chip insertion force does not damage the PC board. If the ZIF socket has a handle, be sure to allow enough clearance for the socket handle. If a LIF or screw machine socket is used, additional PC board support is recommended.
"Plug and Play"	Jumper or switch changes should not be needed to electrically configure the system for the Intel OverDrive processor.
Thorough Documentation	Describe the Intel OverDrive processor's installation procedure in the PC's User's Manual.

*This section applies to the 169-lead PGA versions of the OverDrive processor only. The "End-User Easy" criteria have been incorporated into the OverDrive Ready program. OverDrive Ready is a trademark of Intel Corp.

APPENDIX B
ZIF and LIF SOCKET VENDORS

The following lists provide examples of sockets which can be used as the Intel OverDrive socket for Intel486 SX and Intel486 DX CPU based systems.

NOTE:
This is not a comprehensive list. Intel has not tested the sockets listed below and cannot guarantee that these sockets will meet every PC manufacturer's specific requirements.

Zero Insertion Force Upgrade Sockets and Vendors:

1. AMP Inc.
   P.O. Box 3608
   Harrisburg, PA 17105-3608
   Tel: (800) 522-6752
   Part Number: 55287-3
   Contact: Rick Simonic, New Product Manager
   (717) 561-6143

2. Augat Inc.
   425 John Dietsch Blvd.
   Attleboro Falls, MA 02763
   (508) 699-9800

3. Aries Electronics
   P.O. Box 130
   Frenchtown, NJ 08825
   Tel: (908) 996-6841
   Part Number: 169-PRS17012-10
   Contact: Frank Folmsbee, Marketing Manager
   (908) 996-6841

4. JAE
   599 N. Mathilda Ave., Suite 8
   Sunnyvale, CA 94086
   Tel: (408) 733-0493
   Part Number: PCPS-169-002
   Contact: Bob Gerleman, Western Sales Manager
   (408) 733-0493

5. Thomas and Betts
   200 Executive Center Drive
   P.O. Box 24901
   Greenville, SC 29616-2401
   Tel: (803) 676-2900
   Part Number: PGA169A17-S-1AC
   Contact: Scott Roland,
   Product Marketing Manager
   (803) 676-2910

6. Yamaichi Electronics
   1420 Koll Circle, Suite B
   San Jose, CA 95112
   Tel: (408) 452-0797
   Part Number: NP111-16911-G4
   Contact: Jim Bennett, Sales Manager
   (408) 452-0797

Low Insertion Force Sockets and Vendors:

1. AMP Inc.
   P.O. Box 3608
   Harrisburg, PA 17105-3608
   Tel: (800) 522-6752
   Part Number:
   (Premium Base Material) 55589-5
   (Standard Base Material) 916227-3

2. Thomas and Betts
   200 Executive Center Drive
   P.O. Box 24901
   Greenville, SC 29616-2401
   Tel: (803) 676-2900
   Part Number: LPG169A17-S-1AC