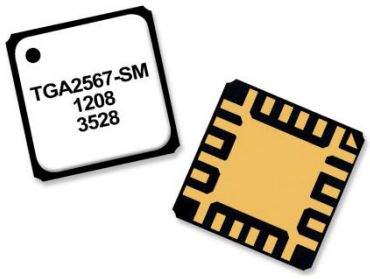
# TGA2567-SM

***2-20 GHz LNA Amplifier***

## Applications

- General Purpose LNA/Gain Block
- Point to Point Radio
- Electronic Warfare
- Military & Commercial Radar
- Communications

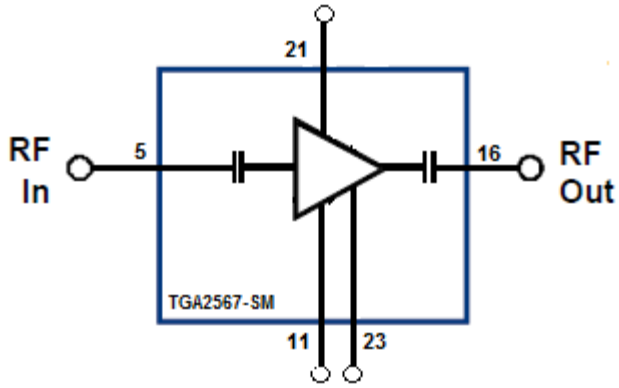



QFN 4x4mm 24L

## Product Features

- Frequency Range: 2 – 20 GHz
- $P_{SAT}$ : 22 dBm
- $P_{1dB}$ : 19 dBm
- Small Signal Gain: 17 dB
- Adjustable Gain Range
- Output TOI: 29 dBm
- Noise Figure: 2 dB
- Bias: $V_D$ = 5 V, $I_{DQ}$ = 100 mA, $V_{G1}$ = -0.7 V, $V_{G2}$ = +1.3 V Typical
- ESD Protection Circuitry on $V_D$ , $V_{G1}$ and $V_{G2}$
- Package Dimensions: 4.0 x 4.0 x 1.42 mm

## Functional Block Diagram




## General Description

TriQuint's TGA2567-SM is a LNA Gain Block fabricated on TriQuint's proven 0.15um pHEMT production process.

The TGA2567-SM operates from 2 to 20 GHz and typically provides 19 dBm of 1dB compressed output power with 17 dB of small signal gain. Greater than 16 dB of adjustable gain can be achieved by varying $V_{G2}$. The Noise Figure is typically 2 dB at mid band

The TGA2567-SM is available in a low-cost, surface mount 24 lead 4x4 AIN QFN package base with an Air cavity LCP lid. TGA2567-SM is ideally suited to support both commercial and defense related applications.

Lead-free and RoHS compliant.

Evaluation Boards are available upon request.

## Pad Configuration

| Pad No. | Symbol |
|---|---|
| 1,2,4,6,7,12,13,15,17-19,24,25 | GND |
| 3,8-10,14,20,22 | N/C |
| 5 | RF IN |
| 11 | $V_{G1}$ |
| 16 | RF OUT |
| 21 | $V_D$ |
| 23 | $V_{G2}$ |

## Ordering Information

| Part | ECCN | Description |
|---|---|---|
| TGA2567-SM | EAR99 | 2 – 20 GHz LNA / Gain Block |

## Absolute Maximum Ratings

| Parameter | Value |
|---|---|
| Drain Voltage ($V_D$) | 6 V |
| Drain to Gate Voltage ($V_D$-$V_{G1}$) | 8 V |
| Gate Voltage Range ($V_{G1}$) | -2 to 1 V |
| Gate Voltage Range ($V_{G2}$) | -2 to +4 V |
| Drain Current ($I_D$) | 160 mA |
| Gate Current ($I_{G1}$, $I_{G2}$) | -1 to 40 mA |
| Power Dissipation ($P_{DISS}$) | 2.8 W |
| RF Input Power, CW, 50 Ω, T = 25 °C ($P_{IN}$) | +22 dBm |
| Channel Temperature ($T_{CH}$) | 200 °C |
| Mounting Temperature (30 Seconds) | 260 °C |
| Storage Temperature | -55 to 150 °C |

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

## Recommended Operating Conditions

| Parameter | Value |
|---|---|
| Drain Voltage ($V_D$) | 5 V |
| Drain Current ($I_{DQ}$) | 100 mA |
| Gate Voltage ($V_{G1}$) | -0.7 V (Typ.) |
| Gate Voltage ($V_{G2}$) | 1.3 V |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

## Electrical Specifications

Test conditions unless otherwise noted: 25 °C, $V_D$ = 5 V, $I_{DQ}$ = 100 mA , $V_{G1}$ = -0.7 V, $V_{G2}$ = 1.3 V

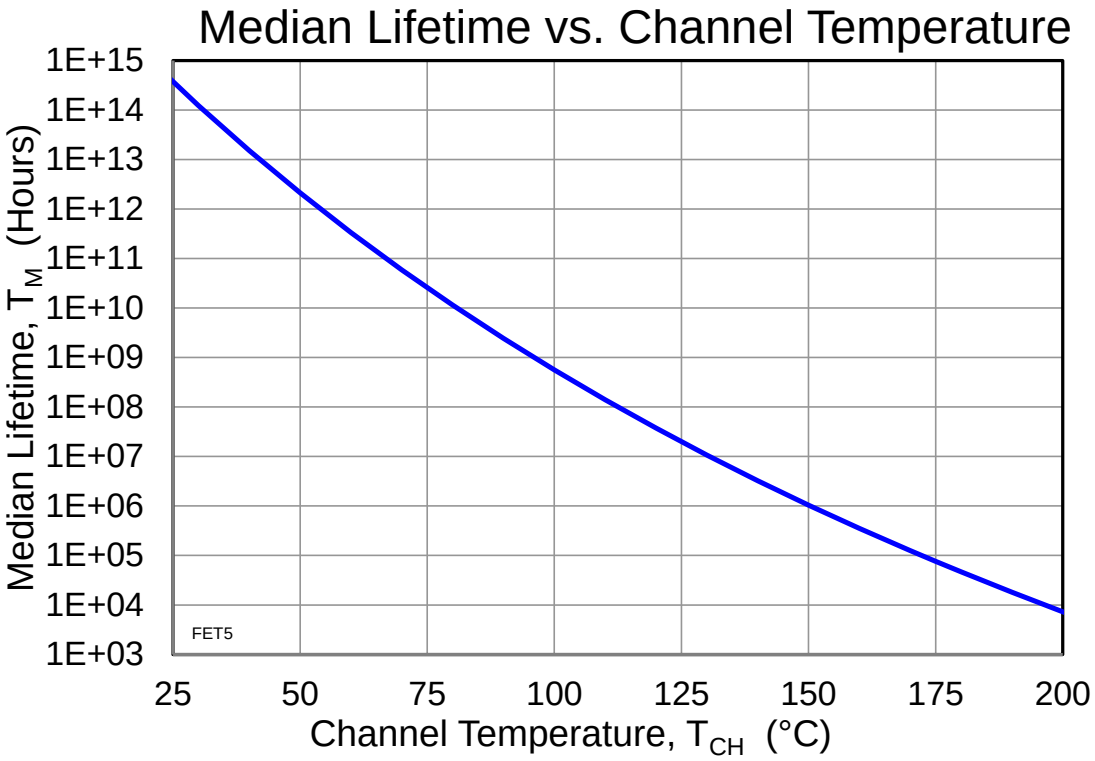
| Parameter | Min | Typical | Max | Units |
|---|---|---|---|---|
| Operational Frequency Range | 2 | | 20 | GHz |
| Small Signal Gain | | 17 | | dB |
| Input Return Loss | | 15 | | dB |
| Output Return Loss | | 14 | | dB |
| Output Power at Saturation | | 22 | | dBm |
| Output Power at P1dB | | 19 | | dBm |
| Output TOI | | 29 | | dBm |
| Noise Figure | | 2 | | dB |
| Gain Temperature Coefficient | | 0.013 | | dB/°C |
| Noise Temperature Coefficient | | 0.009 | | dB/°C |

## Thermal and Reliability Information

| Parameter | Test Conditions | Value | Units |
|---|---|---|---|
| Thermal Resistance, $\theta_{JC\ (1)}$ | Tbaseplate = 85 °C | 41 | ºC/W |
| Channel Temperature, $T_{CH}$ (Without RF Drive) | Tbaseplate = 85 °C, $V_D$ = 5 V, $I_{DQ}$ = 100 mA, $P_{DISS}$ = 0.5 W | 106 | °C |
| Median Lifetime, $T_M$ (Without RF Drive) | | 2.4 x 10^8 | Hrs |
| Channel Temperature, $T_{CH}$ (Under RF Drive) | Tbaseplate = 85 °C, $V_D$ = 5 V, $I_{DD}$ = 156 mA, $P_{OUT}$ = 22.8 dBm, $P_{DISS}$ = 0.59 W | 109 | °C |
| Median Lifetime, $T_M$ (Under RF Drive) | | 1.6 x 10^8 | Hrs |

Notes: (1) Thermal resistance measured to back of package.

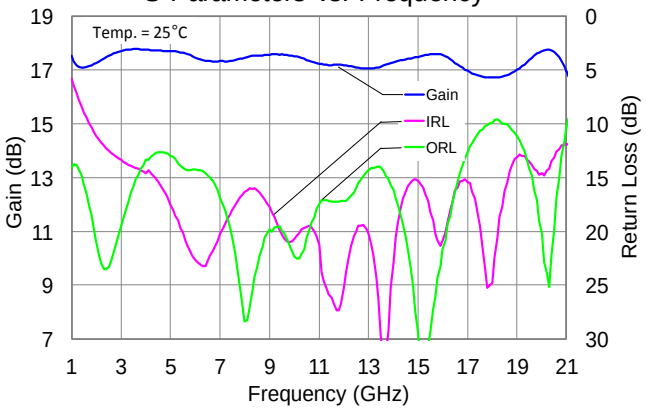
## Median Lifetime



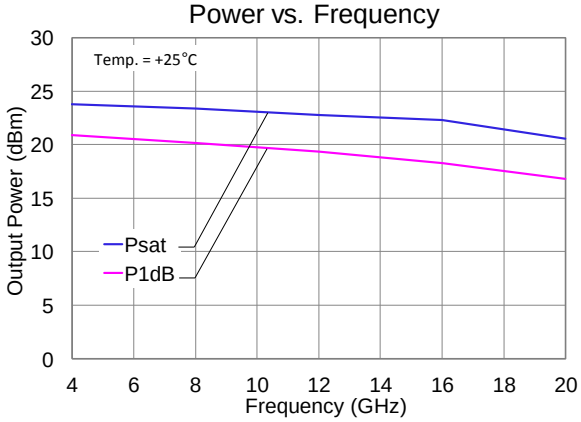
## Typical Performance

Conditions unless otherwise specified: $V_D$ = 5 V, $I_{DQ}$ = 100 mA, $V_{G1}$ = -0.7 V Typical, $V_{G2}$ = 1.3 V.

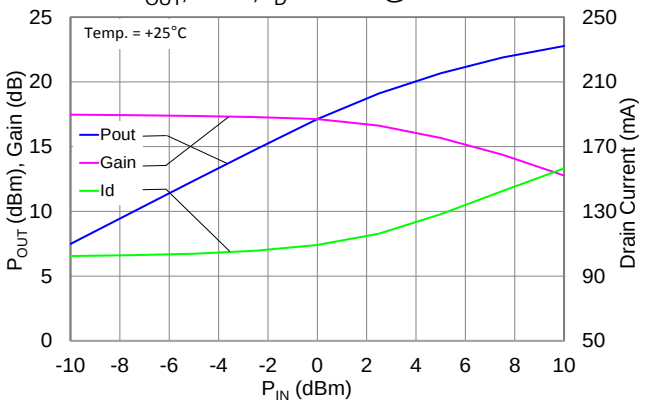
S-Parameters vs. Frequency



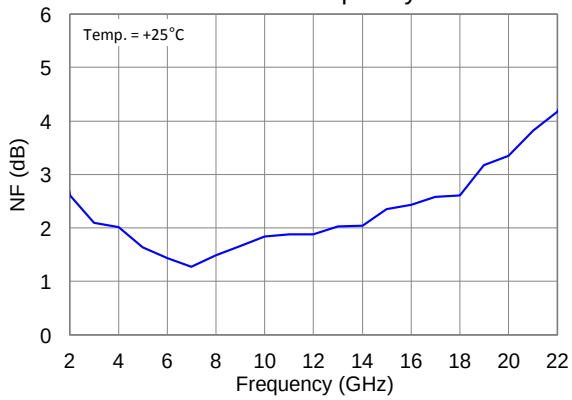

Power vs. Frequency



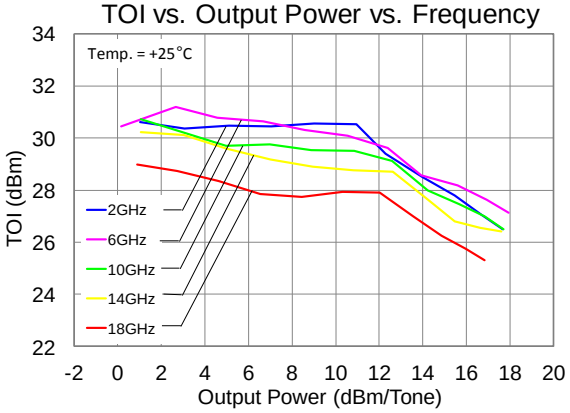

$P_{OUT}$, Gain, $I_D$ vs. Pin @ 12 GHz



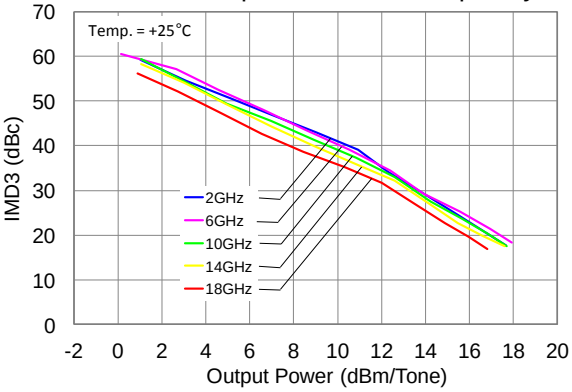

NF vs. Frequency




TOI vs. Output Power vs. Frequency



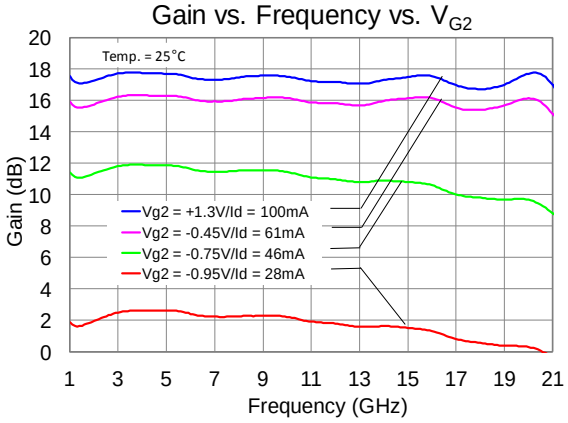

IMD3 vs. Output Power vs. Frequency



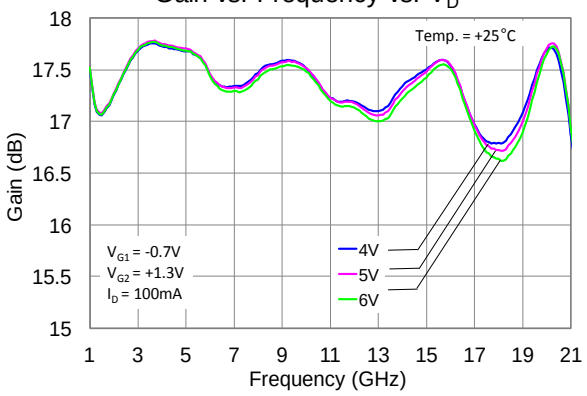
## Typical Performance

Conditions unless otherwise specified: $V_D$ = 5 V, $I_{DQ}$ = 100 mA, $V_{G1}$ = -0.7 V Typical, $V_{G2}$ = 1.3 V.

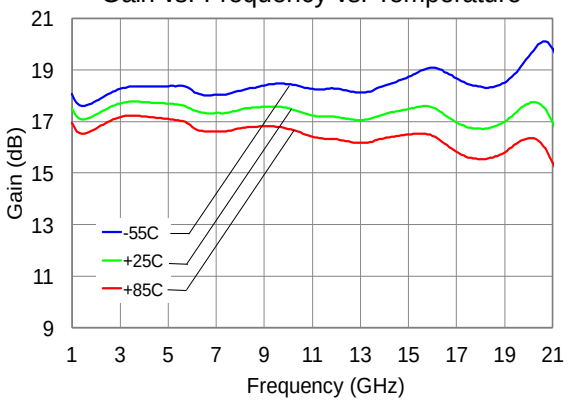
Gain vs. Frequency vs. $V_{G2}$



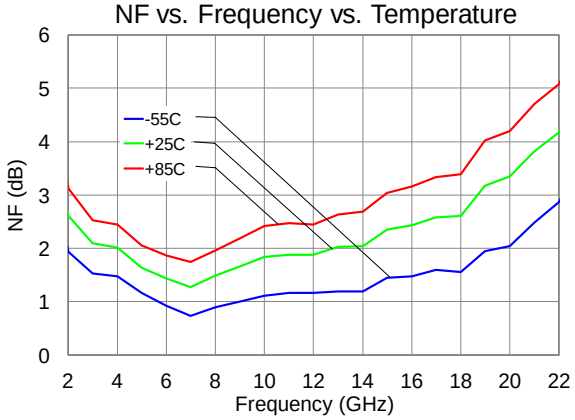

Gain vs. Frequency vs. $V_D$



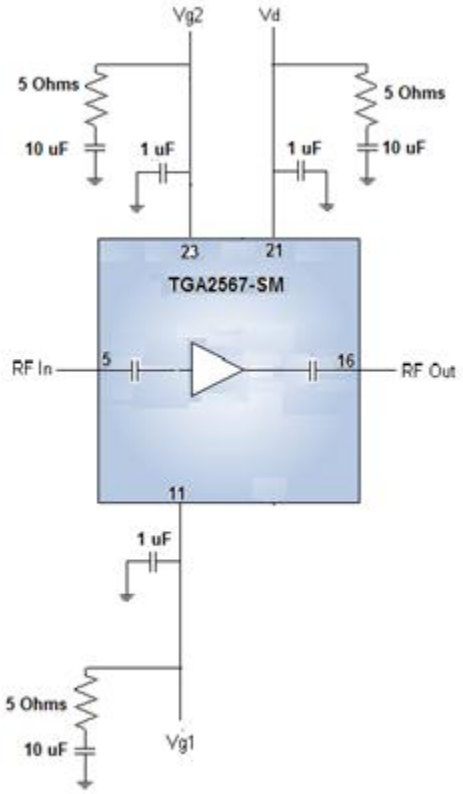

Gain vs. Frequency vs. Temperature




NF vs. Frequency vs. Temperature



## Application Circuit




Notes: To prevent damage to the device due to overshoot or oscillation issues, we recommend that current limits for all power supplies are set properly for each power supply before applying the voltage. The following are recommended current limits for each power supply:

Set 10 mA current limit to $V_{G1}$ and $V_{G2}$
Set 140 mA current limit to $V_D$

## Bias-up Procedure

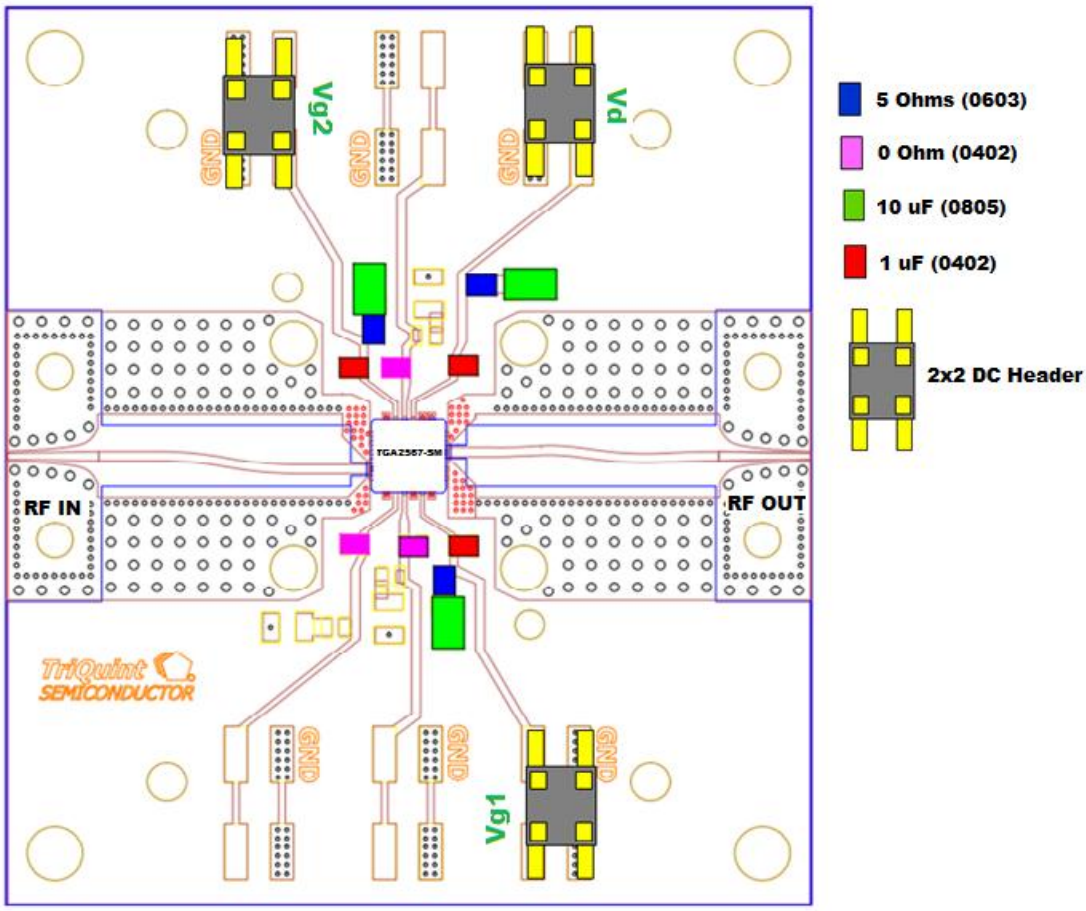
1. Apply -1.5 V to $V_{G1.}$
2. Apply +5 V to $V_{D.}$
3. Apply +1.3 V to $V_{G2}$.
4. Adjust $V_{G1}$ until $I_{DQ}$ = 100 mA ($V_{G1}$ ~ -0.7 V Typ.).
5. Turn On RF supply.
6. Adjust $V_{G2}$ to obtain desired gain

## Bias-down Procedure

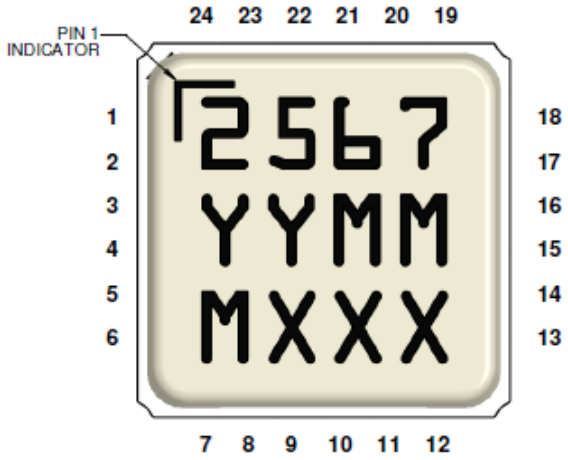
1. Reduce $V_{G2}$ to +1.3 V.
2. Turn off RF supply.
3. Reduce $V_{G1}$ to -1.5 V. Ensure $I_{DQ}$ ~ 0 mA
4. Set $V_{G2}$ to 0 V.
5. Set $V_D$ to 0 V.
6. Set $V_{G1}$ to 0 V.

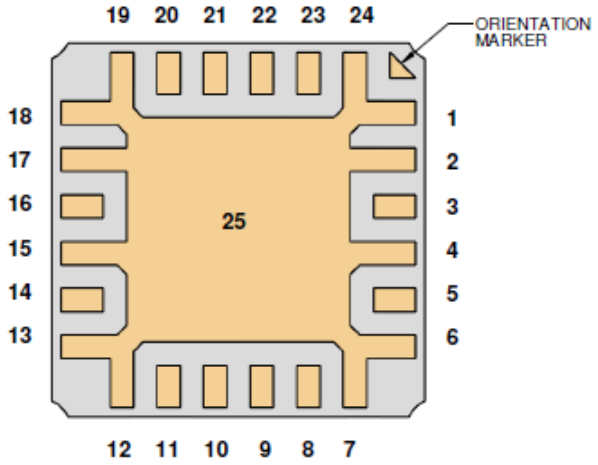
## Recommended Board Layout Assembly

Top dielectric material is ROGERS 4350, 0.010 inch thickness with 0.5 oz copper.



## Pin Layout




## Pin Description

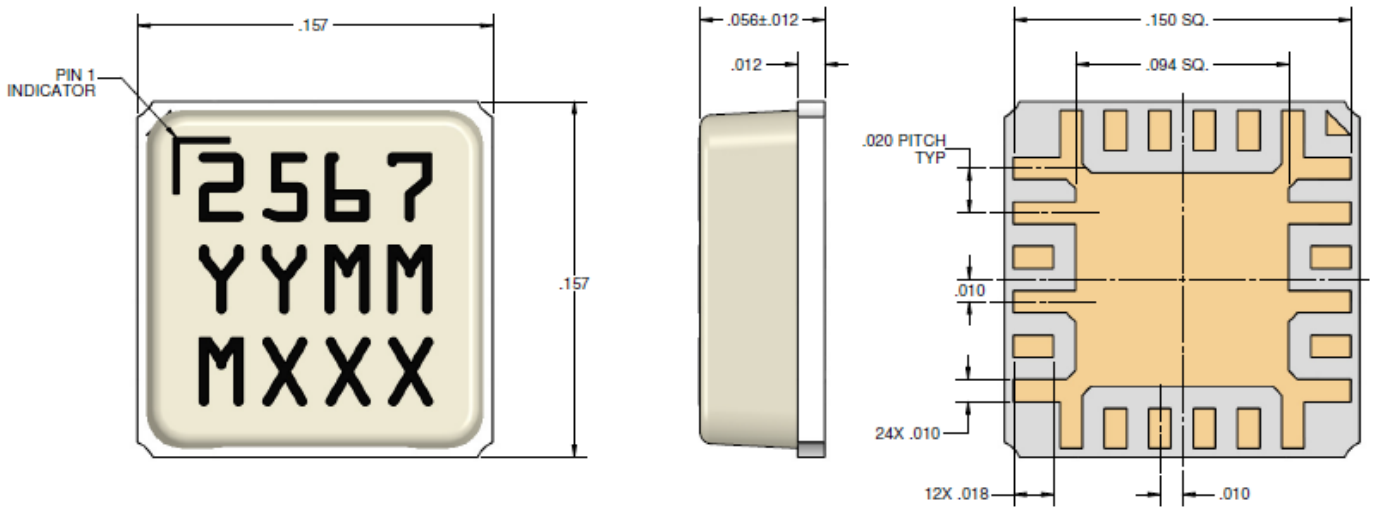
| Pin | Symbol | Description |
|---|---|---|
| 1,2,4,6,7,12,13,15,17-19,24, 25 | GND | Backside paddles; must be grounded on PCB. Multiple vias should be employed to minimize inductance and thermal resistance. (2) |
| 3,8-10,14,20,22 | N/C | No internal connection; must be grounded on PCB. |
| 5 | RF IN | RF input |
| 11 | $V_{G1}$ | Gate voltage. Bias network is required. (1) |
| 16 | RF OUT | RF output. |
| 21 | $V_D$ | Drain voltage. Bias network is required. (1) |
| 23 | $V_{G2}$ | Gate voltage. Bias network is required. (1) |

Notes:

1. See Application Circuit on page 6 as an example.
2. See Mounting Configuration on page 9 for suggested footprint.

## Mechanical Information

All dimensions are in inches. Unless specified otherwise, tolerances: ± 0.127 in.




Marking: Part number – 2567
Year/Month code – YYMM
Batch ID – MXXX

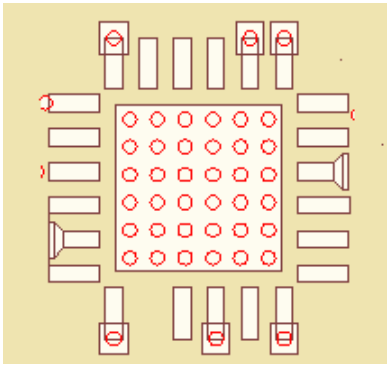
Package Materials:

| | |
|---|---|
| Base | Aluminum Nitride (AIN) |
| Lid | Liquid Crystal Polymer (LCP) |

Part is EPOXY Sealed

Land Pads are Gold Plated

## PCB Mounting Pattern



The pad pattern shown above has been developed and tested for optimized assembly at TriQuint. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

Ground / thermal vias are critical for the proper performance of this device. Vias should use a 0.008 in. diameter drill, and they are solid filled, copper plated shut.

## Product Compliance Information

### ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: TBD
Value: TBD
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

### MSL Rating

Level TBD at +260 °C convection reflow
The part is rated Moisture Sensitivity Level TBD at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

### ECCN

US Department of Commerce: EAR99

### Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°C

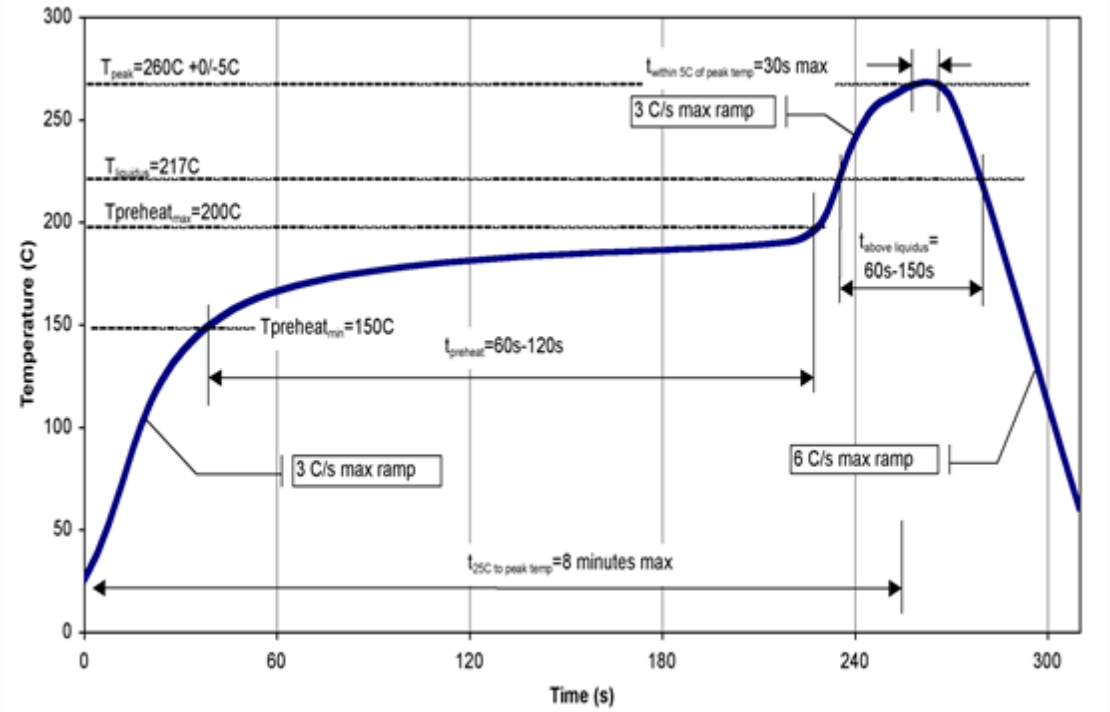
### RoHs Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

## Recommended Soldering Temperature Profile



## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

**Web:** www.triquint.com **Tel:** +1.972.994.8465
**Email:** info-sales@triquint.com **Fax:** +1.972.994.8504

For technical questions and application information: **Email:** info-products@triquint.com

## Important Notice

The information contained herein is believed to be reliable. TriQuint makes no warranties regarding the information contained herein. TriQuint assumes no responsibility or liability whatsoever for any of the information contained herein. TriQuint assumes no responsibility or liability whatsoever for the use of the information contained herein. The information contained herein is provided "AS IS, WHERE IS" and with all faults, and the entire risk associated with such information is entirely with the user. All information contained herein is subject to change without notice. Customers should obtain and verify the latest relevant information before placing orders for TriQuint products. The information contained herein or any use of such information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights, whether with regard to such information itself or anything described by such information.

TriQuint products are not warranted or authorized for use as critical components in medical, life-saving, or life-sustaining applications, or other applications where a failure would reasonably be expected to cause severe personal injury or death.