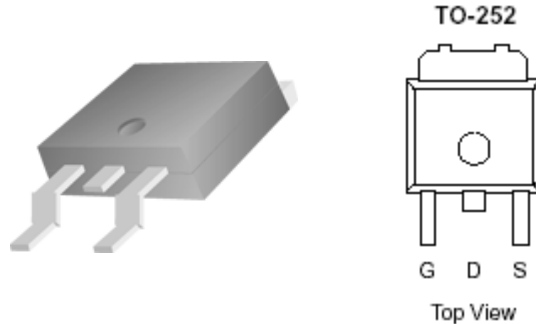


P-Channel 40-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe DPAK saves board space
- Fast switching speed
- High performance trench technology



PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
-40	69 @ $V_{GS} = -10V$	22
	106 @ $V_{GS} = -4.5V$	18

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^a	$T_A=25^\circ C$ I_D	22	A
Pulsed Drain Current ^b	I_{DM}	± 72	
Continuous Source Current (Diode Conduction) ^a	I_S	-30	A
Power Dissipation ^a	$T_A=25^\circ C$ P_D	50	W
Operating Junction and Storage Temperature Range	T_j, T_{stg}	-55 to 175	$^\circ C$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Maximum	Units
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	50	$^\circ C/W$
Maximum Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ C/W$

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T _A = 25°C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 uA	-1			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±25 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24 V, V _{GS} = 0 V			-1	uA
		V _{DS} = -24 V, V _{GS} = 0 V, T _J = 55°C			-5	
On-State Drain Current ^A	I _{D(on)}	V _{DS} = -5 V, V _{GS} = -10 V	-41			A
Drain-Source On-Resistance ^A	r _{DS(on)}	V _{GS} = -10 V, I _D = -22 A			69	mΩ
		V _{GS} = -4.5 V, I _D = -18 A			106	
Forward Transconductance ^A	g _{fs}	V _{DS} = -15 V, I _D = -22 A		31		S
Diode Forward Voltage	V _{SD}	I _S = -41 A, V _{GS} = 0 V		-0.7		V
Dynamic^b						
Total Gate Charge	Q _g	V _{DS} = -15 V, V _{GS} = -4.5 V, I _D = -22 A		10		nC
Gate-Source Charge	Q _{gs}			2.2		
Gate-Drain Charge	Q _{gd}			2.5		
Switching						
Turn-On Delay Time	t _{d(on)}	V _{DD} = -15 V, R _L = 15 Ω , I _D = -24 A, V _{GEN} = -10 V, R _G = 6Ω		10		nS
Rise Time	t _r			2.8		
Turn-Off Delay Time	t _{d(off)}			53.6		
Fall-Time	t _f			46		

Notes

- a. Pulse test: PW ≤ 300us duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

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Typical Electrical Characteristics

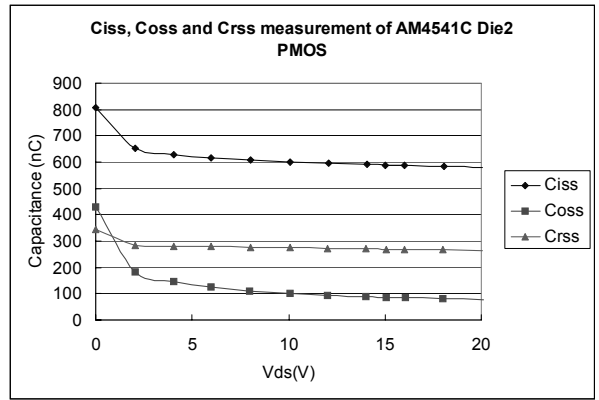
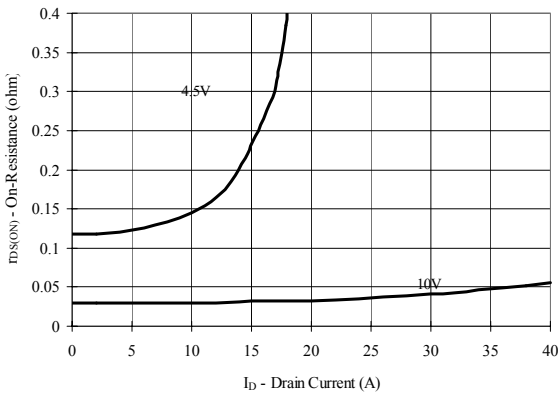
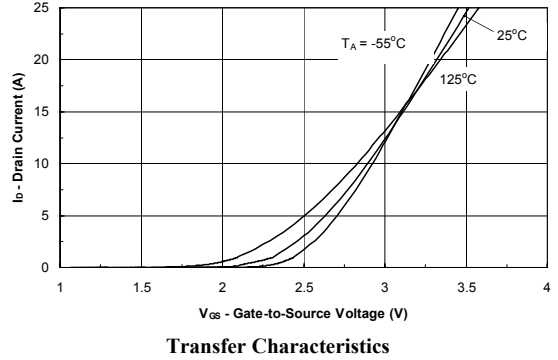
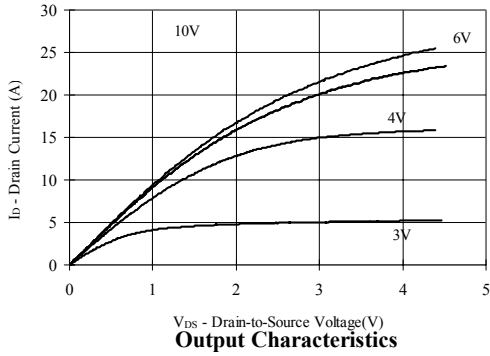
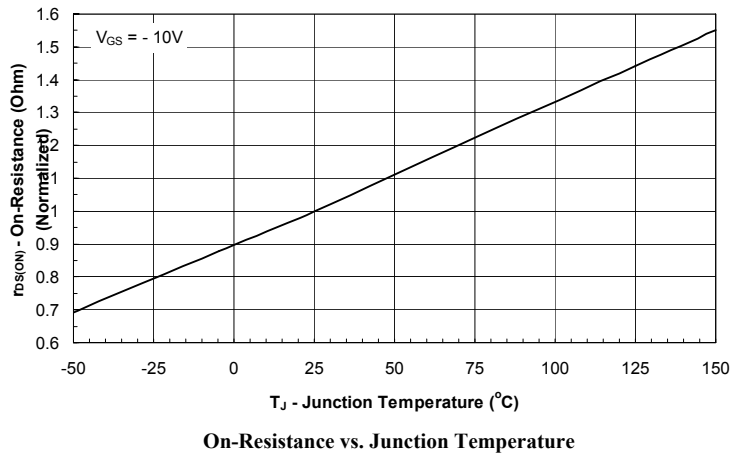
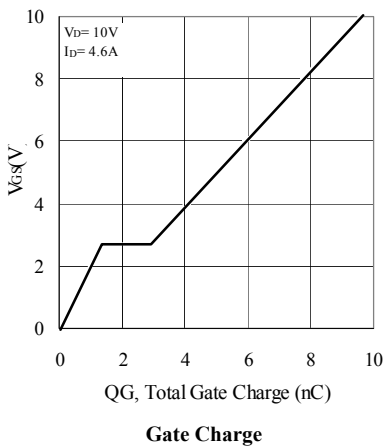
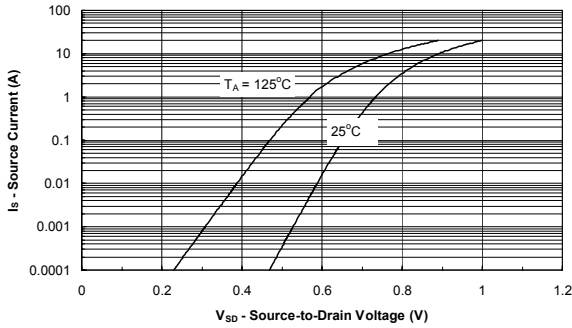


Figure 3. On Resistance Vs Vgs Voltage



Typical Electrical Characteristics



Source-Drain Diode Forward Voltage

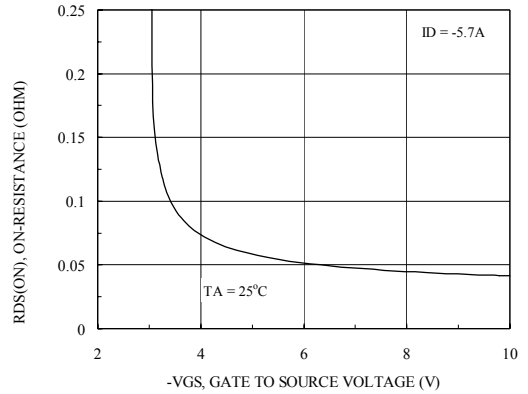
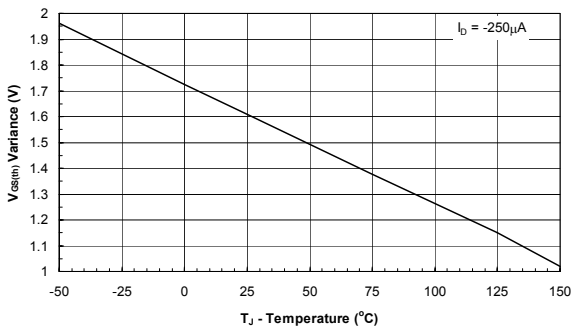


Figure 8. On-Resistance with Gate to Source Voltage



Threshold Voltage

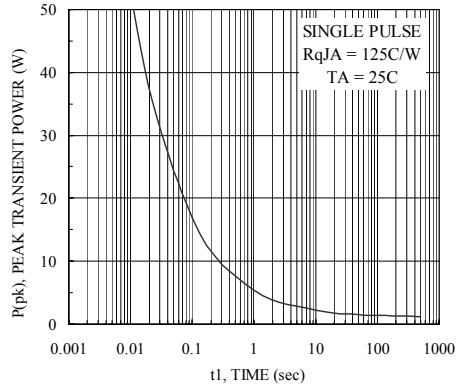


Figure 10. Single Pulse Maximum Power Dissipation

Normalized Thermal Transient Junction to Ambient

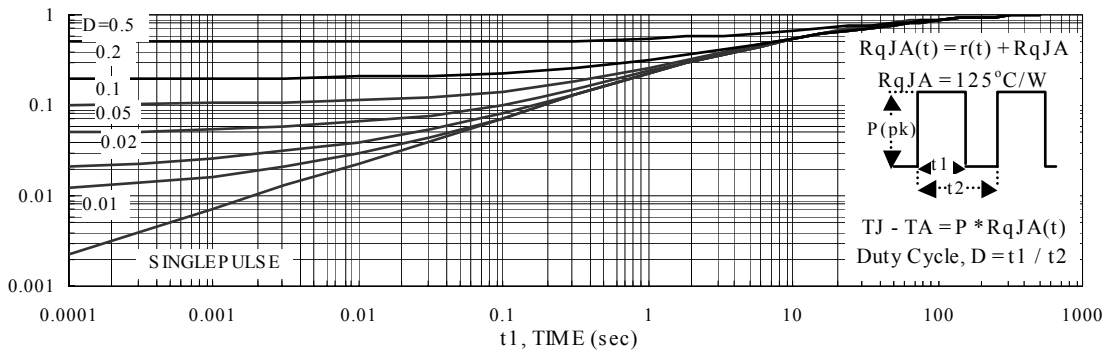
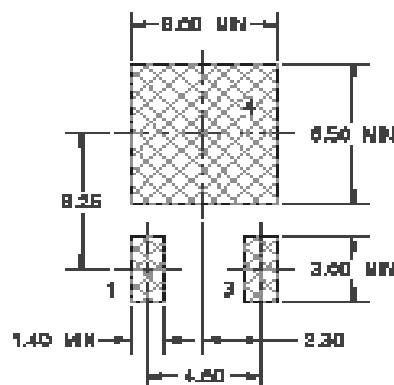
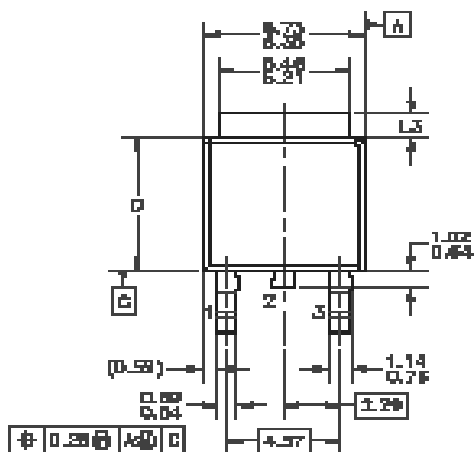
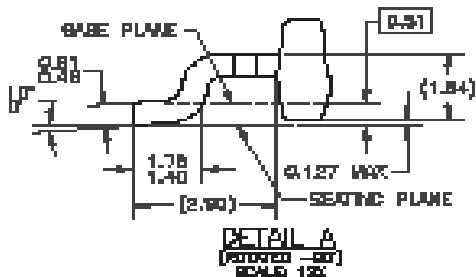
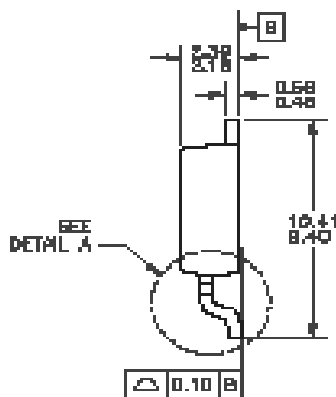
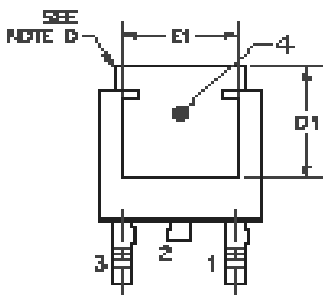


Figure 11. Transient Thermal Response Curve

Package Information



LAND PATTERN RECOMMENDATION



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) THIS PACKAGE CONFORMS TO JEDEC, TO-262, ISSUE C, VARIATION AA IN REF, DATED NOV. 1989.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.00M-1994.
 - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
 - E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION A1	OPTION A2
L3	0.68-1.27	1.62-2.52
D	0.97-0.99	0.93-0.99
E1	4.32 MIN	3.81 MIN
D1	3.81 MIN	4.37 MIN