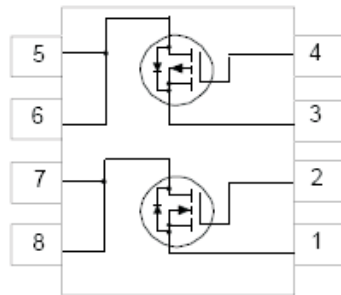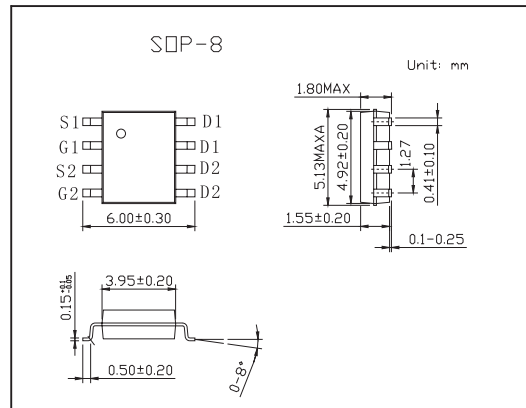# KDS9952A

■ Features

● N-Channel 3.7A, 30V, $R_{DS(ON)}$=0.08W @ V_{GS}=10V.

   P-Channel -2.9A, -30V, $R_{DS(ON)}$=0.13W @ V_{GS}=-10V.

● High density cell design or extremely low $R_{DS(ON)}$.

● High power and current handling capability in a widely used

● surface mount package.

   Dual (N & P-Channel) MOSFET in surface mount package.

SOP-8
Unit: mm

■ Absolute Maximum Ratings Ta = 25℃

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain to Source Voltage		V_{DSS}	30	-30	V
Gate to Source Voltage		V_{GS}	±20	±20	V
Drain Current Continuous	(Note 1a)	I_D	±3.7	±2.9	A
Drain Current Pulsed			±15	±10	A
Power Dissipation for Dual Operation		P_D	2		W
Power Dissipation for Single Operation	(Note 1a)	P_D	1.6		
	(Note 1b)		1		
	(Note 1c)		0.9		
Operating and Storage Temperature		T_J, T_{STG}	-55 to 150		℃
Thermal Resistance Junction to Case	(Note 1)	$R_{\theta JC}$	40		℃/W
Thermal Resistance Junction to Ambient	(Note 1a)	$R_{\theta JA}$	78		℃/W

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KDS9952A

■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Testconditons	Type	Min	Typ	Max	Unit
Drain□Source Breakdown Voltage	B$_{VDSS}$	V$_{GS}$ = 0 V, I$_D$ = 250 μA	N-Ch	30			V
		V$_{GS}$ = 0 V, I$_D$ = -250 μA	P-Ch	-30			
Zero Gate Voltage Drain Current	I$_{DSS}$	V$_{DS}$ = 24 V, V$_{GS}$ = 0 V	N-Ch			2	μA
		V$_{DS}$ = 24 V, V$_{GS}$ = 0 V,T$_J$ = 55℃				25	
		V$_{DS}$ = -24 V, V$_{GS}$ = 0 V	P-Ch			-2	
		V$_{DS}$ = -24 V, V$_{GS}$ = 0 V,T$_J$ = 55℃				-25	
Gate-Body Leakage, Forward	I$_{GSSF}$	V$_{GS}$ = 20 V, V$_{DS}$ = 0 V	ALL			100	nA
Gate-Body Leakage, Reverse	I$_{GSSR}$	V$_{GS}$ = -20 V, V$_{DS}$ = 0 V	ALL			-100	nA
Gate Threshold Voltage	V$_{GS(th)}$	V$_{DS}$ = V$_{GS}$, I$_D$ = 250 μA	N-Ch	1	1.7	2.8	V
		V$_{DS}$ = V$_{GS}$, I$_D$ = 250 μA,T$_J$ = 125℃		0.7	1.2	2.2	
		V$_{DS}$ = V$_{GS}$, I$_D$ = -250 μA	P-Ch	-1	-1.6	-2.8	
		V$_{DS}$ = V$_{GS}$, I$_D$ = -250 μA,T$_J$ = 125℃		-0.85	-1.25	-2.5	
Static Drain-Source On-Resistance	R$_{DS(on)}$	V$_{GS}$ = 10 V, I$_D$ = 1.0 A	N-Ch		0.06	0.08	Ω
		V$_{GS}$ = 10 V, I$_D$ = 1.0 A,T$_J$ = 125℃			0.08	0.13	
		V$_{GS}$ = 4.5 V, I$_D$ = 0.5 A			0.08	0.11	
		V$_{GS}$ = 4.5 V, I$_D$ = 0.5 A,T$_J$ = 125℃			0.11	0.18	
		V$_{GS}$ =-10 V, I$_D$ =-1.0 A	P-Ch		0.11	0.13	
		V$_{GS}$ =-10 V, I$_D$ =-1.0 A,T$_J$ = 125℃			0.15	0.21	
		V$_{GS}$ = -4.5 V, I$_D$ =- 0.5 A			0.17	0.2	
		V$_{GS}$ = -4.5 V, I$_D$ =- 0.5 A,T$_J$ = 125℃			0.24	0.32	
On□State Drain Current	I$_{D(on)}$	V$_{GS}$ = 10 V, V$_{DS}$ = 5 V	N-Ch	15			A
		V$_{GS}$ = -10 V, V$_{DS}$ = -5 V	P-Ch	-10			
Forward Transconductance	g$_{FS}$	V$_{DS}$ = 15 V, I$_D$ = 3.7 A	N-Ch		6		S
		V$_{DS}$ = -15 V, I$_D$ = -2.9 A	P-Ch		4		
Input Capacitance	C$_{iss}$	N-Channel	N-Ch		320		pF
		V$_{DS}$ = 10 V, V$_{GS}$ = 0 V,f = 1.0 MHz	P-Ch		350		
Output Capacitance	C$_{oss}$		N-Ch		225		pF
		P-Channel	P-Ch		260		
Reverse Transfer Capacitance	C$_{rss}$	V$_{DS}$ = -10 V, V$_{GS}$ = 0 V,f = 1.0 MHz	N-Ch		85		pF
			P-Ch		100		
Turn-On Delay Time	t$_{d(on)}$	N-Channel	N-Ch		10	15	ns
		V$_{DD}$ = 10 V, I$_D$ = 1 A	P-Ch		9	40	
Turn-On Rise Time	tr	V$_{GS}$ = 10 V, R$_{GEN}$ = 6 Ω (Note 2)	N-Ch		13	20	ns
			P-Ch		21	40	
Turn-Off Delay Time	t$_{d(off)}$	P-Channel	N-Ch		21	50	ns
		V$_{DD}$ = -10 V, I$_D$ = -1 A	P-Ch		21	90	
Turn-Off Fall Time	tf	V$_{GS}$ = -10 V, R$_{GEN}$ = 6 Ω (Note 2)	N-Ch		5	50	ns
			P-Ch		8	50	
Total Gate Charge	Q$_g$	N-Channel	N-Ch		9.5	27	nC
		V$_{DS}$ = 10 V, I$_D$ = 3.7 A,V$_{GS}$ = 10 V	P-Ch		10	25	
Gate□Source Charge	Q$_{gs}$		N-Ch		1.5		nC
		P-Channel	P-Ch		1.6		
Gate□Drain Charge	Q$_{gd}$	V$_{DS}$ = -10 V, I$_D$ = -2.9 A,V$_{GS}$ = -10 V	N-Ch		3.3		nC
			P-Ch		3.4		

KDS9952A

■ Electrical Characteristics Ta = 25℃

| Parameter	Symbol	Testconditons	Type	Min	Typ	Max	Unit
Maximum Continuous Drain-Source Diode Forward Current	Is		N-Ch			1.2	A
			P-Ch			-1.2	
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS} = 0 V, Is = 1.25 A (Note 2)	N-Ch		0.8	1.3	V
		V_{GS} = 0 V, Is =-1.25 A (Note 2)	P-Ch		-0.8	-1.3	
Reverse Recovery Time	trr	V_{GS}=0 V, I_F=1.25 A,dI_F/dt=100A/μ s	N-Ch			75	ns
		V_{GS}=0 V, I_F=-1.25 A,dI_F/dt=100A/μ s	P-Ch			100	

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed design while $R_{\theta CA}$ is determined by the user's board design.
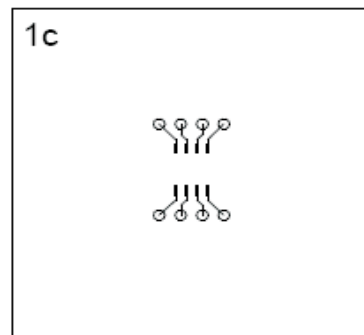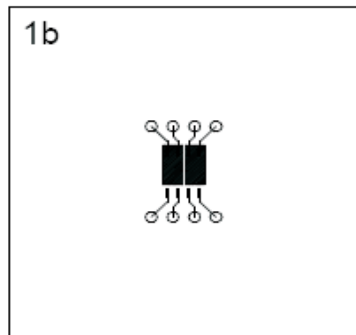
$$P_D(t) = \frac{T_J - T_A}{R_{\theta J A(t)}} = \frac{T_J - T_A}{R_{\theta J C} + R_{\theta CA(t)}} = I_D^2(t) \times R_{DS(ON)} @T_J$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

   a. 78°C/W when mounted on a 0.5 in² pad of 2oz opper.

   b. 125°C/W when mounted on a 0.02 in² pad of 2oz opper.

   c. 135°C/W when mounted on a 0.003 in² pad of 2oz opper.
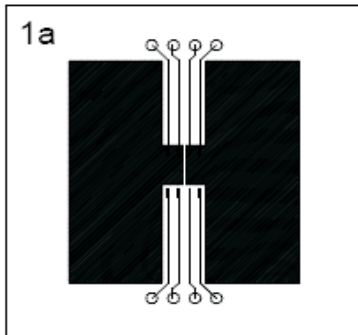
Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.