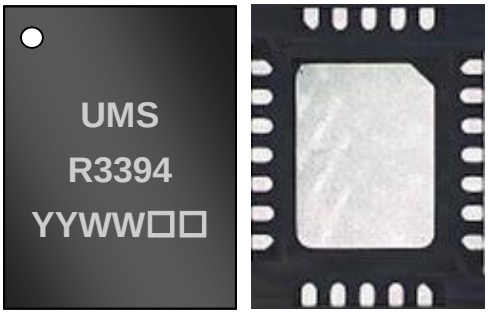
37-40GHz Integrated Down Converter

GaAs Monolithic Microwave IC in SMD leadless package

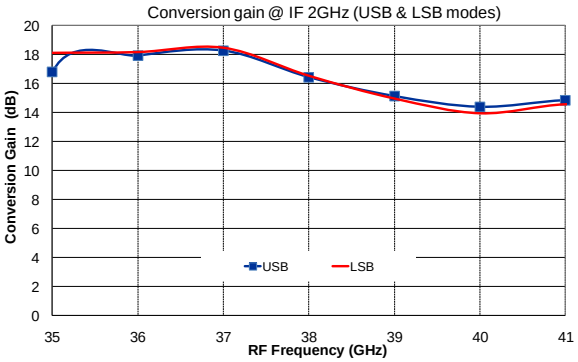
Description

The CHR3394-QEG is a multifunction monolithic receiver, which integrates a balanced cold FET mixer, a LO chain with buffers associated to a time two multiplier, and a RF low noise amplifier.
It is designed for a wide range of applications, from military to commercial communication systems.
The circuit is manufactured with a pHEMT process, 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is supplied in RoHS compliant SMD package.



Main Features

- Broadband performances: 37-40GHz
- 13dB Conversion gain
- 15dBc Image Rejection
- 1dBm IIP3
- 3.5dB Noise Figure for IF>0.1GHz
- 0dBm LO input Power
- DC bias: Vd=4V @ Id=250mA
- 24L-QFN4x5
- MSL1



Main Characteristics

Tamb.= +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	37		40	GHz
F_{LO}	LO frequency range	17.5		21.0	GHz
F_{IF}	IF frequency range	DC		3.5	GHz
G	Conversion gain		13		dB

United Monolithic Semiconductors S.A.S.
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Main Characteristics

Tamb.= +25°C, VD = VD1 = +4V [1]

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	37		40	GHz
F_{LO}	LO frequency range	17.5		21.0	GHz
F_{IF}	IF frequency range	DC		3.5	GHz
G	Conversion gain [2]		13		dB
NF	Noise Figure for IF>0.1GHz		3.5		dB
Im_rej	Image rejection [2]		15		dBc
P_{LO}	LO Input power		0		dBm
IIP3	Input IP3		1		dBm
LO RL	LO return loss		-12		dB
RF RL	RF return loss		-6		dB
VGL	LNA DC gate voltage		-0.1		V
VGX	Multiplier DC gate voltage		-0.9		V
IDt	Total Drain current (ID+ID1) [3]		250		mA

These values are representative of on-board measurements.

[1] VD: LO-chain drain bias voltage. VD1: LNA drain bias voltage.

[2] An external combiner 90° is required on I/Q.

[3] ID: LO-chain drain current, typically 125mA.
[3] ID1: LNA drain current, typically 125mA, should be tuned with VGL.

Electrostatic discharge sensitive device observe handling precautions!

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Absolute Maximum Ratings (1)

Tamb.= +25°C

Symbol	Parameter	Values	Unit
VD, VD1	Drain bias voltages	4.5V	V
IDt	Drain bias current	340	mA
VGL, VGX	Gate bias voltages	-2 to +0.4	V
P_RF	Maximum peak input power overdrive (2)	+15	dBm
P_LO	Maximum LO input power	+15	dBm
Tj	Junction temperature	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +155	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s.

Typical Bias Conditions

Tamb.= +25°C

Symbol	Pad N°	Parameter	Values	Unit
VD1, VD	10, 11	DC drain voltages (LNA and LO-chain)	4	V
ID1	10	LNA drain current controlled with VGL	125	mA
VGL	9	LNA DC gate voltage	-0.1	V
VGX	12	Multiplier DC gate voltage	-0.9	V

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Device thermal performances

All the figures given in this section are obtained assuming that the QFN device is cooled down only by conduction through the package thermal pad (no convection mode considered). The temperature is monitored at the package back-side interface (Tcase) as shown below. The system maximum temperature must be adjusted in order to guarantee that Tcase remains below than the maximum value specified in the next table. So, the system PCB must be designed to comply with this requirement.

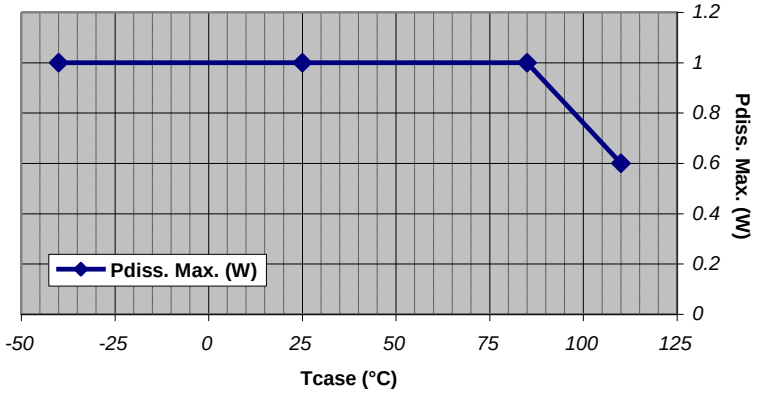
A derating must be applied on the dissipated power if the Tcase temperature can not be maintained below than the maximum temperature specified (see the curve Pdiss. Max) in order to guarantee the nominal device life time (MTTF).

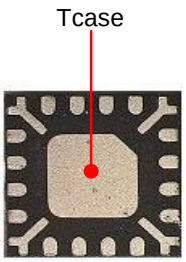
DEVICE THERMAL SPECIFICATION : CHR3394-QEG				
Recommended max. junction temperature (Tj max)			:	147 °C
Junction temperature absolute maximum rating			:	175 °C
Max. continuous dissipated power @ Tcase=	85	°C	:	1 W
=> Pdiss derating above Tcase(1)=	85	°C	:	16 mW/°C
Junction-Case thermal resistance (Rth J-C)(2)			:	<62 °C/W
Min. package back side operating temperature(3)			:	-40 °C
Max. package back side operating temperature(3)			:	85 °C
Min. storage temperature			:	-55 °C
Max. storage temperature			:	155 °C

(1) Derating at junction temperature constant = Tj max

*(2) Rth J-C is calculated for a worst case where the **hotter junction** of the MMIC is considered.*

(3) Tcase=Package back side temperature measured under the die-attach-pad (see the drawing below).





Example of QFN 16L 3x3 back-side view, temperature reference point (Tcase) location.

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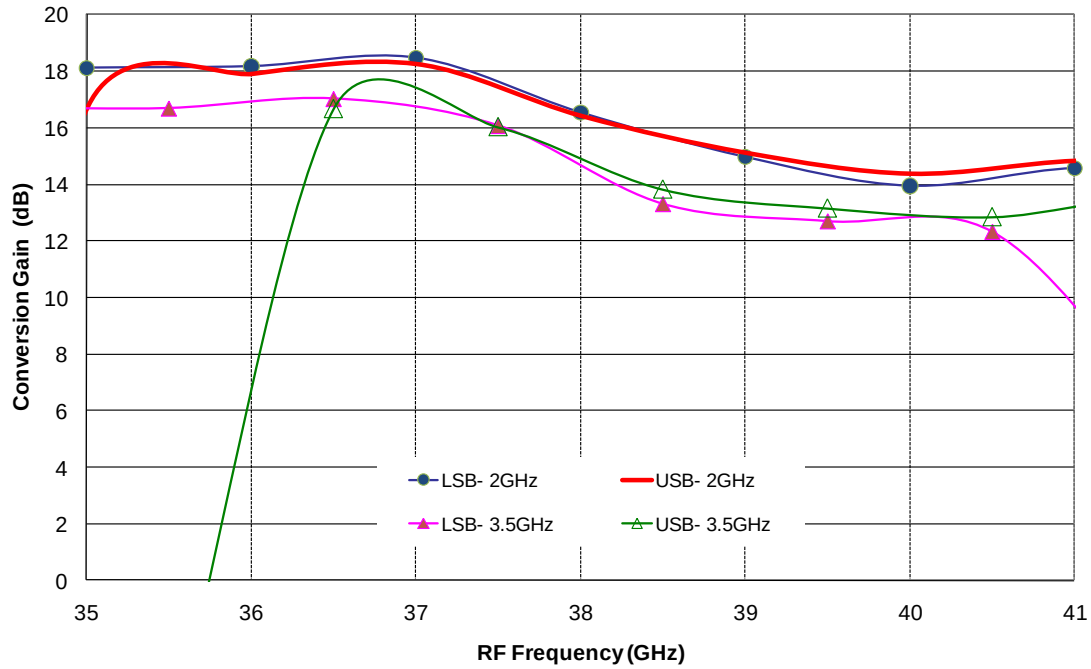
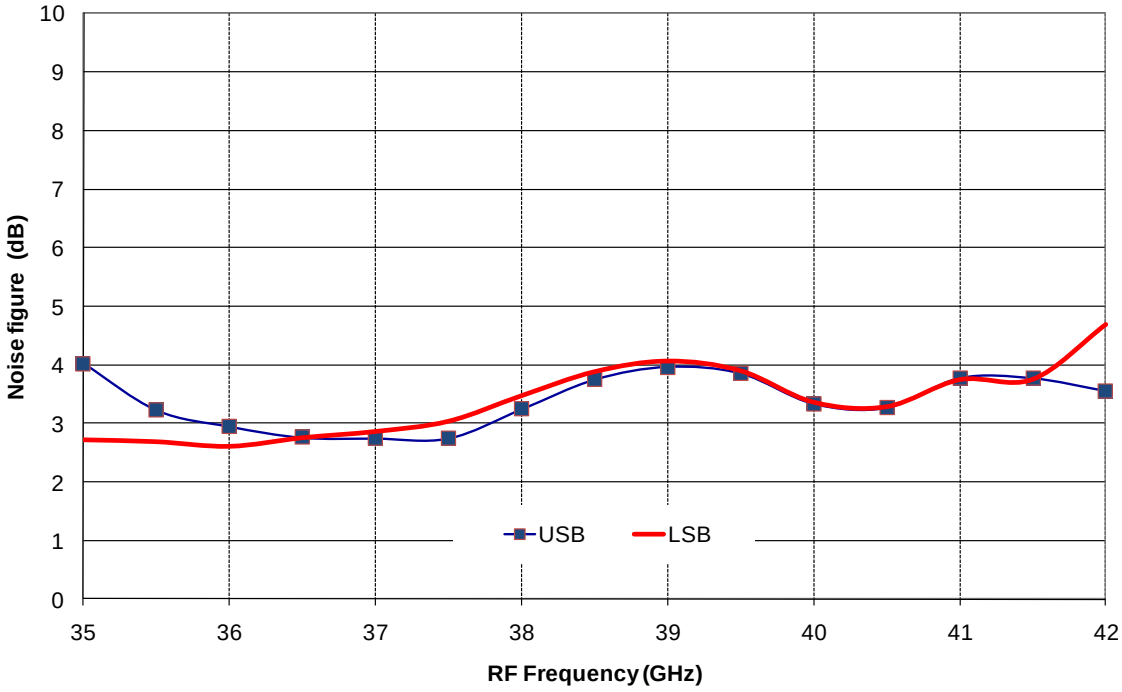
Typical Board Measurements

Tamb.= +25°C, VD = VD1 =+4V, VGL = -0.1V, VGX = -0.9V, P_LO = 0dBm (IDt = 250mA)
These values are representative of onboard measurements as defined on the drawing in paragraph "Evaluation mother board". Data given in the package access planes.

Conversion Gain versus RF & IF frequency (USB & LSB modes)



Noise figure versus RF frequency at IF 3GHz



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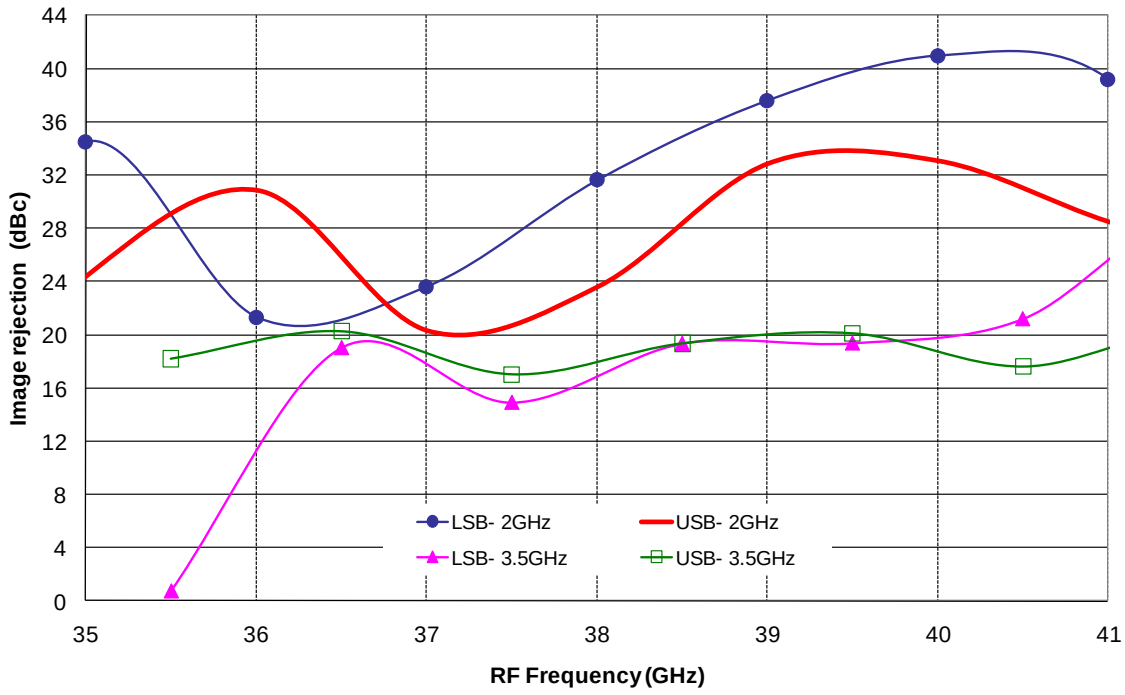
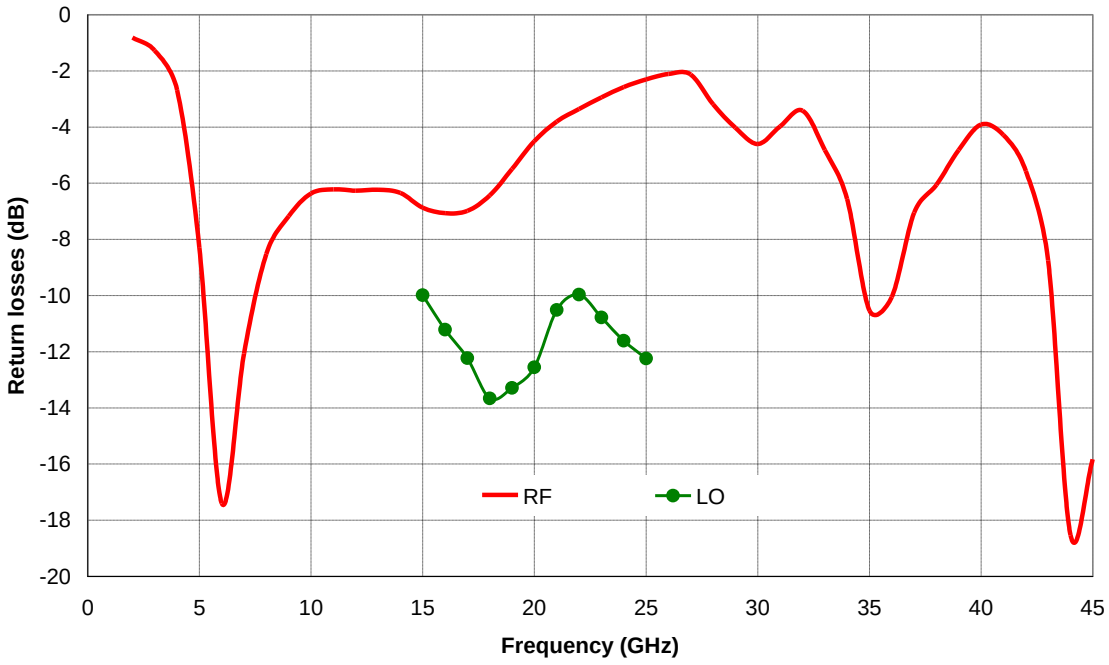
Typical Board Measurements

Tamb.= +25°C, VD = VD1 = +4V, VGL = -0.1V, VGX = -0.9V, P_LO = 0dBm (IDt = 250mA)

Image rejection versus RF & IF frequency



Return Losses (LO & RF) versus frequency



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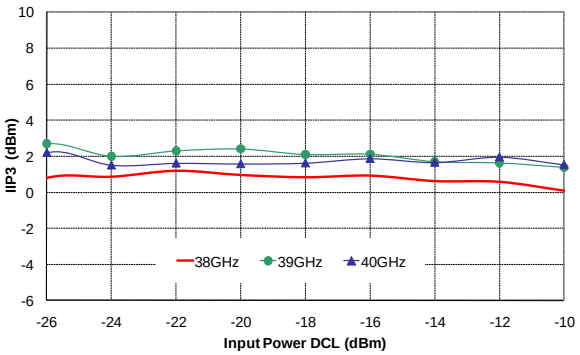
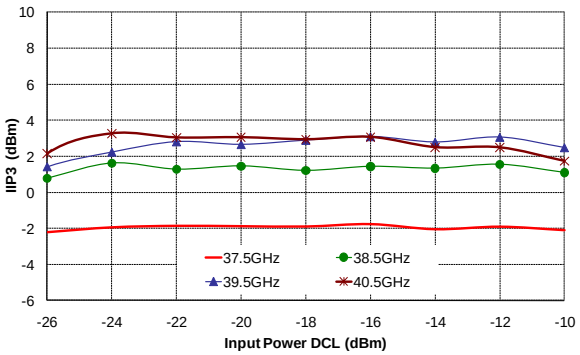
Typical Board Measurements

Tamb.= +25°C, VD = VD1 = +4V, VGL = -0.1V, VGX = -0.9V, P_LO = 0dBm (IDt = 250mA)

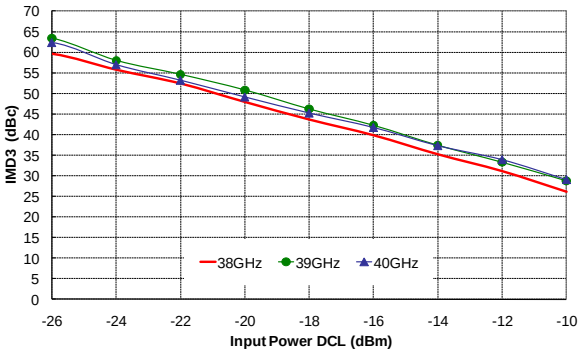
Input IP3 vs RF frequency at IF 2GHz



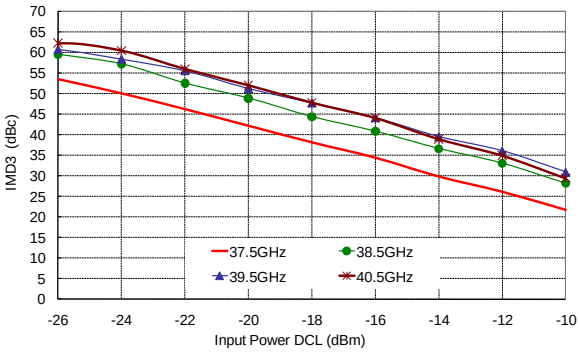
Input IP3 vs RF frequency at IF 3.5GHz



IMD3 vs RF frequency at IF 2GHz



IMD3 vs RF frequency at IF 3.5GHz



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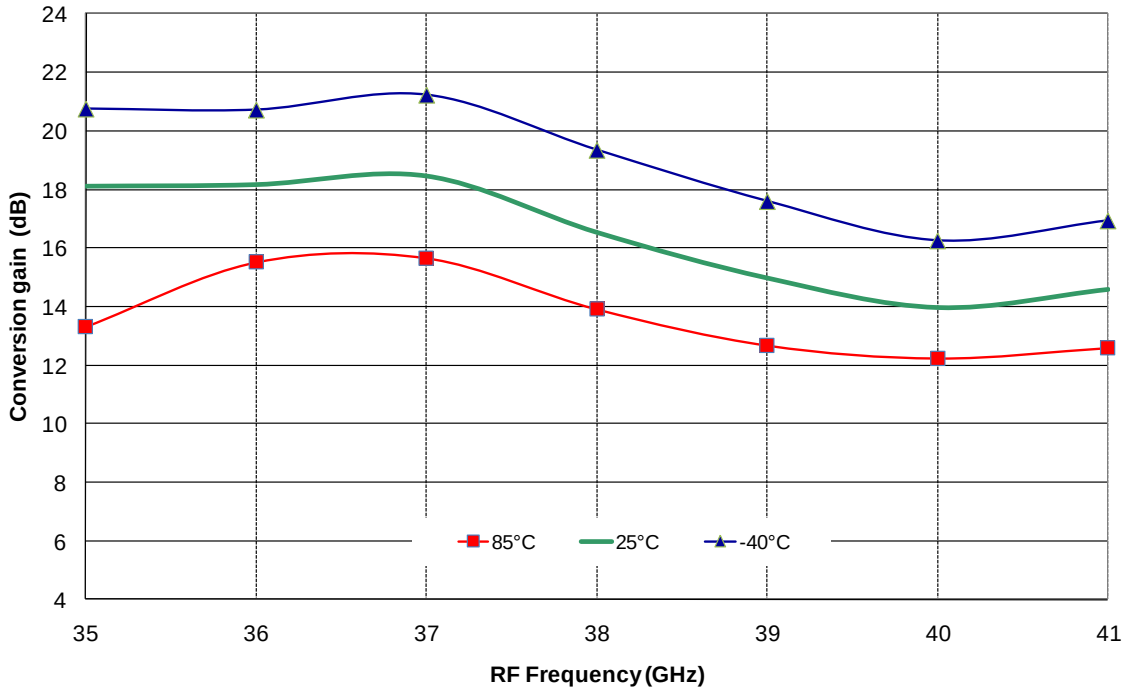
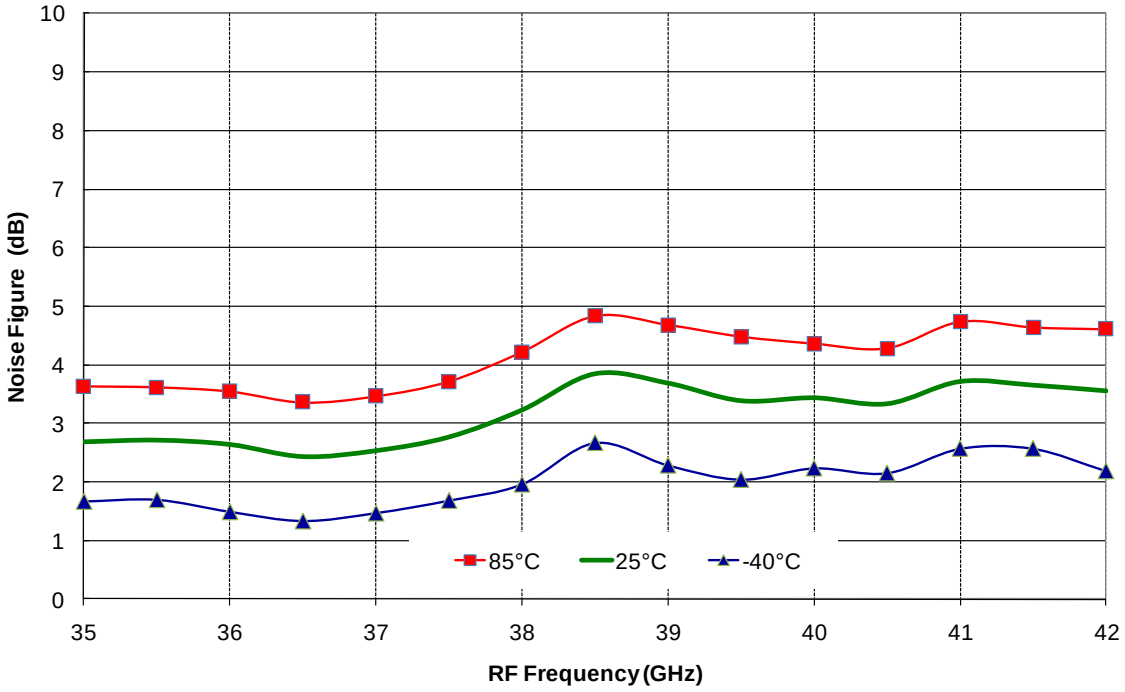
Typical Board Measurements

Tamb = +25°C, Tcold = -40°C, Thot = +85°C
VD = VD1 = +4V, VGL = -0.1V, VGX = -0.9V, P_LO = 0dBm

Conversion Gain versus temperature at IF 2 GHz (USB mode)



Noise figure versus temperature at IF 2GHz (USB mode)



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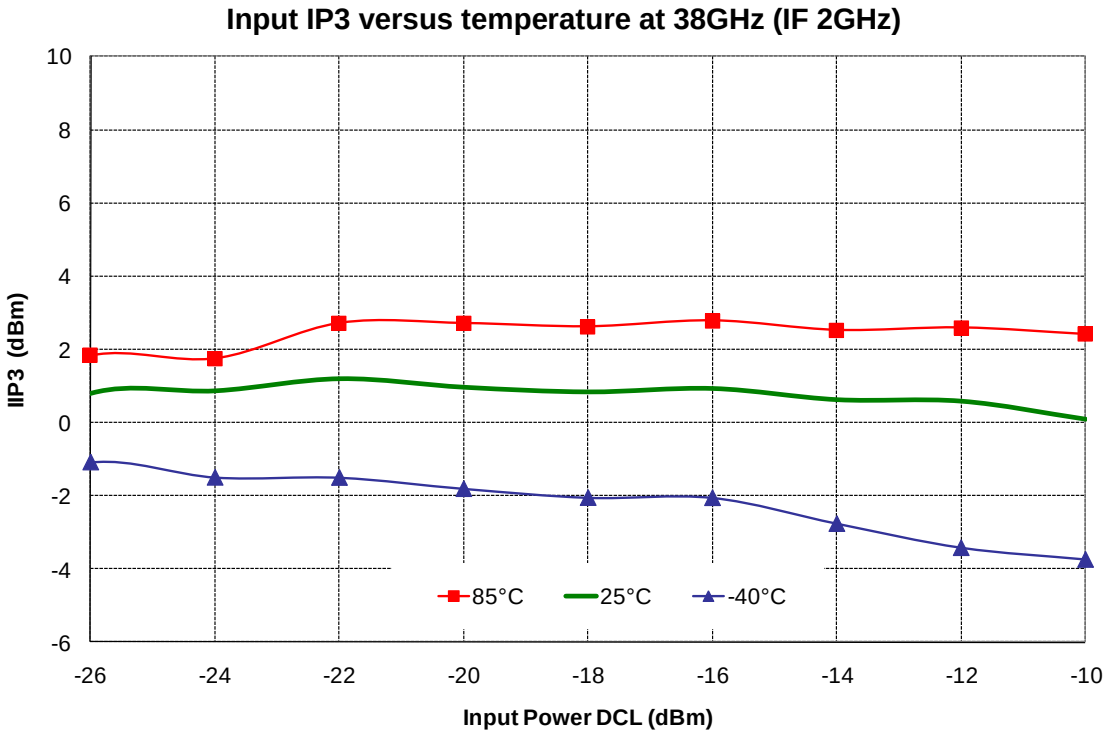
Typical Board Measurements

Tamb = +25°C, Tcold = -40°C, Thot = +85°C
VD = VD1 = +4V, VGL = -0.1V, VGX = -0.9V, P_LO = 0dBm



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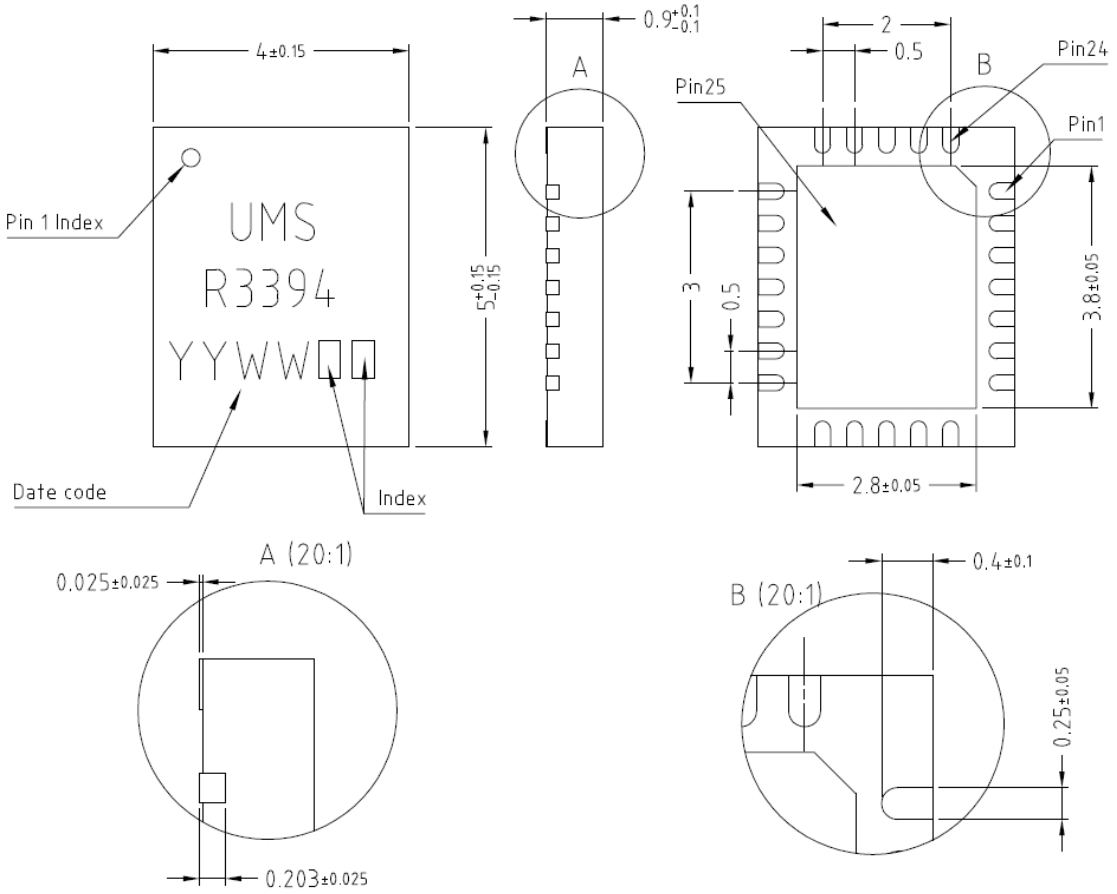
Package outline (1)



Matt tin, Lead Free	(Green)	1-	Nc	9-	VGL	17-	Gnd(2)
Units :	mm	2-	Nc	10-	VD1	18-	Nc
From the standard :	JEDEC MO-220	3-	Nc	11-	VD	19-	Nc
	(VGGD)	4-	Gnd(2)	12-	VGX	20-	IF_I
25-	GND	5-	RF in	13-	Nc	21-	Gnd(2)
		6-	Gnd(2)	14-	Nc	22-	IF_Q
		7-	Nc	15-	Gnd(2)	23-	Nc
		8-	Nc	16-	LO in	24-	Nc

(1) The package outline drawing included to this data-sheet is given for indication. Refer to the application note AN0017 (http://www.ums-gaas.com) for exact package dimensions.

(2) It is strongly recommended to ground all pins marked “Gnd” through the PCB board. Ensure that the PCB board is designed to provide the best possible ground to the package.

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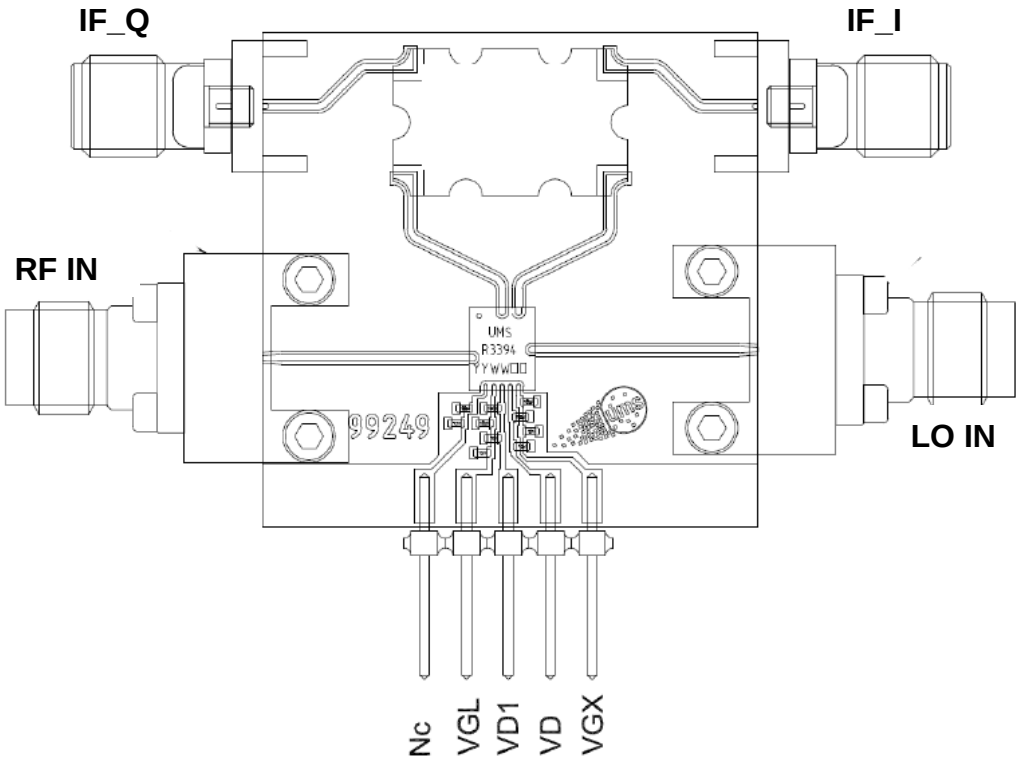
Evaluation mother board

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a micro-strip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- See application note AN0017 for details.
- Hybrid coupler 90° for 2-4GHz.



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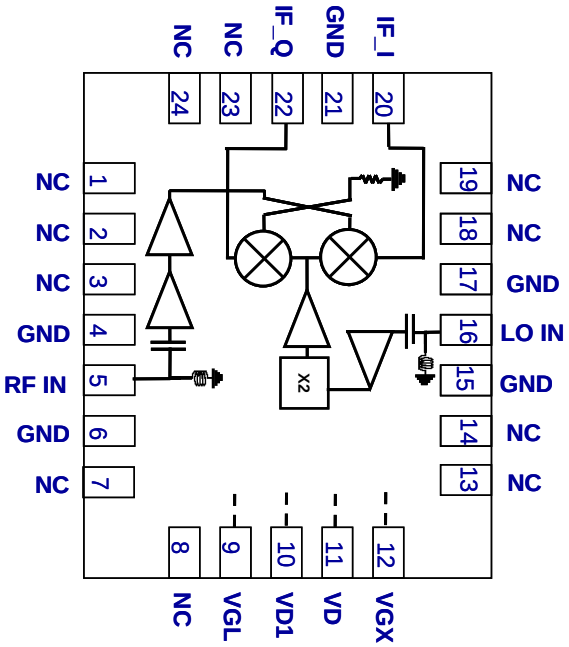
Notes

Due to ESD protection circuits on RF and LO inputs, an external capacitance might be requested to isolate the product from external voltage that could be present on these accesses.



ESD protections are also implemented on gate access.
The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (10nF) on the PC board, as close as possible to the package.

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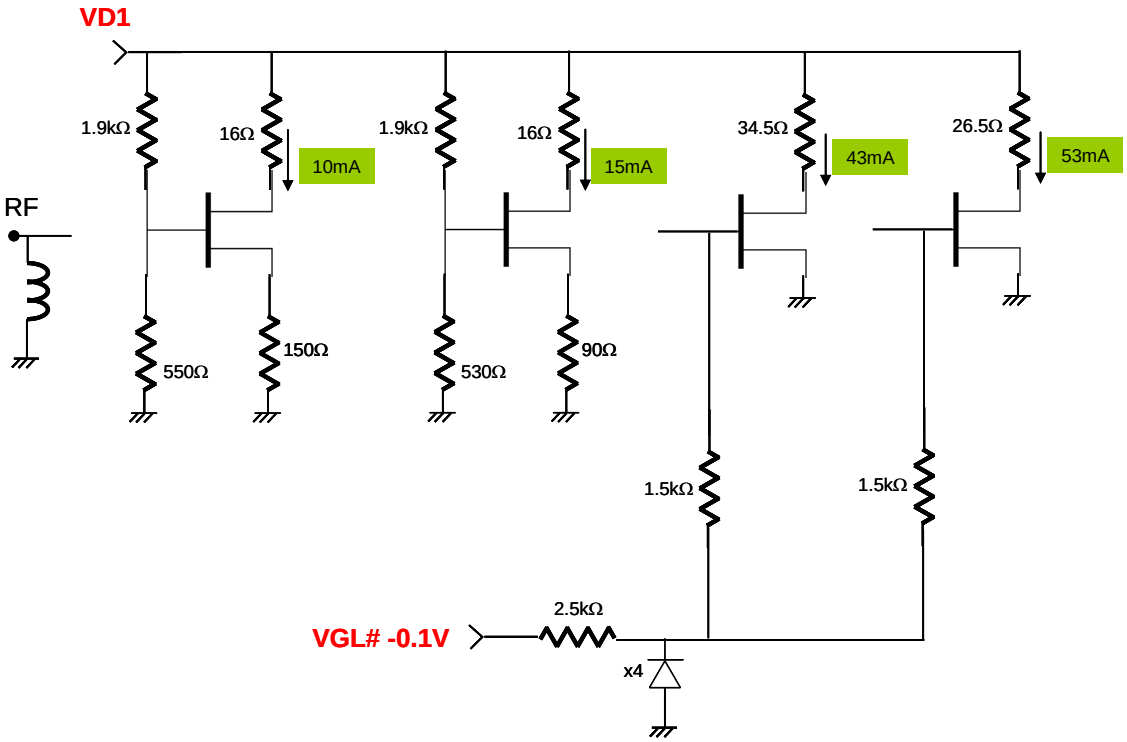
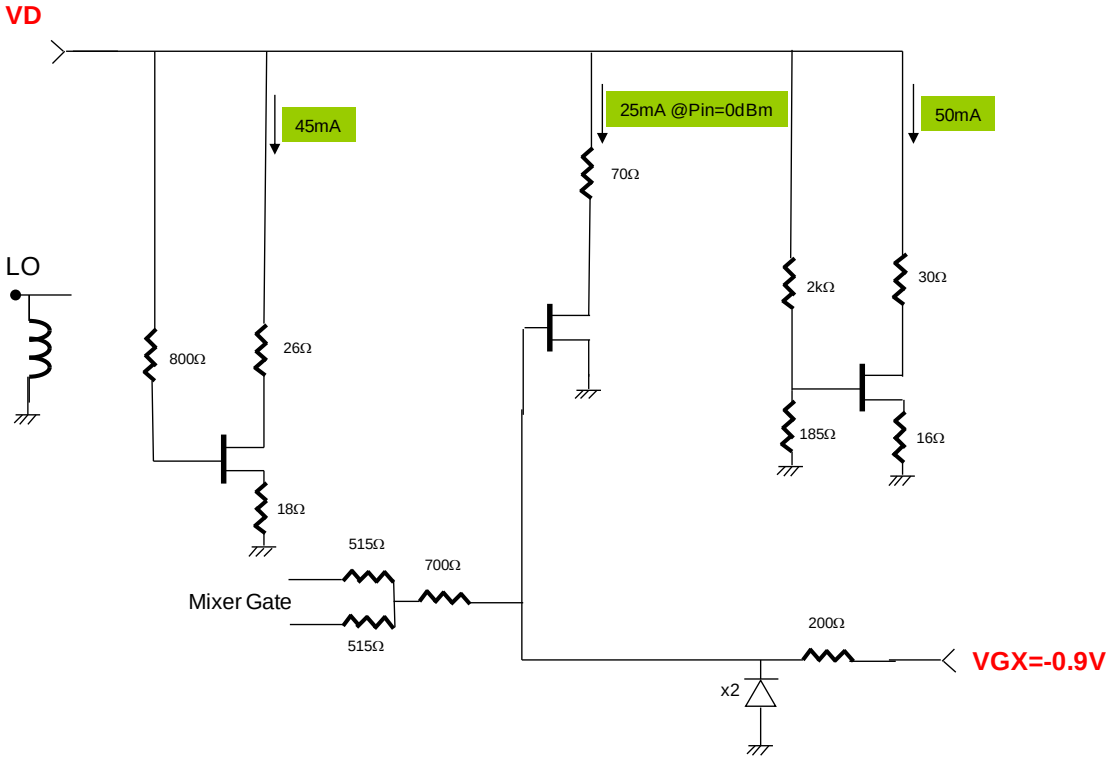
DC Schematic

LNA: 4V, 125mA



LO chain: 4V, 125mA



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Recommended package footprint

Refer to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommendations.

SMD mounting procedure

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Recommended environmental management

Refer to the application note AN0019 available at http://www.ums-gaas.com for environmental data on UMS package products.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

Ordering Information

QFN 4x5 RoHS compliant package:	CHR3394-QEG/XY	
	Stick: XY = 20	Tape & reel: XY = 21

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