THA1008

Thesys

THA1008 High Density Array Series

Description

The THA1008 High Density Array is an HCMOS metal programmable array product targeted at high performance, low cost and high complexity applications. The THA1008 series is based on 0.8 micron 2 layer metal HCMOS technology. 22 masterslices with raw gate counts of between 440 and 573,240 are available. The THA1008 proprietary cell architecture offers a gate delay of 325 picoseconds; the higher density also results in higher chip level performance due to lower parasitic and fanout loadings.

The THA1008 is designed for cost sensitive applications which also demand high circuit performance. The series eliminates the necessity of fighting the time-to-market versus production cost decision, because the THA1008 design philosophy addresses both of these issues.

The THA1008 design kits support most popular design platforms and environments, and allow use of State of the Art design methodology through top-down design techniques.

Features

- ❑ Up to 145,000 usable gates
- ❑ Up to 472 I/O pads
- ❑ 0.8 micron drawn HCMOS technology (0.6 micron effective)
- ❑ Typical gate delay of 325 ps
- ❑ Power dissipation of < 5 µW/gate/MHz
- ❑ Low noise output buffers with up to 24mA drive

- ❑ CMOS/TTL level input drivers
- ❑ Extensive macrocell, logic function libraries
- ❑ RAM, ROM and logic compilers
- ❑ ESD protection in accordance with MIL-STDs
- ❑ Latch-up resistance up to 200 mA
- ❑ Supports State-of-the-Art design platforms

Product Family

Master	Total Gates	Usable Gates [1]	No. Pads	No. I/Os [2], [3]
THA8001	440	210	32	16
THA8002	2,116	1,000	46	30
THA8005	5,472	2,500	66	50
THA8010	9,858	4,500	80	64
THA8013	13,671	6,200	92	76
THA8018	18,000	8,100	100	84
THA8024	24,360	9,800	116	100
THA8031	31,872	13,000	128	112
THA8040	40,500	16,500	144	128
THA8052	52,521	21,000	160	144
THA8063	63,045	24,000	176	160
THA8077	77,850	27,500	192	176
THA8094	94,766	33,500	208	192
THA8110	109,114	38,500	224	208
THA8140	140,592	50,000	252	236
THA8170	171,487	58,500	276	260
THA8210	215,750	70,000	308	292
THA8260	260,150	78,000	336	320
THA8320	320,860	93,000	368	352
THA8390	393,700	110,000	408	392
THA8450	453,750	118,000	436	420
THA8570	573,240	145,000	483	472

Notes: [1] Usable Gates is an estimation and will vary, depending on design
[2] I/O pads can be used as VDD / VSS pads.
[3] Minimum 2 I/O pads must be applied as VDD/VSS for core logic

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