DATEL

ADC-881 Ultra-Linear, 8-Bit A/D Converter

T-51-10-08

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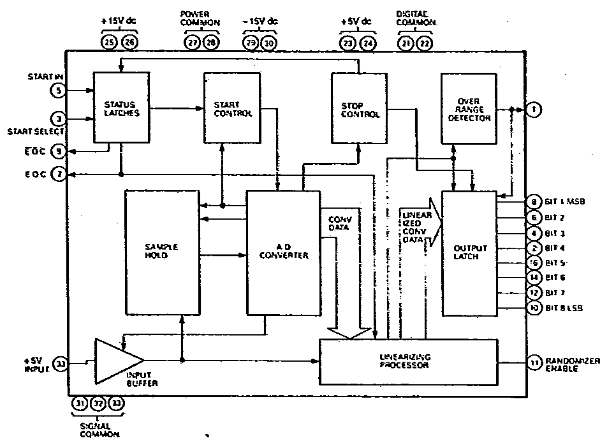
FEATURES

- 8-Bit resolution
- Statistically linearized conversion
- 14-Bit linearity
- ±5V dc input range
- 1.5 Microseconds conversion time
- Out-of-range indication



GENERAL DESCRIPTION

The ADC-881 is an 8-bit analog-to-digital converter with an internal sample-hold. This converter employs a stochastic distributional technique to enhance the statistical (average) linearity by a factor of 11.2, thus achieving a linearity error of only 0.005%. Systematic nonlinearities are scattered in a pseudorandom fashion over the range of the converter, thus appearing as noise rather than nonlinearities. This result is particularly desirable in applications that use the digital output of an A/D converter to compile a histogram. The fundamental properties of any non-distributive A/D converter cause class widths within the histogram to vary from the ideal, thereby artificially increasing or decreasing the frequency within discrete class widths.

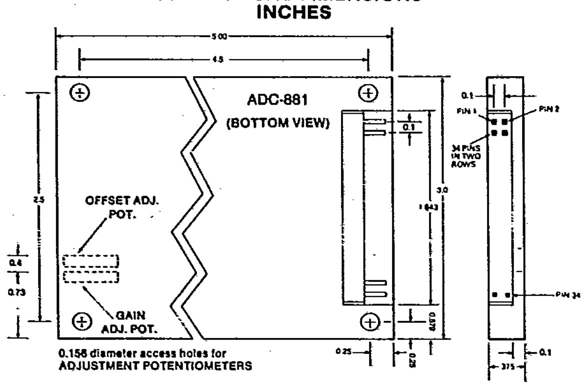
The ultra-linear A/D has a wide range of applications in spectrum analysis, nuclear research, vibration analysis, geological research, sonar digitizing, medical imaging systems, industrial testing and other signal analysis applications.

The ADC-881 has an analog input range of ±5V dc and will accomplish an eight-bit sample and conversion in 1.5 microseconds maximum. Output data is coded as offset binary with an over range output to indicate analog values out of the converter's range.

Additional specifications include a gain tempco of 25 ppm/°C maximum, offset tempco of 25 ppm/°C maximum, zero crossing tempco of 8 ppm/°C maximum and long term stability of ±0.02%/year.

Each converter is a functionally complete unit requiring only ±15V dc and +5V power supplies for operation. The device is packaged in a compact 5" x 3" x 0.375" black enameled steel module. For information on extended temperature range versions contact the factory.

MECHANICAL DIMENSIONS INCHES



0.156 diameter access holes for ADJUSTMENT POTENTIOMETERS

INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	$\overline{\text{OVER RANGE}}$
2	BIT 4
3	START SELECT
4	BIT 3
5	START In
6	BIT 2
7	EOC
8	BIT 1 (MSB)
9	$\overline{\text{EOC}}$
10	BIT 8 (LSB)
11	Random, Enable
12	BIT 7
13	NC
14	BIT 6
15	NC
16	BIT 5
17	Do Not Connect
18	Do Not Connect
19	Do Not Connect
20	Do Not Connect
21	Digital Common
22	Digital Common
23	+5V dc
24	+5V dc
25	+15V dc
26	15V dc
27	Power Common
28	Power Common
29	−15V dc
30	−15V dc
31	Signal Common
32	Signal Common
33	Analog Input
34	Signal Common

FUNCTIONAL SPECIFICATIONS

Typical at +25°C, ±15V dc and +5V dc supplies, unless otherwise noted.

INPUTS	
Analog Input Range	±5V
Analog Input Impedance	14 kΩ
Start Conversion	A pulse[1] 20 nsec. to 80 nsec. duration with rise and fall times less than 10 nsec. Logic "0" = 0V to +0.8V. Logic "1" +2.0 to +5.5V. Conversion commences on the leading edge of the pulse. Loading: 1 LSTTL load.
Start Select	For positive start input pulses, set Start Select to a Logic "1". For negative start input pulses, set Start Select to a Logic "0" or ground.
Randomizer Reset	Hold at logical high for randomizing operations after reset[2]. Loading: 4 LSTTL loads.
OUTPUTS	
Parallel Output Data	8 parallel latched data lines -8 bits binary. V out "0" ≤ +0.4V, V out "1" ≥ +2.4V. Loading: 5 TTL loads
Coding	Offset Binary
$\overline{EOC}$	Conversion Status Signal; High (V out "1" ≥ 2.4V) from 32 nsec. typical after leading edge of Start Convert to 14 nsec. typical after all data outputs are valid. V out "0" ≤ +0.4V. Loading: 5 TTL loads.
EOC	Conversion Status Signal. Complement of EOC. Loading: 5 TTL loads
$\overline{\text{Over Range}}$[3]	Out of Range Signal. High (Vout "1" ≥ +2.4V) for all Signal Input values within ±5V, Low (V out "0" ≤ +0.4V for all Signal Input values beyond ±5V.
PERFORMANCE	
Conversion time[4], max.	1.5 μsec
Resolution	8 Bits
Integral Linearity Error[4]	0.005% of FSR
Differential Linearity Error[5]	0.005% of FSR
Noise (RMS)[6]	0.2% of FSR
Gain Error	Adjustable to zero
Offset Error	Adjustable to zero
Gain Tempco, max.	±25 ppm of FSR/°C
Offset Tempco, max.	±25 ppm of FSR/°C
Zero Crossing Tempco, max.	±8 ppm of FSR/°C
Long Term Stability	±0.02% / year
POWER REQUIREMENTS	
Analog Supply	+15V ±0.5V at 100 mA max. −15V ±0.5V at 100 mA max.
Logic Supply	+5V ±0.25V at 300 mA max.
Power Dissipation, max.	4.5 Watts.
Power Supply Rejection	±0.002%/% supply
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	
ADC-881	0°C to +70°C
ADC-881-EX	−25°C to +85°C
ADC-881-EXX-HS	−25°C to +85°C Hermetic Sealed Semiconductors
Storage Temperature Range	−55°C to +125°C
Package Type	Black enameled 25 gauge CR steel. 5 x 3 x 0.375 in. (127 x 76 x 10 mm)
Weight	6.5 ounces (184 grams)
Connector	0.25" square pins, gold plated phosphor bronze. Mating connector—supplied—is similar to AMP #1-85930-1.

FOOTNOTES:

1. An alternate method for generating Start Input pulses is to drive the Start Input with a rising edge and the Start Select with a falling edge delayed 20 nanoseconds to 80 nanoseconds.
2. After power-up, pin 11 (RANDOMIZER ENABLE) must remain low for at least 25 nanoseconds to reset the pseudo-random signal generator and to clear other gating circuitry.
3. When the Signal Input is less than −5V, the Data Output lines are all "0". When the Signal Input is greater than +5V, the Data Output lines are all "1".
4. Conversion Time is measured from the leading edge of the Start Conversion input to the trailing edge of the $\overline{EOC}$ output.
5. The Linearity Error is the systematic error which remains after a sufficient number of samples have been averaged to suppress the noise.
6. The RMS noise value is reduced by the second root of the number of samples that have been averaged.

ABSOLUTE MAXIMUM RATINGS

Positive Supply	+18V dc
Negative Supply	+18V dc
Logic Supply	+7V dc
Digital Supply	+5.5V dc

THEORY OF OPERATION

The ADC-881 employs a statistically linearized conversion technique that yields unique advantages in many applications. This technique uses a fundamental property of all A/D converters, differential nonlinearity, in a pseudo-random distributional technique to yield a converter with an "ideal" transfer function. This technique scatters the effects of systematic nonlinearities over the full range of the A/D in pseudo-random (a random sequence of finite length) fashion. The average transfer function, taken over the full range of the pseudo-random sequence, has extremely good integral linearity and minimal differential non-linearity. The trade-off appears here as "noisy" codes, this is the result of distributing systemic nonlinearities over a wide range. Noise may be suppressed by repeated sampling of the data since the average value of true random noise is zero. The RMS noise value of the data is reduced by the second root of the number of samples less one that have been averaged.

Since this converter's extreme linearity is realized in an average transfer function, it follows that averaging a larger number of conversions will improve linearity. This is true, with maximal linearity resulting as an average of all values within the pseudo-random sequence (127 random values). Since the ADC-881 has conversion times of 1.2 microseconds typical and 1.5 microseconds maximum, this averaging procedure will require between 165 and 191 microseconds (127 conversions x conversion time). In applications where repeated sampling is employed to reduce noise, this converter yields optimal linearity when the number of samples averaged is an integral multiple of 127 (this is inherent in the stochastic distributional technique used).

OFFSET AND GAIN CALIBRATION PROCEDURE

T-51-10-08

1. Connect the A/D converter to external test circuitry shown in "Calibration Connection" diagram with no power applied.
2. Apply power to the A/D converter and test circuitry and allow them to reach operating temperature.
3. Observe the A/D output as a crossplot on the oscilloscope. Calibrate the axis gain for one cm per step and adjust the crossplot dither amplitude for 10 cm. Calibrate the Y axis for an easily read crossplot.
4. Apply a precision voltage reference set to −5V dc to the analog input (pin 33). Observe the crossplot as shown in Figure 1. The last step should be centered on the vertical grid line one cm to the left of center. Adjust the offset potentiometer as necessary to achieve this positioning.
5. Set the precision voltage reference to +5V dc. Observe the crossplot as shown in Figure 2. The last step should be centered on the vertical grid line two cm. to the right of center. Adjust the gain potentiometer as necessary to achieve this position.
6. Repeat steps 4 and 5 until no further adjustment is required. Repetition is necessary, as the offset and gain adjustments interact. The following technique will minimize the number of adjustments. After the initial adjustment outlined in steps 4 and 5, repeat step 4. At this point repeat step 5, over-adjusting the gain potentiometer so that the error displayed maintains its initial magnitude but occurs in a direction opposite from its original one. For instance, if the crossplot is 1.5 cm to the left of its desired position, adjust the gain potentiometer so that the crossplot is 1.5 cm to the right of its desired position. Repeat steps 4 and 5; the crossplot should now show optimum position.

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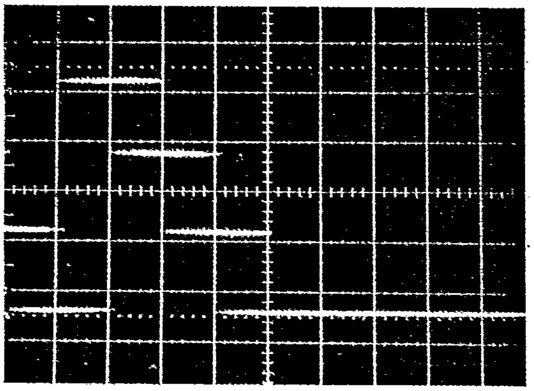


Figure 1. Negative Voltage Display

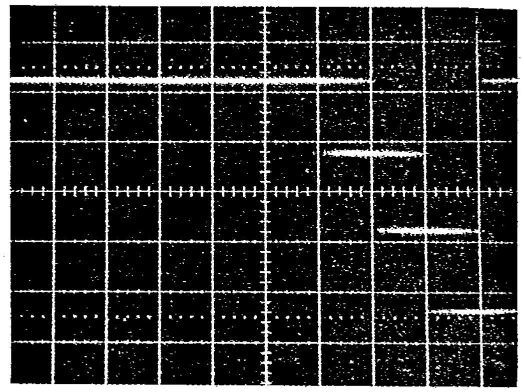
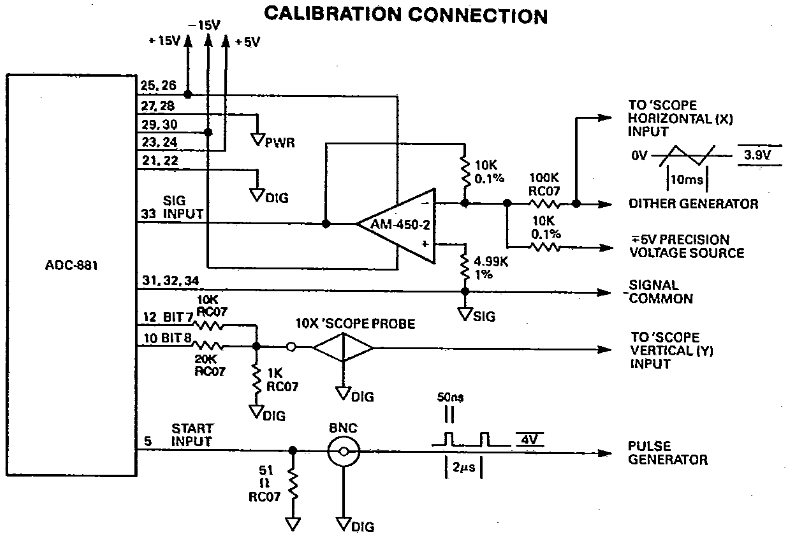


Figure 2. Positive Voltage Display

CALIBRATION CONNECTION



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APPLICATION NOTE

The largest group of applications for this class of converters is in areas in which recurring systematic nonlinearities have an adverse effect on the distribution of acquired data values. This is particularly of interest in situations where data is required to compile a histogram (a frequency distribution of sample data into discrete categories). The effects of converter nonlinearities cause some categories to be artificially "widened" while others are "narrowed", thus increasing and decreasing, respectively, the frequence of occurrence of data values within these categories.

This effect causes a non-linearized converter to yield a "converter distorted" histogram. Until now many users had to resort to extensive computational processing of digitized data simply to minimize the effects of "converter distortion." The architecture of the ADC-881 obviates the need for this, allowing statistically valid processing of analog data in real-time. Thus we see that the ADC-881 is ideally suited for applications in spectrum analysis, particle event monitors, fast signal processing, vibration analysis, sonar digitizing, and a whole spectrum of imaging applications, from medical imaging to industrial non-destructive testing.

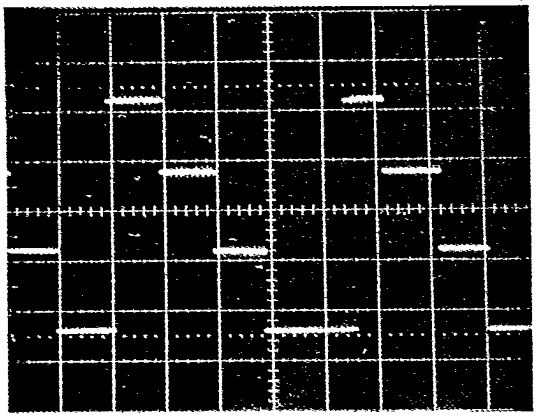

Figure 3. The output of a non-linearized 8 bit A/D converter is shown above. The display shows the 4 least significant bits at the major carry transition demonstrating differential nonlinearity. This is a property of all nonlinearized A/D converters. (The unit used for this example is a typical non-linearized A/D with ± ½ LSB of integral linearity and ± ½ LSB of differential nonlinearity).

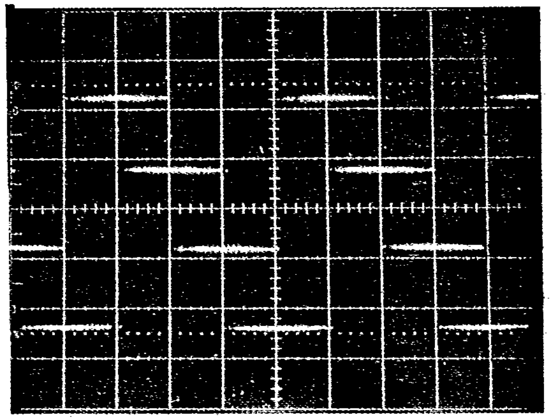

Figure 4. The output of a linearized 8 bit A/D shown for the 4 least significant bits at the major carry. Notice the improvement in differential nonlinearity. This photo shows the effect of averaging multiple conversions performed with the linearizing technique employed in the ADC-881.

ORDERING INFORMATION

MODEL NO.	OPERATING TEMP. RANGE
ADC-881	0°C to +70°C

For information on extended temperature range and high reliability versions of this product, contact factory.

THIS PRODUCT IS COVERED BY GSA CONTRACT.

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